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*Research Article*

# Carrier-Based Common Mode Voltage Control Techniques in Three-Level Diode-Clamped Inverter

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Switching converters are used in electric drive applications to produce variable voltage, variable frequency supply which generates harmful large $dv/dt$ and high-frequency common mode voltages (CMV). Multilevel inverters generate lower CMV as compared to conventional two-level inverters. This paper presents simple carrier-based technique to control the common mode voltages in multilevel inverters using different structures of sine-triangle comparison method such as phase disposition (PD), phase opposition disposition (POD) by adding common mode voltage offset signal to actual reference voltage signal. This paper also presented the method to optimize the magnitude of this offset signal to reduce CMV and total harmonic distortion in inverter output voltage. The presented techniques give comparable performance as obtained in complex space vector-based control strategy, in terms of number of commutations, magnitude, and rate of change of CMV and harmonic profile of inverter output voltage. Simulation and experimental results presented confirm the effectiveness of the proposed techniques to control the common mode voltages.

## 1. Introduction

In the medium-voltage, high-power adjustable speed drive (ASD) system, AC supply is first converted into DC (known as DC buffer stage) and then converting back this DC into variable voltage variable frequency AC supply using inverter (voltage source or current source type). Figure 1 shows the general block diagram of AC-DC-AC induction motor drive system. The front-end converter may be uncontrolled or controlled voltage source or current source rectifier while the motor side converter can be conventional two-level or multilevel VSI, CSI. In VSI fed drive, the DC link capacitor $C_d$ ($C_1$ and $C_2$) is sufficiently large and DC link inductor $L_d$ is not required whereas in CSI fed drive, $L_d$ is sufficiently large and $C_d$ is not needed [1, 2].

The DC buffer stage consists of only large capacitor in the case of voltage source inverter and only large inductor in the case of current source inverter. This process involves switching power semiconductors to manipulate the magnitude and frequency of the output waveforms. The switching action of rectifiers and inverters results in common mode voltages which are essentially zero-sequence voltages superimposed with switching noise which will appear at rectifier, inverter, and motor terminals [1, 2]. If not mitigated, they appear on the neutral of the stator winding with respect to ground, which should be zero when the motor is powered by a three-phase balanced utility supply. Further, the motor line-to-ground voltage, which should be equal to the motor line-to-neutral (phase) voltage, can be substantially increased due to the common mode voltages, leading to premature failure of motor winding insulation system. As a consequence, the motor life expectancy is shortened. This phenomenon is different from the high $dv/dt$ caused by the switching transients of the high-speed switches [3–6].

Therefore, it is necessary to control/eliminate the common mode voltage magnitude and its rate of change.

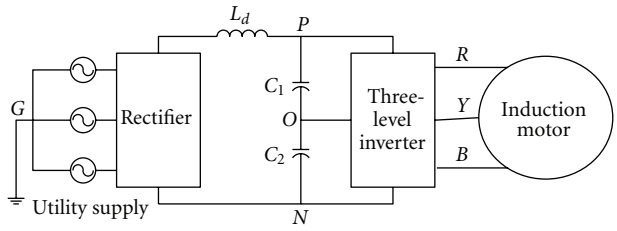



Figure 1: General block diagram of AC-DC-AC VSI or CSI fed ASD (only $L_d$ in CSI and only $C_1$, $C_2$ in VSI).

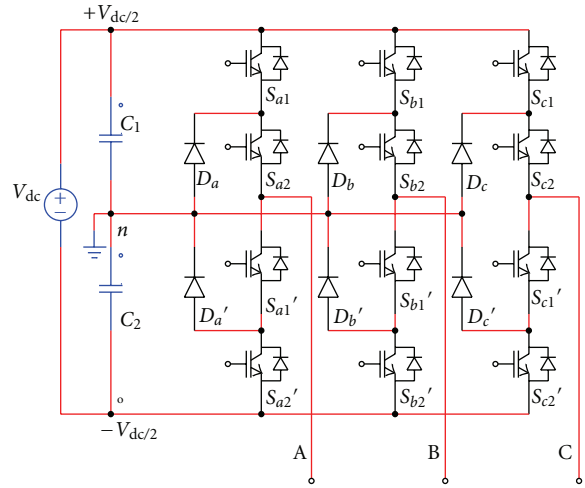



Figure 2: Schematic diagram of three-phase, three-level diode-clamped inverter.

Common mode voltage reduction/elimination techniques, available in literature, can be classified as given below [1–6]:

(A) using some extra hardware circuitry such as isolation transformer, zero-sequence impedance (common mode choke), active and passive filters, dual bridge inverter, using four-leg (four-phase) inverter, or

(B) using modification in control strategy employed based on space vector PWM technique (SVPWM) or sinusoidal PWM technique (SPWM).

Techniques mentioned in (A) above increases the system cost and complexity in control with reduced reliability. Techniques mentioned in (B) are commonly used. In SVPWM techniques, the switching state voltage vectors generating zero common mode voltage are only used [7, 8]. Various forms of SVPWM techniques are available to mitigate the common mode voltage problem, that is, nearest three vector selection (NTV) SVPWM, radial state SVPWM zero common mode voltage SVPWM, and so forth [8]. CMV reduction in adjustable speed drive system and its rate of change play an important role in designing electromagnetic interference (EMI) filters. SVPWM-based techniques for this purpose requires comparatively complex algorithm [7, 9–12].

In industrial applications requiring variable voltage, variable frequency supply to fed three-phase induction motors at medium- and high-voltage levels, multilevel inverters (MLI) have been found better counterpart to conventional two-level inverters. MLI produce lower common mode voltage stress across converter and motor terminals. Carrierbased modulation techniques are most widely used in MLI, especially in neutral point clamped (NPC) inverter. For cascaded H-bridge inverters, phase shifted carrier-based modulation techniques are most widely used with some derived strategies for improved performance [6, 8]. However, research is going on SVPWM-based technique to solve some inherent problems in NPC inverters, carrier-based SPWM techniques remain widely adopted because of their simplicity and reduced computational requirements as compared to SVPWM technique. Recent work reported in [6, 13–17] shows that carrier-based SPWM and SVPWM techniques for MLI are equivalent. Due to inherent problem of unequal properties of two DC link capacitors, inverter voltage gets unbalanced which can be made balanced easily by using the technique presented in [17, 18].

A current control strategy is presented in [19] to reduce the maximum common mode voltage levels of a three-phase inverter in adjustable speed drive applications. A hybrid selective harmonic elimination PWM scheme is given in [20] for common mode voltage reduction in three-level neutral-point-clamped inverter-based induction motor drive system. It automatically corrects the modulation index level to control the number of switching per cycle and also improves the load voltage and current waveform quality. Loh et al. presented the space vector PWM-based modulation

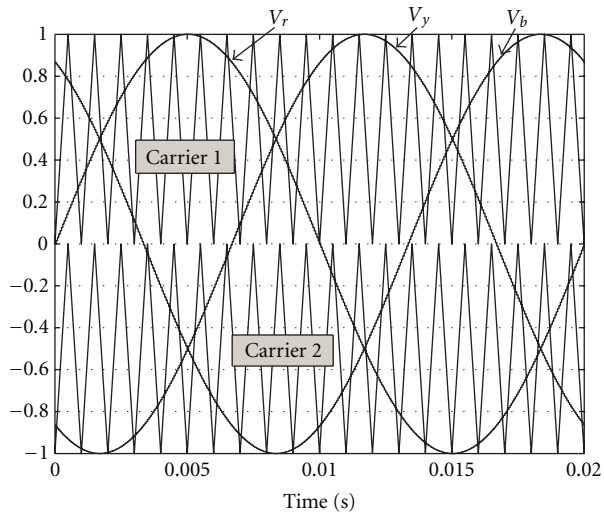



Figure 3: Generation of control pulses for 3-level inverter with PD SPWM technique.

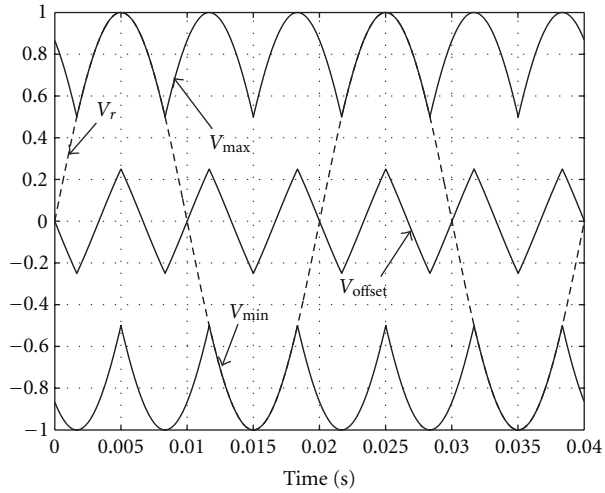



Figure 4: Signals "$V_{\max}$," "$V_{\min}$," "$V_r$," and offset voltage "$V_{\text{offset}}$" in offset PD SPWM technique.

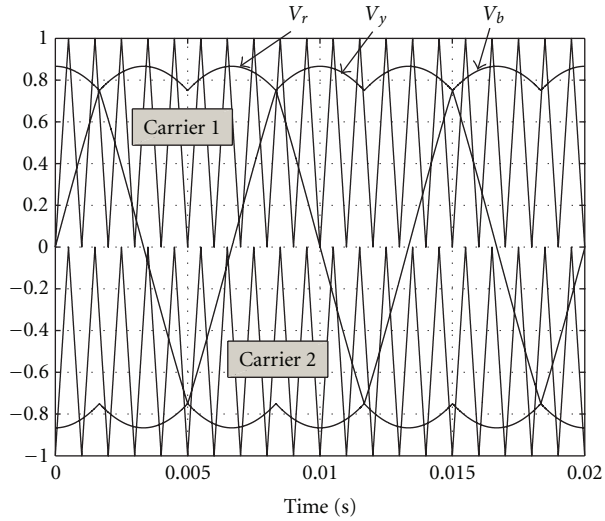



Figure 5: Generation of pulses for 3-level inverter with offset PD SPWM technique.

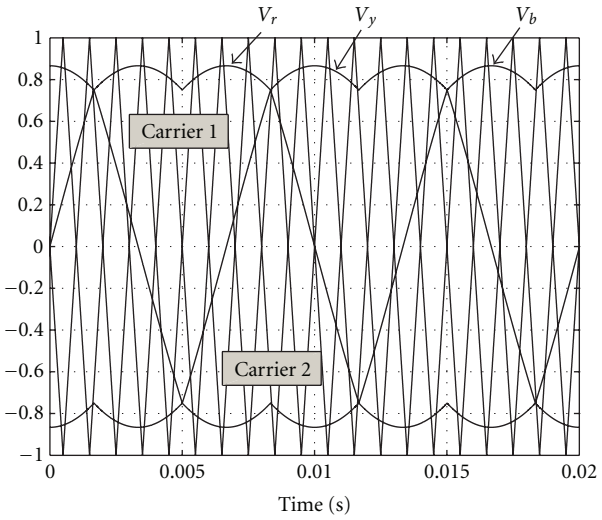



Figure 6: Generation of pulses for 3-level inverter with offset POD SPWM technique.

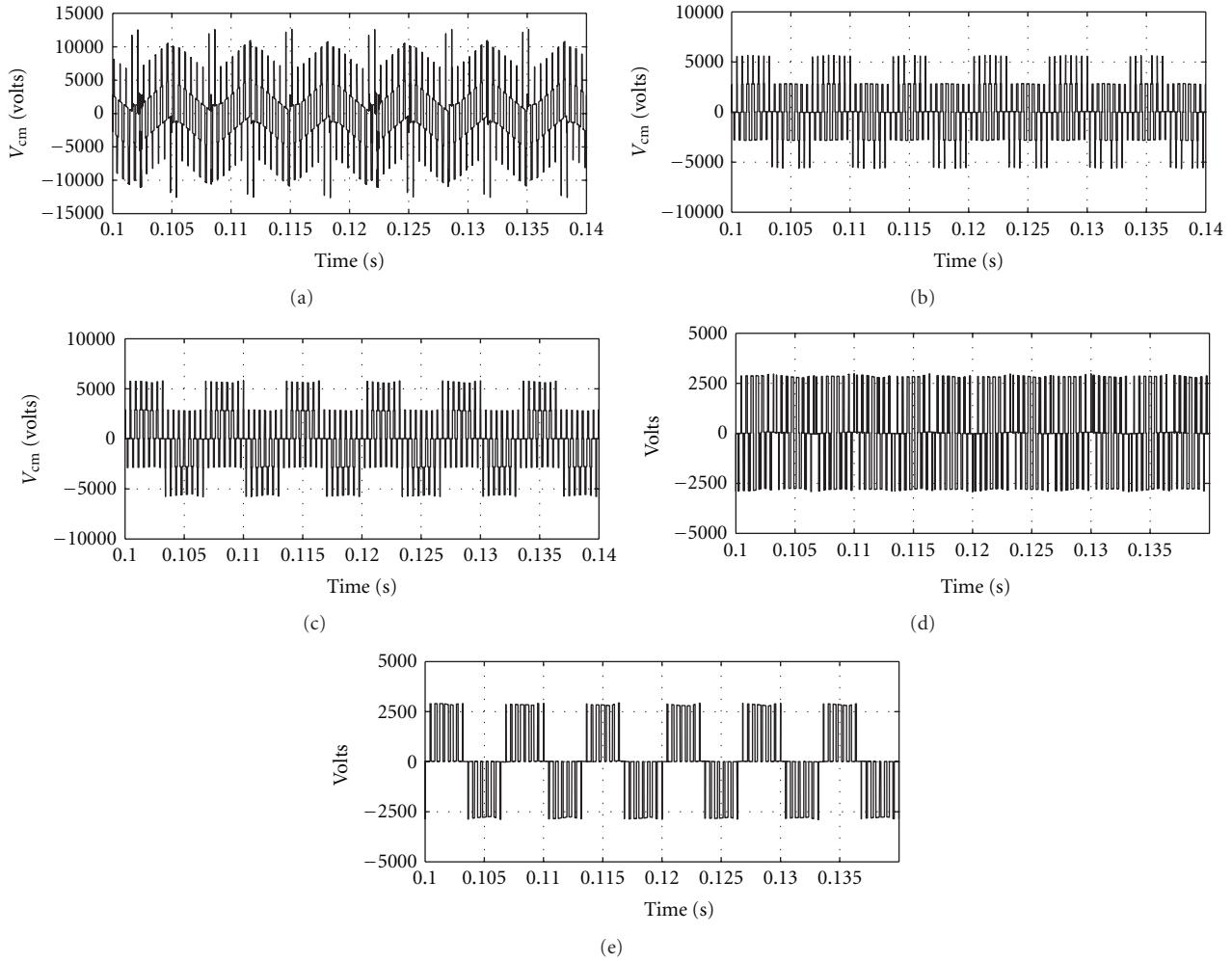



Figure 7: Common mode voltages in (a) 2-level inverter, (b) PD SPWM, (c) PD SPWM with offset voltage signal, (d) POD SPWM, and (e) POD with offset voltage signal.

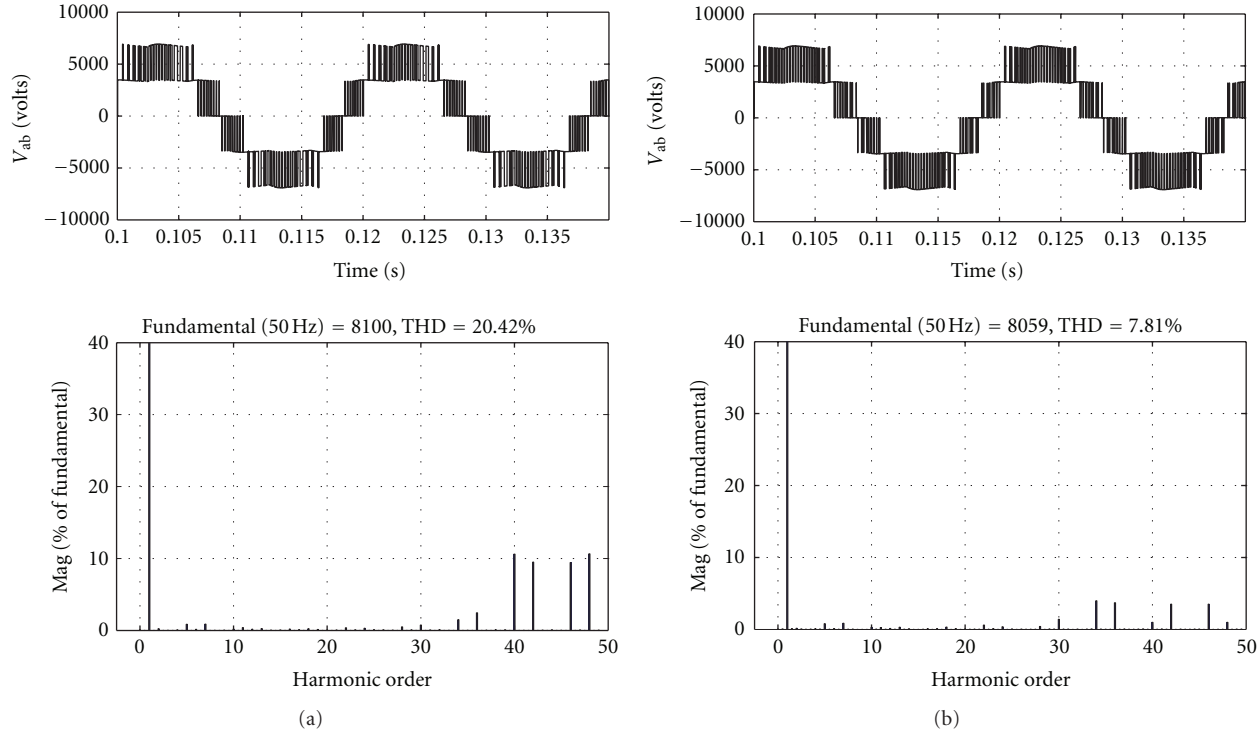



Figure 8: Inverter output voltage and its harmonic spectrum with (a) PD SPWM and (b) offset PD SPWM.

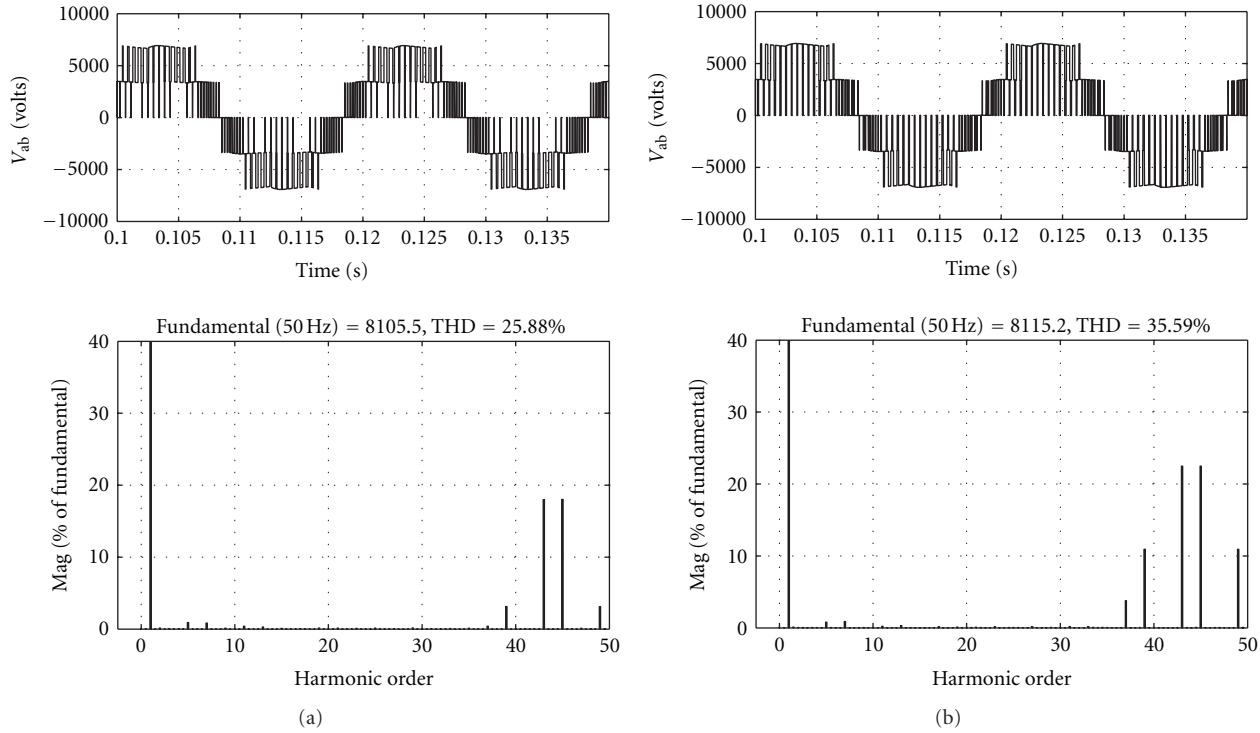



Figure 9: Inverter output voltage and its harmonic spectrum with (a) POD SPWM and (b) offset POD SPWM.

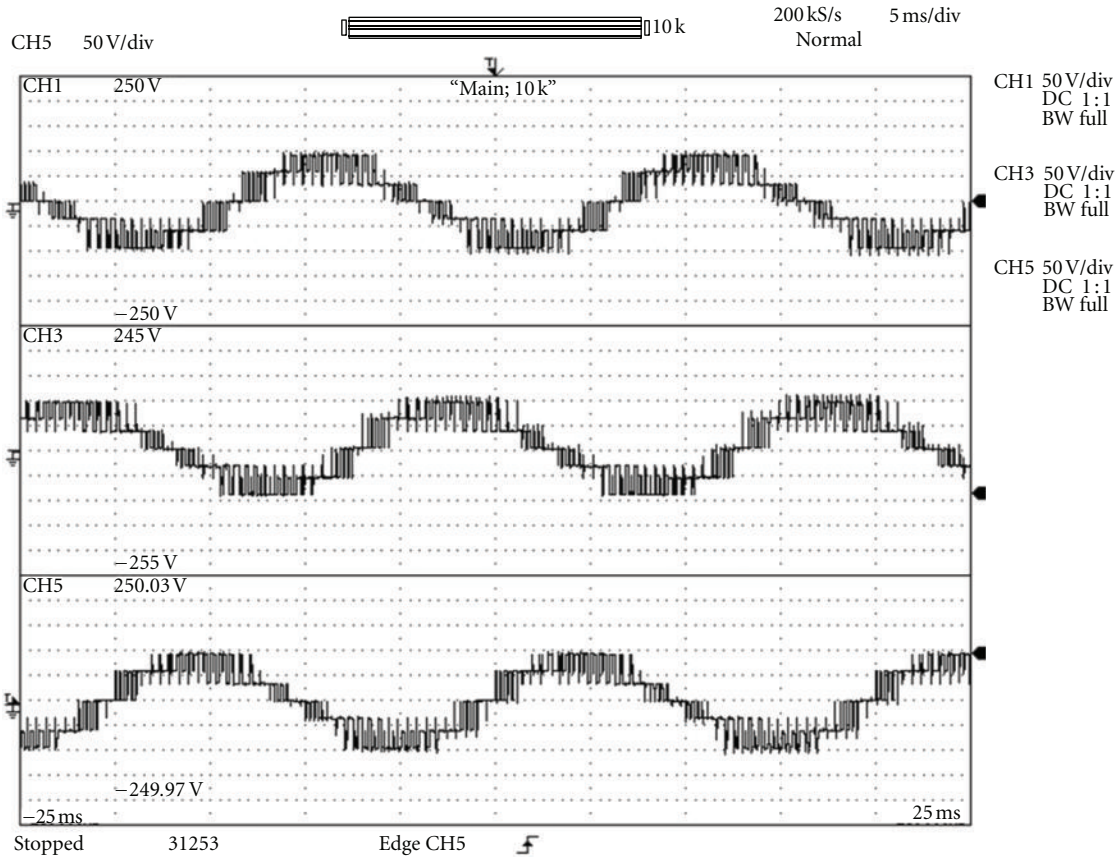



FIGURE 10: Inverter output voltages $V_{ab}$, $V_{bc}$, and $V_{ca}$ with PD SPWM technique ($x$-axis: 5 ms/div, $y$-axis: 50 V/div).

techniques to reduce the common mode voltage in cascaded multilevel inverter [21]. The techniques used by Loh were phase disposition, phase opposition disposition, and alternate phase opposition disposition with phase shifting algorithm using space vector PWM.

Holmes and others [14–16] presented analytical expressions for different voltages using FFT analysis for cascaded and hybrid multilevel inverters. The modulation technique used was alternate phase opposition disposition and phase shifted carrier PWM for 5-level cascaded and hybrid multilevel inverters. Simple SPWM-based techniques have been proposed in the presented work to control the CMV in AC-DC-AC ASD system. The proposed SPWM-based control techniques are based on phase disposition (PD) and phase opposition disposition (POD) concepts with addition of offset voltage signal to actual reference signal.

The second section reviews the various common mode voltage control techniques and explains the proposed concept to control CMV. Simulation performance of the proposed control technique is given in section three. Experimental verification of proposed techniques is presented in section four. Section five gives conclusion.

## 2. Common Mode Voltage Control

Various common mode voltage reduction/elimination techniques can be classified as given below.

(A) Using some extra hardware circuitry such as

(i) isolation transformer;

(ii) zero-sequence impedance (common mode choke);

(iii) active and passive filters;

(iv) dual bridge inverter;

(v) using four-leg (four-phase) inverter.

(B) Using modification in control strategy employed such as, based on

(i) space vector PWM technique (SVPWM);

(ii) sinusoidal PWM technique (SPWM).

The proper choice of common mode choke provides high impedance to common mode current and can eliminate the CMV. Further, any practice to eliminate CMV may increase the common mode current [9, 11]. Thus, investigation is required on this issue. The main issue is that the THD and switching losses increase with controlling the CMV. During the control pulse generation in multilevel inverters, some switching states produce reduced/zero common mode voltage across motor windings and inverter output terminals.

In SVPWM techniques, the switching state voltage vectors generating zero common mode voltage are only used

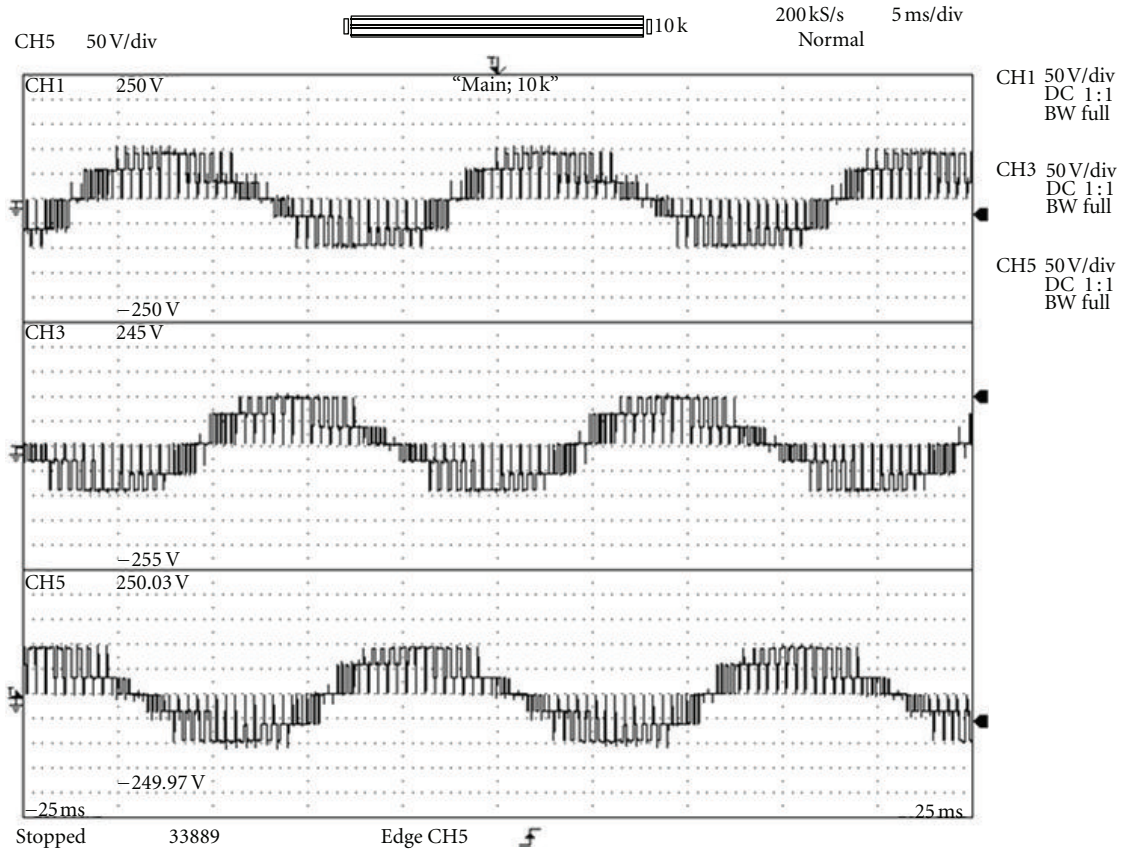



Figure 11: Inverter output voltages $V_{ab}$, $V_{bc}$, and $V_{ca}$ with POD SPWM technique ($x$-axis: 5 ms/div, $y$-axis: 50 V/div).

Table 1: Simulation parameters.

| | |
|---|---|
| DC link voltage | 10.16 kV |
| Load power | 2.45 MW |
| Load voltage | 6.6 kV |
| Load current | 256 amps |
| Load power factor | 0.84 |
| Carrier frequency | 2.2 kHz |

[7, 8]. Various forms of SVPWM techniques are available to mitigate the common mode voltage problem, that is, nearest three vector selection (NTV) SVPWM, radial state SVPWM, zero common mode voltage SVPWM, and so forth [8].

In ASD system, magnitude and rate of change of CMV play an important role in designing EMI filters. SVPWM-based techniques for this purpose require comparatively complex algorithm [7, 9–12]. On the other hand, SPWM-based techniques require less complex algorithm with ease to implement.

This section presents various simple SPWM-based techniques controlling the magnitude and rate of change of CMV. Different SPWM techniques can be classified as [14–16]

(i) phase disposition (PD) method,

(ii) phase opposition Disposition (POD) method,

(iii) phase-shifted (PS) method,

(iv) hybrid (H) method,

(v) Third harmonic injection (THIPWM) method.

Figure 2 shows the schematic diagram of three-phase, three-level diode-clamped inverter. Figure 3 shows the principle of generation of control pulses for 3-level inverter with conventional PD SPWM technique. Fundamental frequency three-phase sinusoidal reference waves $V_r$, $V_y$, and $V_b$ are compared with two high-frequency triangular carrier waves "carrier 1" and "carrier 2". Each intersection gives rise to the control pulses for switching devices of inverter. These reference sinusoidal waves, $V(r, y, b)$ can be represented by

$$\begin{aligned} V_r &= V_m \sin(\omega t), \\ V_y &= V_m \sin(\omega t - 120^\circ), \\ V_b &= V_m \sin(\omega t - 240^\circ). \end{aligned} \tag{1}$$

The control pulses generated by comparison of reference voltage wave with "carrier 1" are given to upper switches ($S_{a1}$, $S_{b1}$, $S_{c1}$) of inverter shown in Figure 2. The corresponding complementary signals of these pulses are given to ($S_{a1}'$, $S_{b1}'$, $S_{c1}'$). The control pulses generated by comparison of reference voltage wave with "carrier 2" are given to switches ($S_{a2}$, $S_{b2}$, $S_{c2}$). The corresponding complementary signals of these pulses are given to ($S_{a2}'$, $S_{b2}'$, $S_{c2}'$).

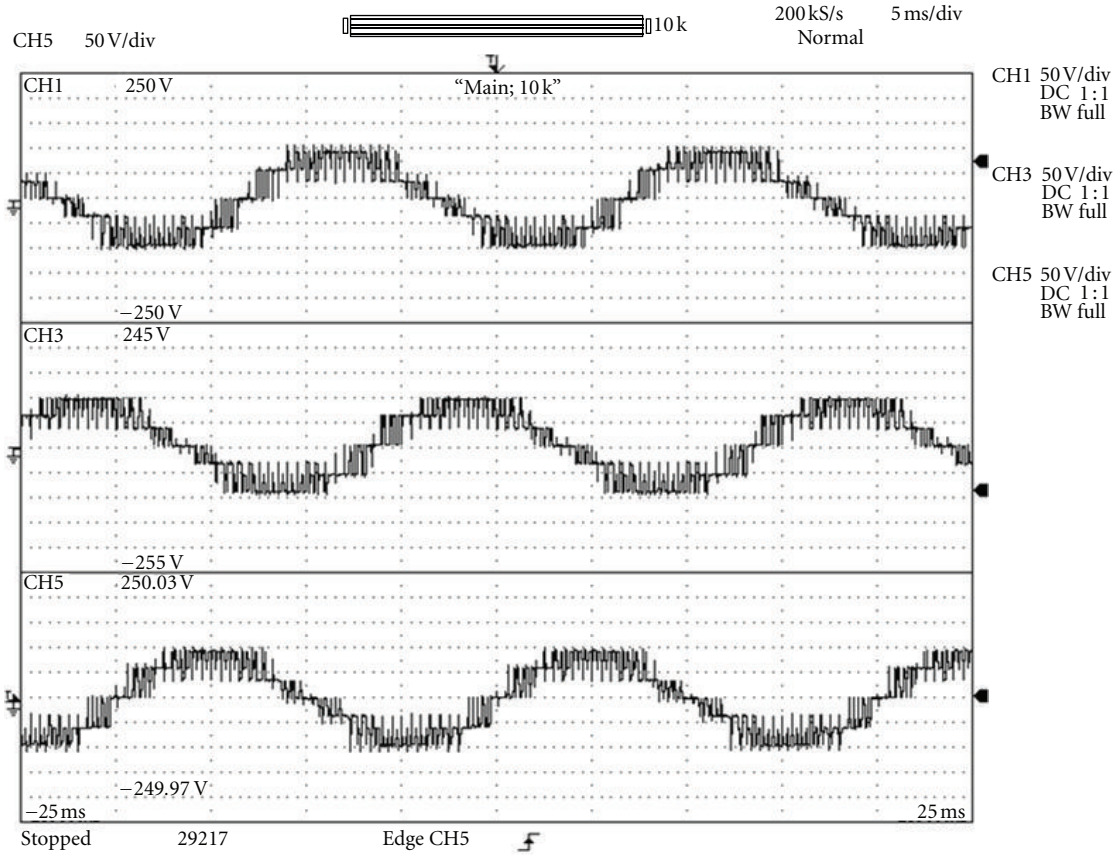



Figure 12: Inverter output voltages $V_{ab}$, $V_{bc}$, and $V_{ca}$ with offset PD SPWM technique ($x$-axis: 5 ms/div, $y$-axis: 50 V/div).

*2.1. Proposed Method of CMV Control.* Common mode voltage magnitude and its rate of change depend on the control pulse width, number of commutation, and its frequency which can be modified by adding some offset signal to reference voltage wave. Offset voltage plays an important role in modifying the modulating signal. This section gives the basic idea of adding the offset signal to PD and POD SPWM techniques. Common mode voltage or zero sequence voltage in output voltage of inverter can be represented by

$$V_{\text{cm}} = \frac{\left(V_r + V_y + V_b\right)}{3}, \tag{2}$$

where, $V_r$, $V_y$, and $V_b$ are the phase voltages of inverter. This voltage is around DC link voltage in conventional 2-level inverters and half of the DC link voltage in 3-level inverter. To reduce it, following common mode offset voltage is to be added

$$V_{\text{off}} = -\frac{\left[\min\left(V_r, V_y, V_b\right) + \max\left(V_r, V_y, V_b\right)\right]}{2}, \tag{3}$$

where $\min(V_r, V_y, V_b)$ and $\max(V_r, V_y, V_b)$ are the minimum and maximum functions of reference voltage wave. New reference or modulating wave can be calculated by adding this common mode offset voltage signal to original reference voltage wave as

$$V^*(r, y, b) = V(r, y, b) + V_{\text{off}}, \tag{4}$$

where, $V(r, y, b)$ is given by (1). The "max", "min", one-phase voltage $V_r$ and offset voltage signal, according to (1) to (4), are shown in Figure 4 for PD SPWM technique. This common mode voltage offset signal controls the CMV in inverter output. Figures 5 and 6 give the new 3-phase reference waves as obtained from (4) in PD and POD SPWM techniques. In POD SPWM technique, the two carrier signals are in phase opposition as shown in Figure 6.

## 3. Simulation Results

The proposed CMV control techniques are now verified in simulation. The simulation parameters for common mode control are given in Table 1 for medium voltage, 3-phase, squirrel cage induction motor.

The CMV in 2-level inverter is compared with CMV in 3-level SPWM techniques using the proposed offset voltage SPWM techniques. Figure 7 shows the common mode voltages in 2-level and different 3-level SPWM techniques indicating the effect of adding the CMV offset signal. Figures 8 and 9 show the inverter output voltage and its harmonic spectrum with PD SPWM, Offset PD SPWM, POD SPWM, and offset POD SPWM.

The magnitude of CMV is reduced as we move from 2-level to 3-level SPWM technique or from PD to POD SPWM technique as shown. The frequency of CMV is three times the fundamental frequency of inverter output voltage.

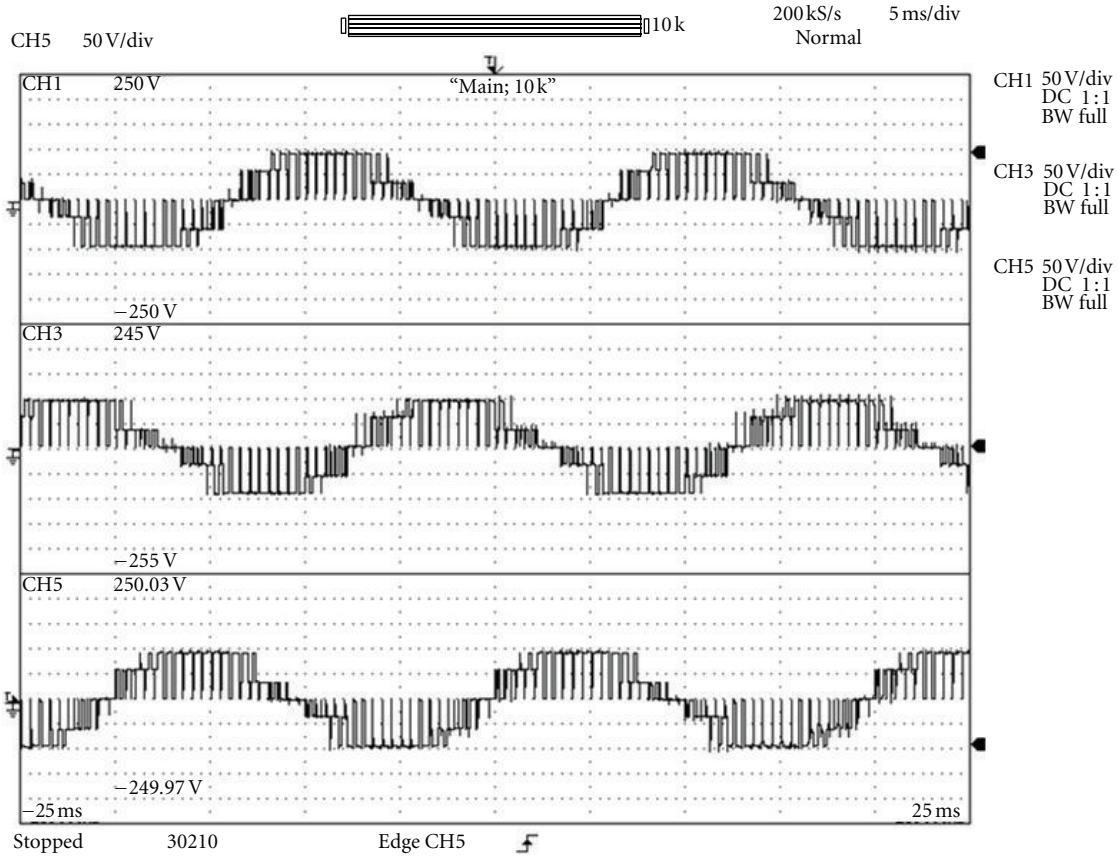
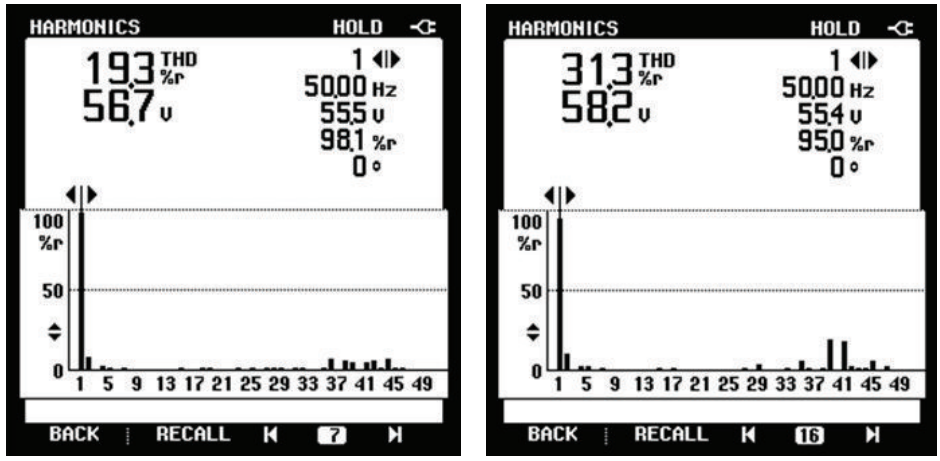



Figure 13: Inverter output voltages $V_{ab}$, $V_{bc}$, and $V_{ca}$ with offset POD SPWM technique ($x$-axis: 5 ms/div, $y$-axis: 50 V/div).



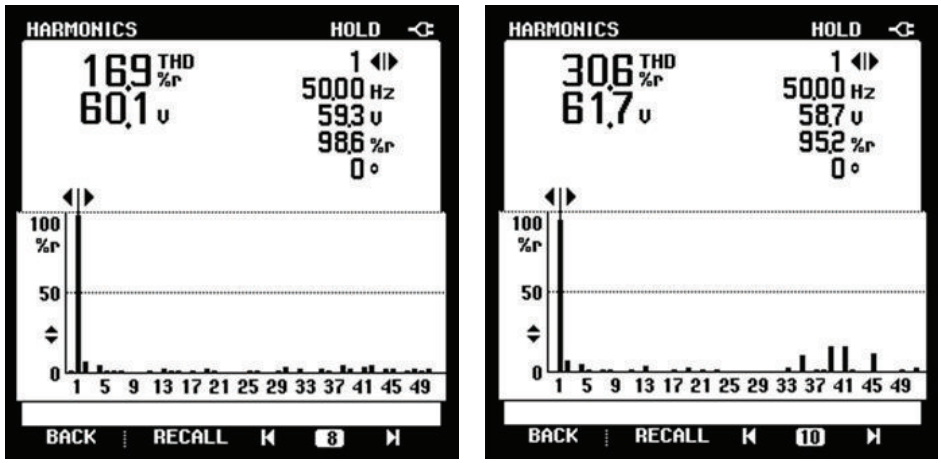

(a) (b)

Figure 14: Frequency spectrums of inverter output line voltage ($V_{ab}$) with (a) PD SPWM and (b) POD SPWM techniques.

POD with offset signal gives better CMV behavior but at the cost of increased voltage THD. While PD SPWM with offset signal gives much better voltage THD performance (7.81% without any filter) with reduced switching transients in CMV as compared to PD SPWM and other techniques.

The magnitude, ripples, and number of commutations in CMV at inverter and load terminals in POD with offset signal are greatly reduced. Comparison of inverter voltage THD for these techniques is given in Figures 8 and 9, respectively.

The switching frequency is increased in PD with offset signal technique which can be controlled by the method




(a) (b)

Figure 15: Frequency spectrums of inverter output line voltage ($V_{ab}$) with (a) offset PD SPWM and (b) offset POD SPWM techniques.

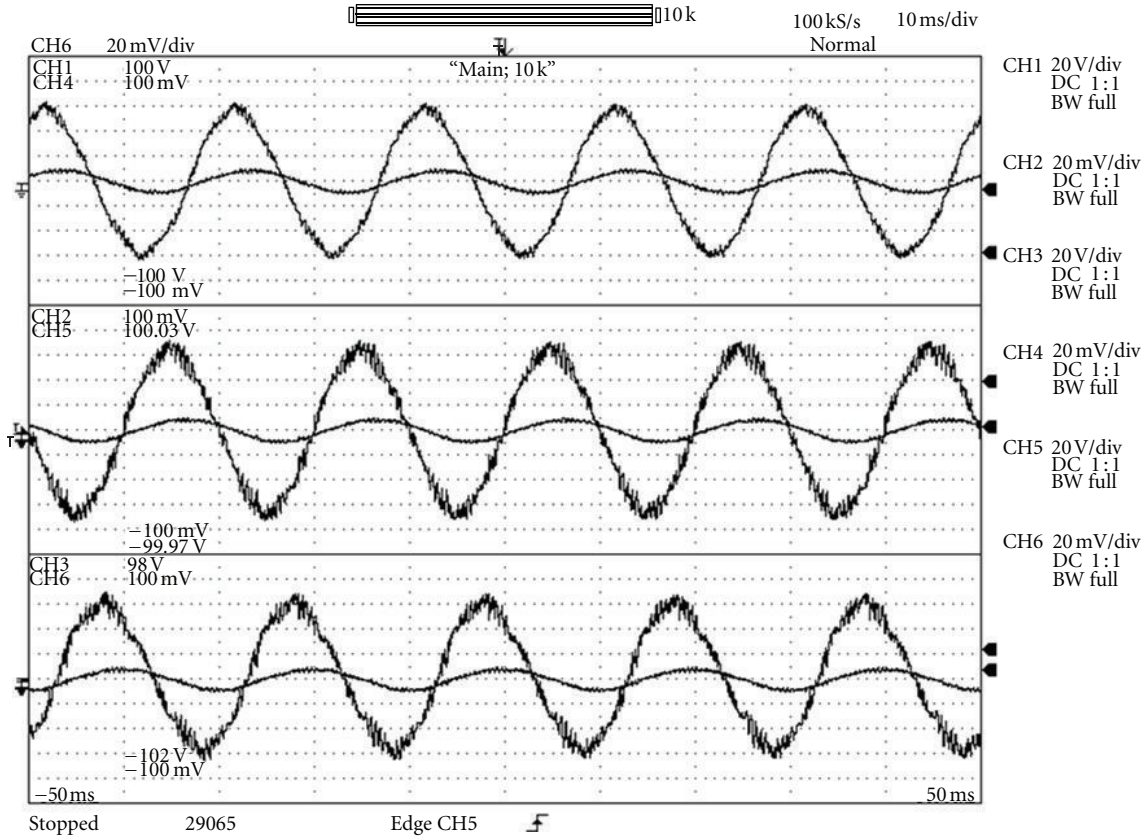



Figure 16: Load voltages and load currents PD SPWM technique ($x$-axis: 10 ms/div, $y$-axis: voltages-20 V/div, currents-5 A/div).

proposed in [17]. However, the change in line voltage across switching devices is two times in POD and offset POD method as compared to PD and offset PD method as given in Figure 9. It compensates any increase in switching frequency because switching losses depend on instantaneous voltage and current across and through the switch, respectively. Table 2 provides comprehensive comparison of these techniques based on inverter voltage/current THD (without/with passive filter), average CMV, and average neutral point potential (NPP).

## 4. Experimental Results

A laboratory prototype of three-phase, diode-clamped or neutral-point-clamped inverter has been developed for experimentation. The experimental parameters are listed in

Table 2: Comparison of CMV control techniques.

| SPWM technique | Without filter | | | | With filter ($L$ = 1.2 mH, $C$ = 100 uF) | | | | Average NPP (Vnp) volts | Average CMV (Vcm) volts |
|---|---|---|---|---|---|---|---|---|---|---|
| | Line voltage (kV) | | Line current (amps) | | Line voltage (kV) | | Line current (amps) | | | |
| | $V_{1ab}$ | % THD | $i_{1a}$ | % THD | $V_{1ab}$ | % THD | $i_{1a}$ | % THD | | |
| PD | 8.1 | 20.51 | 254 | 28.39 | 15.6 | 3.13 | 256 | 0.86 | 8.3 | 59.2 |
| POD | 8.1 | 25.97 | 250 | 32.57 | 15.6 | 2.92 | 254 | 0.78 | 16.1 | 69.1 |
| PD + off-set voltage | 8.0 | **7.81** | 254 | **18.16** | 15.6 | **3.24** | 258 | **0.85** | **1.4** | **25.3** |
| POD + off-set voltage | 8.1 | 35.63 | 257 | 43.43 | 15.6 | 3.39 | 259 | 0.77 | 8.3 | 59.6 |

Table 3: Experimental parameters.

| | |
|---|---|
| DC link voltage | 100 volts |
| DC link capacitor | 2200 $\mu$F (each) |
| Load resistance | 45 $\Omega$ |
| Load inductance | 5.2 mH |
| Carrier frequency | 2 kHz |

Table 3. The dSPACE DS1104 has been used for real-time control of the inverter.

The inverter line voltages are shown in Figures 10, 11, 12 and 13 for PD, POD, offset PD, and offset POD techniques, respectively. It is clearly shown that the frequency of switching per half cycle and the rate of change of switch voltage is different in each case. Slight unbalance in line voltage is due to no load operation. The DC link voltage balancing has been given in [17, 18] which not only balances the DC link voltages but also reduces the switching losses.

Figure 14 shows the frequency spectrums of inverter output line voltage ($V_{ab}$) with (a) PD SPWM, and (b) POD SPWM techniques, respectively. Figure 15 shows the frequency spectrums of inverter output line voltage ($V_{ab}$) with (a) offset PD SPWM, and (b) offset POD SPWM techniques, respectively. It is clearly shown that minimum THD occurs in offset PD SPWM technique and maximum fundamental load voltage is available in offset POD SPWM technique. Second-order harmonics is present in each case because of slight unbalance in DC link voltages which can be easily balanced by using the technique given in [18]. Figure 16 shows the waveforms of load voltages and load currents with PD SPWM techniques. Figure 17 shows the frequency spectrums of load voltage ($V_{ab}$) and load current ($i_a$) with PD SPWM technique. These experimental results are comparable with the simulation results presented in Figures 8 and 9.

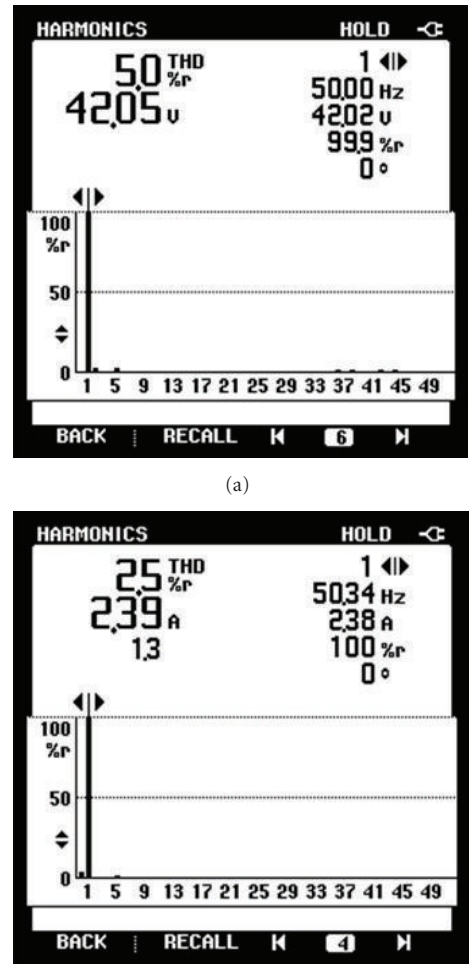



Figure 17: Frequency spectrums of load voltage ($V_{ab}$) and load current ($i_a$) with PD SPWM technique.

## 5. Conclusion

This paper explored the opportunities of common mode voltage (CMV) control using simple sine-triangle comparison techniques for 3-level diode-clamped inverter. CMV at inverter terminals has been obtained and compared for 2-level, 3-level PD SPWM, and 3-level POD SPWM techniques. Further, a new method for reduction of CMV based on SPWM technique has been derived based on the addition of variable CMV offset signal to the original modulating wave.

Simulation and experimental results show the effectiveness of the proposed techniques giving improved performance with the reduction of magnitude and number of commutations per cycle in CMV. It shows that offset PD SPWM gives drastically reduced voltage THD (7.81%) without using any filter. These values are much lower as compared to their counterpart 2-level (52.48%), 3-level PD SPWM (20.51%), and POD SPWM (25.97%). Average value of neutral point potential (NPP) and CMV are minimum in

offset PD SPWM technique. The sharp edges in CMV with conventional SPWM technique are also reduced with the proposed method. Experimental results are comparable with the simulated results. The problem of slight unbalancing in DC link voltages as evident from experimental results can be solved by using the technique presented in [17, 18].

## References


[1] J. Pontt, J. Rodríguez, and R. Huerta, "Mitigation of nonelim-inated harmonics of SHEPWM three-level multipulse three-phase active front end converters with low switching frequency for meeting standard IEEE-519-92," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1594–1600, 2004.

[2] D. A. Rendusara, E. Cengelci, P. N. Enjeti, V. R. Stefanovic, and J. W. Gray, "Analysis of common mode voltage-"Neutral shift" in medium voltage PWM adjustable speed drive (MV-ASD) systems," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1124–1133, 2000.

[3] J. Rodríguez, J. Pontt, P. Correa, P. Cortés, and C. Silva, "A new modulation method to reduce common-mode voltages in multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 4, pp. 834–839, 2004.

[4] J. Rodríguez, J. Pontt, R. Huerta, and P. Newman, "24-pulse active front end rectifier with low switching frequency," in *Proceedings of the 35th IEEE Annual Power Electronics Specialists Conference (PESC '04)*, pp. 3517–3523, June 2004.

[5] B. P. Schmitt and R. Sommer, "Retrofit of fixed speed induction motors with medium voltage drive converters using NPC three-level inverter high-voltage IGBT based topology," in *Proceedings of the IEEE International Symposium on Industrial Electronics Proceedings (ISIE '01)*, pp. 746–751, June 2001.

[6] F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage PWM voltage-source-inverter drive applications," *IEEE Transactions on Industry Applications*, vol. 36, no. 5, pp. 1336–1341, 2000.

[7] A. Videt, P. Le Moigne, N. Idir, P. Baudesson, and X. Cimetière, "A new carrier-based PWM providing common-mode-current reduction and DC-bus balancing for three-level inverters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3001–3011, 2007.

[8] F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters," *IEEE Transactions on Industry Applications*, vol. 38, no. 2, pp. 500–506, 2002.

[9] A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1672–1681, 2007.

[10] R. S. Kanchan, P. N. Tekwani, and K. Gopakumar, "Three-level inverter scheme with common mode voltage elimination and dc link capacitor voltage balancing for an open-end winding induction motor drive," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1676–1683, 2006.

[11] P. C. Loh, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "A reduced common mode hysteresis current regulation strategy for multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 192–200, 2004.

[12] S. Wei, N. Zargari, B. Wu, and S. Rizzo, "Comparison and mitigation of common mode voltage in power converter topologies," in *Proceedings of the 39th IEEE Industry Applications Conference (IAS '04)*, pp. 1852–1857, October 2004.

[13] H. Akagi and T. Hatada, "Voltage balancing control for a three-level diode-clamped converter in a medium-voltage transformerless hybrid active filter," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 571–579, 2009.

[14] B. P. Mcgrath and D. G. Holmes, "A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC '00)*, vol. 2, pp. 647–679, November 2000.

[15] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858–867, 2002.

[16] B. P. McGrath, D. G. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1293–1301, 2003.

[17] P. K. Chaturvedi, S. Jain, and P. Agarwal, "A simple carrier based neutral point potential regulator for 3-level diode clamped inverter," *International Journal of Power Electronics*, vol. 3, no. 1, pp. 1–25, 2011.

[18] P. K. Chaturvedi, S. Jain, and P. Agarwal, "Reduced switching loss pulse width modulation technique for three-level diode clamped inverter," *IET Power Electronics*, vol. 4, no. 4, pp. 393–399, 2011.

[19] M. E. Adabi and A. Vahedi, "Common mode voltage reduction with a modified hysteresis current control strategy," in *Proceedings of the 2nd Power Electronics, Drive Systems and Technologies Conference (PEDSTC '11)*, pp. 415–420, February 2011.

[20] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, and T. Lu, "Hybrid selective harmonic elimination PWM for common mode voltage reduction in three-level neutral point clamped inverters for variable speed induction drives," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1152–1158, 2012.

[21] P. C. Loh, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *IEEE Transactions on Industry Applications*, vol. 39, no. 5, pp. 1386–1395, 2003.