International Scholarly Research Network
ISRN Electronics
Volume 2012, Article ID 529194, 7 pages
doi:10.5402/2012/529194

Research Article

Multithreshold MOS Current Mode Logic Based Asynchronous Pipeline Circuits

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Received 21 September 2012; Accepted 31 October 2012

Academic Editors: A. Mercha and I. Shubin

Multithreshold MOS Current Mode Logic (MCML) implementation of asynchronous pipeline circuits, namely, a C-element and a double-edge triggered flip-flop is proposed. These circuits use multiple-threshold MOS transistors for reducing power consumption. The proposed circuits are implemented and simulated in PSPICE using TSMC 0.18 μm CMOS technology parameters. The performance of the proposed circuits is compared with the conventional MCML circuits. The results indicate that the proposed circuits reduce the power consumption by 21 percent in comparison to the conventional ones. To demonstrate the functionality of the proposed circuits, an asynchronous FIFO has also been implemented.

1. Introduction

Digital VLSI circuits can be broadly classified into synchronous and asynchronous circuits. A synchronous circuit employs a common clock signal to provide synchronization between all the circuit components. The synchronous circuits suffer from the problems of clock distribution and clock skew which becomes a challenge to overcome as the technology scales down. Asynchronous circuits, on the other hand, are attractive replacements to synchronous designs as they perform synchronization through handshaking between their components. Some other advantages of asynchronous circuits include high speed, low power consumption, modular design, immunity to metastable behavior, and low susceptibility to electromagnetic interference [1].

Traditionally, the asynchronous circuits were implemented by using CMOS logic style but due to the substantial dynamic power consumption at high frequencies, CMOS logic style is usually not preferred. MOS Current Mode Logic (MCML) is found to be an alternative to the CMOS asynchronous circuits in the literature [2–5]. A conventional MCML circuit consists of a differential pull-down network (PDN), a current source, and a load. The PDN implements the logic function, the current source generates the bias current I_{SS}, while the load performs the current to voltage conversion [6]. The circuit has static power consumption given as the product of the supply voltage and the bias current. The power consumption can be lowered by either reducing the bias current or the supply voltage. The reduction in bias current is generally not favored as it degrades the speed [7]. Therefore, lowering the supply voltage of the circuit is preferred. One of the techniques suggested in [8, 9] is multithreshold MOS Current Mode Logic (MT-MCML) which uses multithreshold transistors in conventional MCML circuits. In this paper, MT-MCML technique has been applied to implement low-power multithreshold MCML asynchronous pipeline circuits.

The paper first describes the architecture and the operation of MT-MCML circuits in Section 2. In the next section, a brief introduction to asynchronous pipelines is presented. Thereafter, multithreshold MCML asynchronous pipeline circuits, namely, a double-edge triggered flip-flop and a C-element are proposed in Section 4. In the subsequent Section 5, the proposed circuits are simulated in PSPICE using TSMC 0.18 μm CMOS technology parameters and their performance is compared with existing MCML circuits.

An FIFO is also implemented using the proposed circuit. Finally, the conclusions are drawn in the last section.

2. MT-MCML Circuits

MT-MCML circuits are the modified form of the conventional MCML circuits. They use multithreshold CMOS technology for the realization of the logic functions [8, 9]. The circuit of an MT-MCML AND/NAND gate is shown in Figure 1. It consists of two levels of source-coupled transistor pairs (M2-M5) to implement the logic function and a constant current source M1 to generate bias current I_{SS}. The transistors in the upper level (M4, M5) have lower threshold voltage than the transistors in the lower level (M2, M3). The minimum supply voltage for the circuit is defined as the lowest voltage at which all the transistors in the two levels and the current source operate in the saturation region [8] and is computed as

$$V_{MIN} = 3\ V_{BIAS} - \ 3V_{T1} \ + \ V_{TU}, \tag{1}$$

where V_{T1} and V_{TU} are the threshold voltages of the transistor M1 and the transistors in the upper level (M4, M5), respectively.

As an example, an MT-MCML AND/NAND gate with $V_{BIAS} = 800$ mV, $V_{T1} = 500$ mV, and $V_{TU} = 200$ mV results in a value of $V_{MIN} = 1.1$ V in comparison to the conventional gate which results in $V_{MIN} = 1.4$ V for $V_{T1} = V_{TU} = 500$ mV. Thus, MT-MCML circuits can be used in low-power applications as they can operate at low supply voltage than the conventional one.

3. Asynchronous Pipeline

In asynchronous pipelines, data is communicated between the sender and the receiver modules through a handshaking protocol. A very common protocol is the two-phase bundled-data handshaking protocol [10, 11]. Bundled-data channels connect the sender and the receiver through a data bus consisting of separate requests (Req) and acknowledge signals (Ack) and data signals (Data). The sender initiates the data transfer by placing Data on the bus and raises the Req signal, and the receiver then absorbs the data and acknowledges it by raising the Ack signal. Then, the two signals are reset to zero in the same order.

The block diagram of a typical two-phase bundled-data asynchronous pipeline is shown in Figure 2. It comprise of four-stages wherein each stage consists of a functional unit and a control unit. The functional unit has a combinational stage for computing the result of each stage and a matched delay element inserted in the request line. The control unit employs a double-edge triggered flip-flop (DETFF) and a C-element to control the communication between the successive stages.

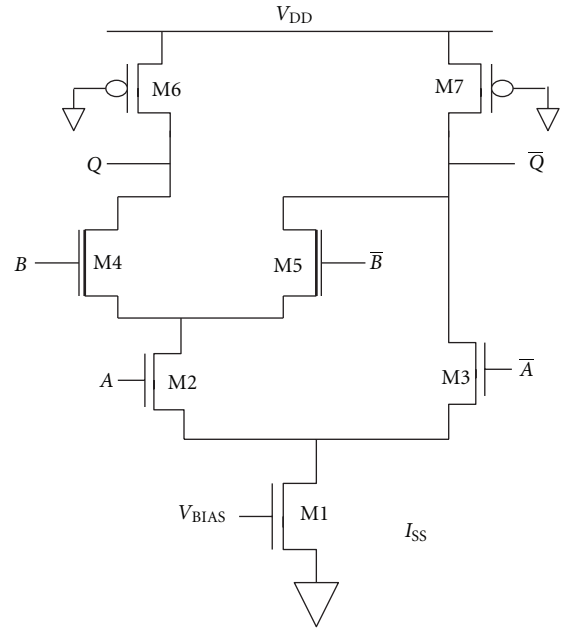

Figure 1: MT-MCML AND/NAND gate.

4. MT-MCML Control Unit

The control unit in asynchronous pipelines consists of two elements, namely, a double-edge triggered flip-flop and a C-element. This section proposes the low-power MT-MCML circuits for both the elements.

4.1. MT-MCML DETFF. A DETFF is an essential element to store the new data produced by the functional unit till the time the successor stage is ready to receive it. It samples the data at the falling and the rising edges of the local clock pulses generated by the C-element.

A block diagram of a DETFF consisting of two opposite level sensitive latches and a multiplexer is shown in Figure 3. When CLK is high, latch L1 becomes transparent and the data stored in the latch L2 is obtained as the output. Similarly, when CLK is low, latch L2 becomes transparent and the data stored in the latch L1 is obtained as the output of the flip-flop. The circuit of the proposed MT-MCML DETFF is shown in Figure 4. It consists of two MT-MCML latches L1, L2 and MCML multiplexer (MUX) with a common source-coupled transistor pair for differential clock input (CLK). The advantage of using common clock source-coupled transistor is the reduction in the routing complexity and the overall area. The transistors in the upper level of latches and the multiplexer (M4-M15) have low threshold voltages values and have been highlighted in the figure.

4.2. MT-MCML C-Element. A C-element is a fundamental component of asynchronous pipelines. It is a state holding element wherein if both inputs are same, that is, low (high), the circuit produces the output which is equal to the input value, that is, low (high), respectively, otherwise the output

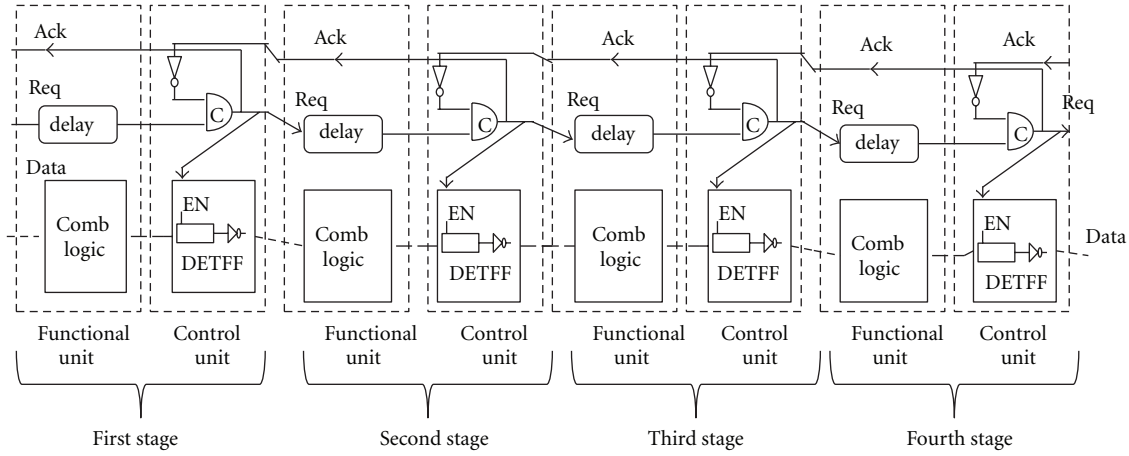

Figure 2: Block diagram of two-phase asynchronous pipeline.

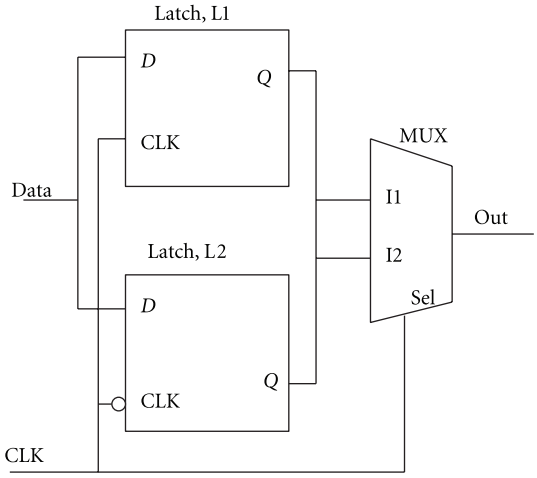

Figure 3: Block diagram of a DETFF.

remains at the previous state value. A state diagram is given in Figure 5 which can be expressed by a Boolean function:

$$C = \left[\hat{C} \cdot (A + B)\right] + (A \cdot B), \tag{2}$$

where A, B are the inputs and $\hat{C}$ is the previous state of the output.

The circuit of the proposed MT-MCML C-element is shown in Figure 6. In circuit, the two stacked transistors (M2, M8) form an AND structure whereas the parallel connection of transistors (M3, M4) performs the OR operation. The cross-coupled transistor pair (M9, M10) forms the latch structure. The transistors in the upper level of the C-element (M8-M11) have low threshold voltages values and have been highlighted in the figure. When both the inputs (A, B) have the same value then the bias current either flows through the two right most branches or the left most branches. This, however, makes the output (C) of the circuit same as the input value. Conversely, when both the inputs (A, B) have different values, the output stores the previous value by making the bias current flow in the latch structure branches only.

5. Simulation Results

This section first presents the simulation results for the proposed control unit elements, namely, DETFF and C-element. Thereafter, the performance of the proposed circuits is compared with the conventional MCML control unit elements. Lastly, the simulation results for an asynchronous FIFO are presented. All the simulations are performed by using TSMC 0.18 μm CMOS technology parameters and load capacitance of 10 fF. The channel length of the transistors is taken as 0.18 μm uniformly. The value of the supply voltage for the MT-MCML and conventional MCML circuits is 1.1 V and 1.4 V, respectively.

5.1. Proposed Control Unit Elements. The proposed MT-MCML control unit elements are implemented with an output voltage swing of 400 mV and a bias current (I_{SS}) of 30 μA and 90 μA for C-element and DETFF, respectively. The bias current of DETFF is taken to be three times the value of bias current in C-element as in DETFF there is a common source-coupled transistor pair that drives the two D-latches and a multiplexer. The aspect ratio of the transistors in the PDN of both the elements is 3 μm/0.18 μm, whereas the aspect ratio for load transistors is 0.46 μm/0.18 μm. The simulation waveforms are shown in Figure 7. In Figure 7(a), it can be observed that in DETFF whenever CLK is low, the previous value stored in L1 is obtained as the output of the DETFF. Similarly, when CLK is high, the previous value stored in L2 is obtained as the output. The simulation waveforms for C-element shown in Figure 7(b) depict that whenever both the inputs (A and B) have the same value an output which is equal to the current vales of the inputs is obtained. Further for different values of the inputs (A and B), the output remains in the previous state value.

The impact of parameter variation on power consumption of the proposed MT-MCML control unit elements is studied at different design corners. It is found that the power consumption of the proposed DETFF varies by a factor of 1.87 between the best and the worst cases. For the proposed

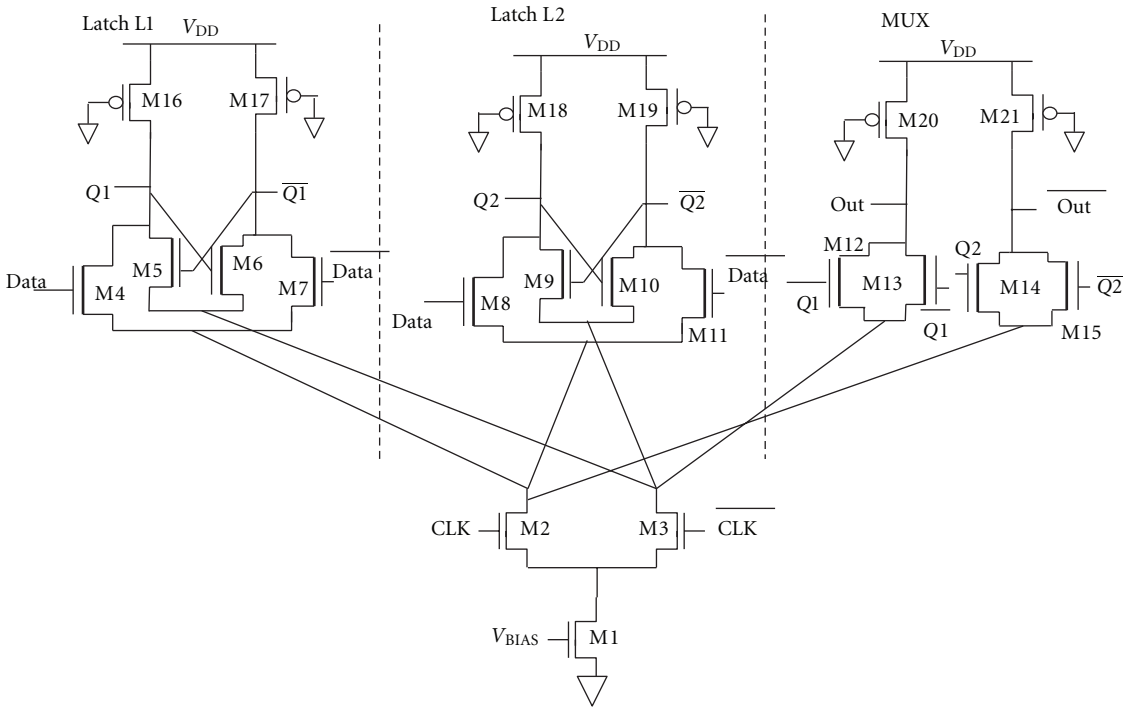

Figure 4: Proposed MT-MCML DETFF.

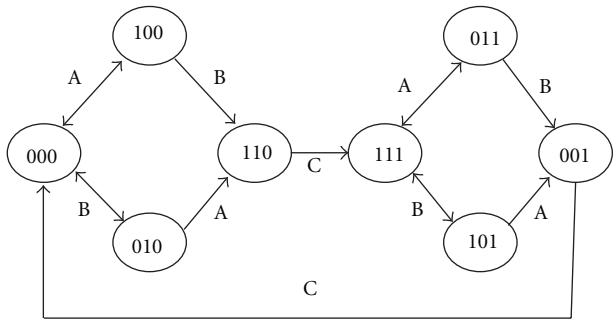

Figure 5: State diagram of the C-element.

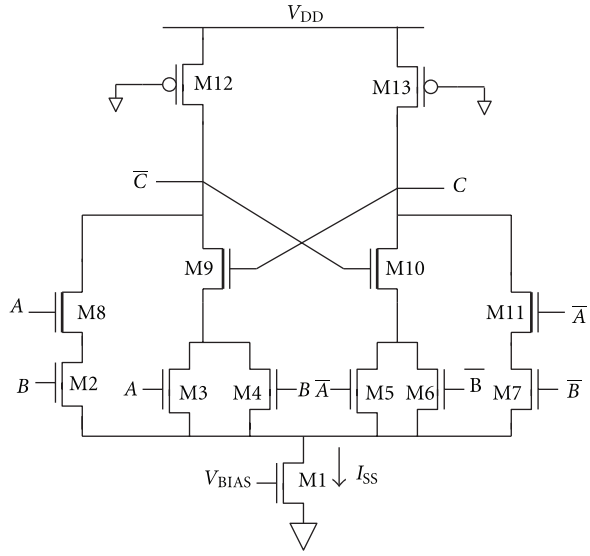

Figure 6: Proposed MT-MCML C-Element.

C-elements, the power consumption varies by a factor of 1.4 between the best and the worst cases.

5.2. Performance Comparison. The performance of the proposed MT-MCML and the conventional MCML control unit elements has been compared using simulation test benches [3] which are redrawn in Figure 8. The simulation results are listed in Tables 1 and 2. The power result for MCML circuits includes static power due to the presence of the constant current source. The result shows that the proposed MT-MCML circuits reduce power consumption by 21 percent due to the operation at low supply voltage through the use of multiple-threshold voltage transistors. Further, the propagation delay of the proposed MT-MCML control unit elements is slightly higher than the conventional MCML elements due to the increase in transistor sizes in the proposed elements [8]. Thus, the power-delay product (PDP) values for the proposed are reduced accordingly. Therefore, the use of MT-MCML circuits can lead to the design of power-efficient asynchronous pipelines.

5.3. An Application. An asynchronous MT-MCML FIFO is implemented as an application of the proposed control unit elements. The block diagram of a 4-stage FIFO is shown in Figure 9. The handshaking signals shown as Req(in) and Ack(out) communicate the data, Data(in) between sender and the first stage. At the receiver side, the signals Req(out) and Ack(in) are used to synchronize the output

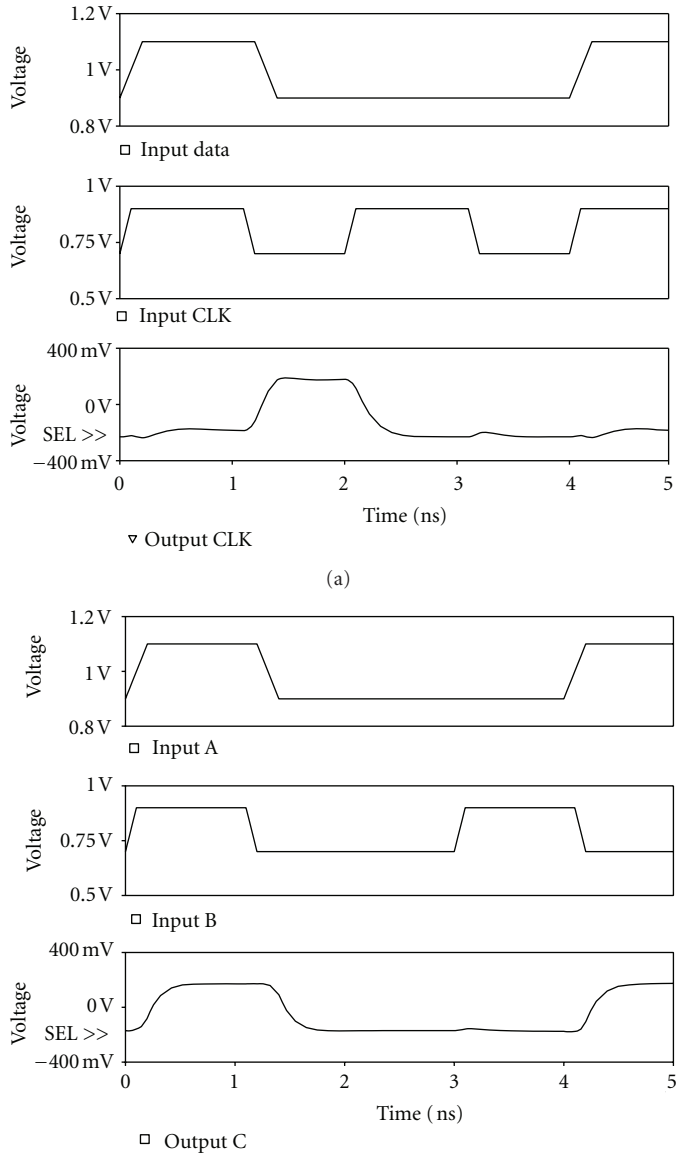

Figure 7: Simulation waveforms of the proposed MT-MCML (a) DETFF and (b) C-Element.

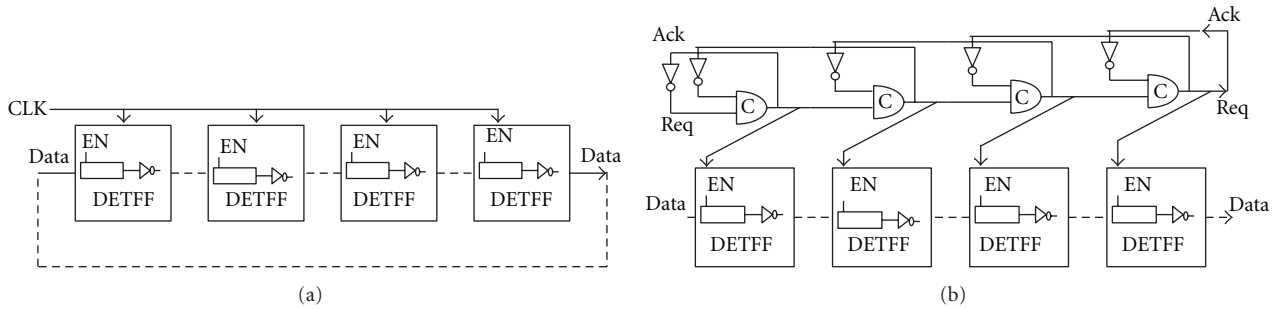

Figure 8: Simulation test bench [3] (a) DETFF and (b) C-element.

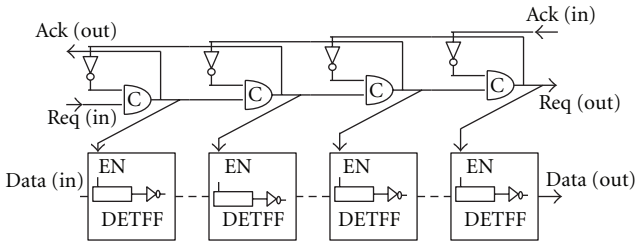

Figure 9: Block diagram of 4-stage asynchronous FIFO.

Table 1: Summary of simulated performance for DETFF.

Parameter	Type of DETFF	
	Conventional MCML	Proposed MCML
Power (μW)	141	111
Propagation delay (ps)	1230	1240
PDP (fJ)	173	138

Table 2: Summary of simulated performance for C-element.

Parameter	Type of C-element	
	Conventional MCML	Proposed MCML
Power (μW)	44	35
Propagation delay (ps)	239	241
PDP (fJ)	11	8

data, Data(out) with the receiver and the last stage. Initially, the input data Data(in) is loaded in the first stage of the FIFO, and the Req(in) is asserted to low to start the data transfer. This results in a transition at the output of a C-element such that the data is stored in the DETFF of the first stage. At the same time an acknowledge signal Ack(out) is given to the sender. The stored data then flows through the different stages in the FIFO. Then, a request signal Req(out) is generated by the last stage to the receiver to enable the receiver to accept the data. This is followed by an acknowledge signal, Ack(in), from the destination to the last stage. The waveforms obtained through the simulation of a four-stage asynchronous FIFO are shown in Figure 10. The first three waveforms correspond to the input data Data(in), request signal (Req(in)), and acknowledge signal (Ack(out)) at the sender section. The last three graphs are the acknowledge signal Ack(in), data Data(out), and request signal Req(out). It can be found that the asynchronous MT-MCML FIFO outputs the sampled data correctly.

6. Conclusions

This paper proposes low-power Multithreshold MOS Current Mode Logic (MT-MCML) asynchronous pipeline circuits. The proposed circuits involve the use of multiple-threshold CMOS technology which helps in reducing the power consumption. The proposed circuits have been simulated using 0.18 μm CMOS technology parameters, and their performance has been compared with the conventional MCML circuits. A performance comparison indicates that

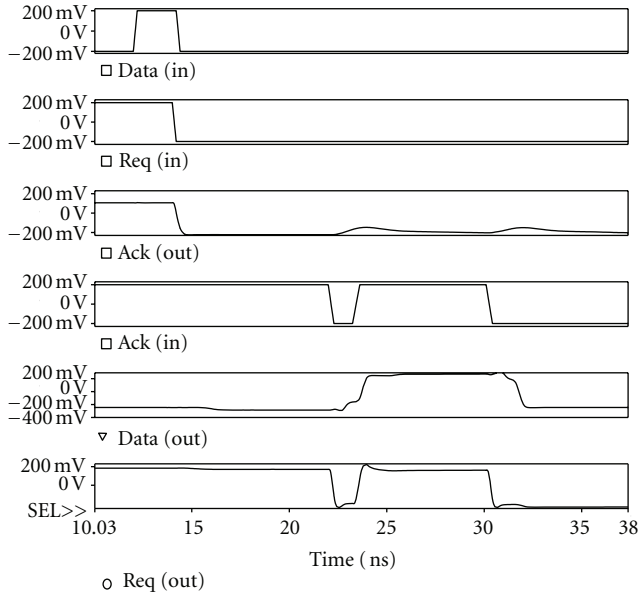

Figure 10: Transient response of the 4-stage multithreshold MCML asynchronous FIFO circuit.

the proposed circuits are power efficient than the conventional ones. An asynchronous FIFO implemented as an application confirms to the functionality of the proposed circuits.

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