International Scholarly Research Network
ISRN Nanotechnology
Volume 2012, Article ID 689023, 35 pages
doi:10.5402/2012/689023

Review Article

Advanced CMOS Gate Stack: Present Research Progress

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Received 6 September 2011; Accepted 29 September 2011

Academic Editors: M. Cazzanelli and K. Yong

The decreasing sizes in complementary metal oxide semiconductor (CMOS) transistor technology require the replacement of SiO_2 with gate dielectrics that have a high dielectric constant (high-k). When the SiO_2 gate thickness is reduced below 1.4 nm, electron tunneling effects and high leakage currents occur which present serious obstacles for device reliability. In recent years, various alternative gate dielectrics have been researched. Following the introduction of HfO_2 into the 45 nm process by Intel in 2007, the screening and selection of high-k gate stacks, understanding their properties, and their integration into CMOS technology have been a very active research area. This paper reviews the progress and efforts made in the recent years for high-k dielectrics, which can be potentially integrated into 22 nm (and beyond) technology nodes. Our work includes deposition techniques, physical characterization methods at the atomic scale, and device reliability as the focus. For most of the materials discussed here, structural and physical properties, dielectric relaxation issues, and projections towards future applications are also discussed.

1. Introduction

With the advance of metal oxide semiconductor technology, Si-based semiconductors, with SiO_2 as an outstanding dielectric, have been dominating microelectronic industry for decades. In the current version of the International Technology Roadmap for Semiconductors (ITRSs), the scaling of the metal-oxide-semiconductor field-effect transistor (MOSFET) is projected to the year 2016 when the channel length should be 9 nm as shown in Figure 1 [1]. Recently, some semiconductor companies have moved to the leading-edge of the 32 nm technology node and successfully realized advanced product development. Presently companies are continuing research and development the 22 nm and beyond complementary metal oxide semiconductor (CMOS) technology [2]. MOSFETs have been scaled down, and the physical thickness of SiO_2 dielectrics becomes as thin as 1.4 nm (just a few atomic layers) [3]. Oxide materials with large dielectric constants (so-called high-k dielectrics) have attracted much attention due to their potential use as gate dielectrics in MOSFETs. When the channel length becomes of the same order of magnitude as the depletion-layer widths of the source and drain, a MOSFET device is considered to be short and the so-called short-channel effects arise. To offset short channel effects, the thickness of the gate oxide must be reduced. This causes a reduction in the on/off current ratios [4]. Moreover, the reduction of oxide thicknesses results in increased gate leakage current, which is a formidable problem, particularly for large density circuits [5]. In the nanoscale Si-based CMOS electronics, the interfaces present throughout a high-k gate stack (schematically shown in Figure 2) are typically less than 1 nm in thickness, serving as a transition between the atoms associated with the materials in the gate electrode, the gate dielectric, and the Si channel [6]. The benefits of high-k dielectrics can be clearly understood from (1), which represents an equivalent oxide thickness (EOT) t_{eq}, a quantity used to compare performance of high-k dielectric MOS devices with performance of SiO_2-based MOS devices. The EOT is the thickness of SiO_2 gate oxide needed to obtain the same gate capacitance as that obtained with thicker high-k dielectrics:

$$t_{eq} = t_{\text{high-}k}\frac{\varepsilon_{SiO_2}}{\varepsilon_{\text{high-}k}} = t_{\text{high-}k}\frac{3.9}{\varepsilon_{\text{high-}k}}. \quad (1)$$

In the past ten years, significant progress has been made on the screening and selection of high-k gate dielectrics,

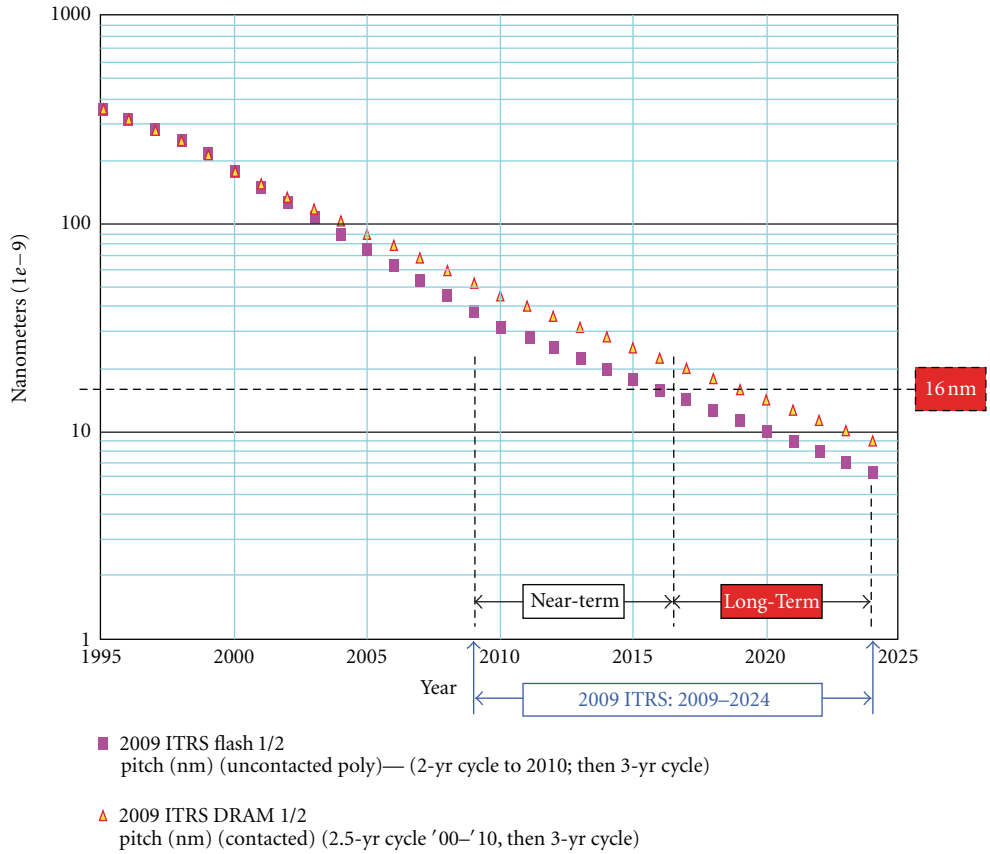

Figure 1: ITRS prediction [1]. In the current version of the International Technology Roadmap for Semiconductors (ITRS), the scaling of the metal-oxide-semiconductor field-effect transistor (MOSFET) is projected for the y-axis by the nanometer unit, which is also represented by technology node or process.

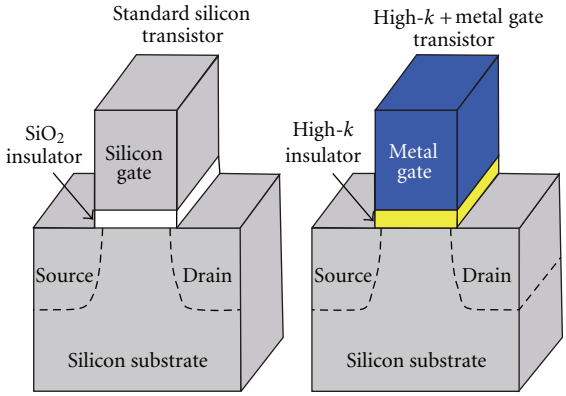

Figure 2: Schematic illustration of important regions in a CMOS FET gate stack [16].

understanding their physical properties, and their integration into CMOS technology. Now it has been recognized that the family of hafnium oxide-based materials (e.g., HfO_2, $HfSi_xO_y$, and $HfSi_xO_yN_z$) emerges as a leading candidate to replace SiO_2 gate dielectrics in advanced CMOS applications [7, 8]. There are a number of high-k dielectrics that have been and/or are actively being pursued for replacing SiO_2. Among them are gadolinium oxide Gd_2O_3, erbium oxide Er_2O_3, neodymium oxide Nd_2O_3, praseodymium oxide Pr_2O_3, cerium oxide CeO_2, cerium zirconate $CeZrO_4$, aluminum oxide Al_2O_3, lanthanum aluminum oxide $LaAlO_3$, lanthanum oxide La_2O_3, yttrium oxide Y_2O_3, tantalum pentoxide Ta_2O_5, titanium dioxide TiO_2, zirconium dioxide ZrO_2, zirconium silicate $ZrSiO_4$, hafnium oxide HfO_2, HfO_2-based oxides $HfSiO_2$, $HfSCO_x$, hafnium silicate $HfSi_xO_y$, strontium titanate $SrTiO_3$, $LaLuO_3$, and rare-earth scandates $LaScO_3$, $GdScO_3$, $DyScO_3$, and $SmScO_3$ [9–13]. Among these variants, HfO_2 and HfO_2-based materials are considered the most promising candidates combining high dielectric permittivity and thermal stability with low leakage current due to a reasonably high barrier height that limits electron tunneling [14–16]. The rare earth oxides, various lanthanides, and their silicates are also be counted as potentially promising candidates, despite the fact that in some cases the permittivity increase is only moderate [17]. Rare earth scandates have also been introduced as high-k candidates; for example, $GdScO_3$ has been reported to have permittivity value of about 20.0, which is considerably higher than those of the constituent oxides, Gd_2O_3 and Sc_2O_3 [18–20]. The detailed feature list for high-k materials is presented in Table 1.

In this paper, we review the progress made in oxides recently (within the latest five years) with an emphasis on

Table 1: High-k materials feature list.

Oxide	Dielectric constant	Features (including deposition, physical, or electrical properties)
HfO_2	17-18	Deposited by liquid injection atomic layer deposition (LI-ALD) and PDA in nitrogen (N_2) ambient
$CeHfO_2$	32	Low hysteresis voltages and negligible flat band voltage shifts
Er-HfO_2	28–30	Dopant elements have been demonstrated to stabilize the cubic fluorite and tetragonal phases of HfO_2
HfTiON	18.9	Improved C-V characteristics and reduced leakage current have been achieved from HfTiON gate dielectric MOS capacitor
$HfSiO_2$	17.7	Exhibit excellent C-V characteristics with an EOT of 1.3 nm which are sufficient for implementing high mobility MOSFETs using compressively strained SiGe channels in future CMOS technology
TiO_2	55	Well-behaved C-V curves observed but high leakage current
HfTaON/AlON	20	Exhibits low interface state to oxide-charge densities, low gate leakage, small CET about 1.1 nm; incorporation of N into both the interlayer and high- k dielectric further improve the device reliability under high field stress through the formation of strong N-related bonds
$LaZrO_2$	11–14	Show good dielectric properties with low hysteresis voltages and negligible flat band voltage shifts
Ge-doped ZrO_2	37.7	Very high-k value at low deposition temperatures and with excellent thermal stability
La-ZrO_2	40	La-doped ZrO_2 thin films grown by O_3-based atomic layer deposition directly on Ge; Ge is widely considered due to its higher carrier motilities
$PrAlO_x$	14	Combine the advantages of the high permittivity of the lanthanide oxide with the chemical and thermal stability of Al_2O_3
Gd_2O_3	10.6	Exhibit the best electrical characteristics, including the lowest gate leakage current, the lowest-noise spectra density, and the high-power performance
$GdScO_3$	23	Small hysteresis and low leakage current densities

high-k dielectric materials deposition techniques, structure characterization, electrical properties, and present existing challenges. Some attention is also paid to dielectric relaxation phenomenon. The article is organized as follows. Section 2 is devoted to high-k dielectric materials deposition techniques. Brief history and basic properties of structure characterization as well as their application and thin-film growth methods are introduced in Section 3. Section 4 deals with electrical properties, including reliability issues, which is followed by a discussion of dielectric relaxation phenomenon in Section 5. Section 6 highlights some important issues that need to be addressed in the future.

2. High-k Films Deposition

Thin-film deposition is the art of applying a thin film to a surface and includes any technique for depositing a thin film of material onto a substrate or onto other previously deposited layers. Deposition techniques fall into two broad categories, depending on whether the process is primarily chemical or physical. Chemical deposition is further categorized by the phase of the precursor. Plating relies on liquid precursors, often a solution of water with a salt of the metal to be deposited. Chemical solution deposition (CSD) uses a liquid precursor, usually a solution of organometallic powders dissolved in an organic solvent. Chemical vapor deposition (CVD) generally uses a gas-phase precursor, often a halide or hydride of the element to be deposited. Physical deposition uses mechanical, electromechanical, or thermodynamic means to produce a thin film of solid. Examples of physical deposition include thermal evaporation, sputtering, pulsed laser deposition, catholic arc deposition, and electrohydrodynamic deposition. Some methods fall outside these two categories, relying on a mixture of chemical and physical means including reactive sputtering, molecular beam epitaxy, and topotaxy. The properties of the thin films so produced have been reported to be closely dependent on the growth method. Studies to gain insight into any correlation among the properties of the films, the interfacial layers, and growth condition have been undertaken.

2.1. Atomic Layer Deposition. Atomic layer deposition, (ALD), a variant of CVD, is a popular technique used to deposit ultrathin metal-oxide layers with excellent electrical characteristics and conformal structure because of the layer-by-layer nature of the deposition kinetics [19]. The growth mechanism of ALD can be simply expressed as the surface exchange reactions between the chemisorbed metal-containing precursor fragments and the other precursor, which in the case of oxide deposition introduces the oxygen. The ALD growth mechanism can be described as a four-step process, where a precursor gas is initially introduced followed by an inert gas to remove unreacted precursor from the reactor chamber. A second precursor is introduced,

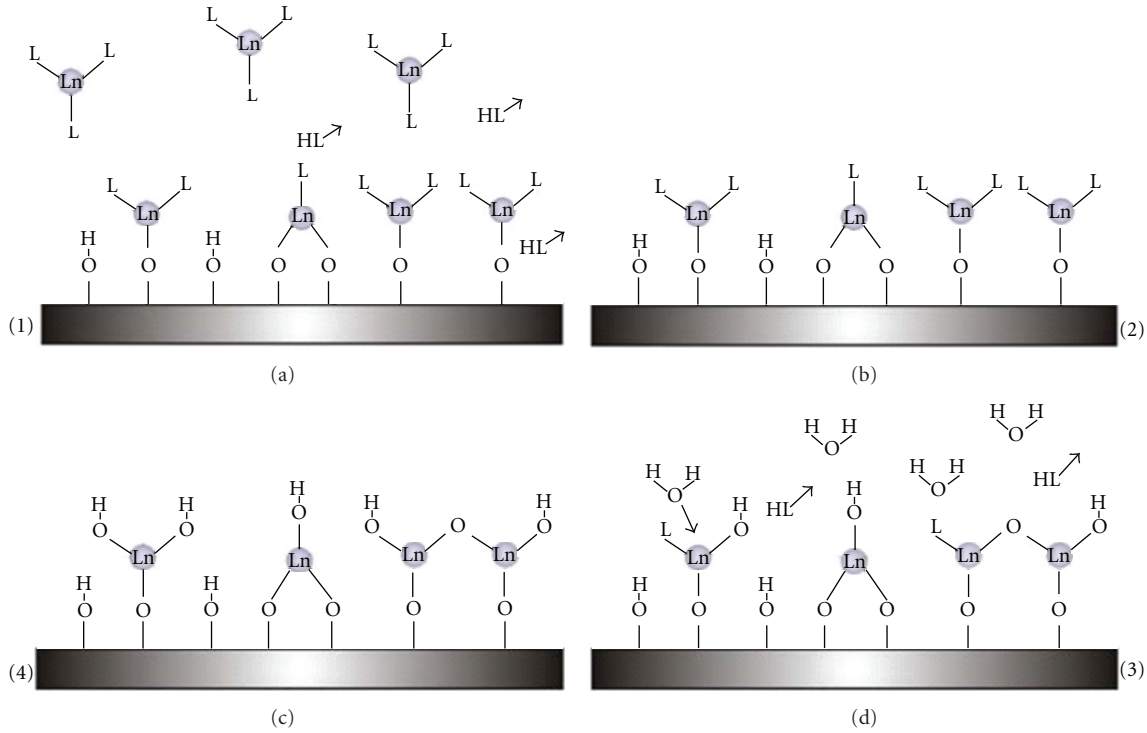

Figure 3: Schematic illustration of an ALD cycle of Ln_2O_3 process where a hypothetical LnL_3 and H_2O precursors are alternatively pulsed (steps 1 and 3) and separated by inert gas purging (steps 2 and 4) [12].

which completes the layer, and this is followed by inert gas to remove unreacted precursor. In self-limiting ALD the growth surface becomes saturated with the precursor forming a new species that is unreactive with the precursor, so that the deposition automatically self-limits at one or two monolayers. Therefore, the growth rate in the system is surface-controlled. Unfortunately, many organometallic precursors commonly used for oxide growth do not exhibit a distinct self-limiting ALD window. Thus, the deposition rate in these processes is dependent on the temperature. Additionally some precursors would deposit films with a relatively high concentration of residual impurities originating from the ligands, which is unfavorable for gate dielectrics. Thus, the choice of precursors providing low contamination and ability to self-limit is a critical issue for the ALD growth of high-quality oxide films. ALD can be used to deposit several types of thin films, including various oxides (e.g., Al_2O_3, TiO_2, SnO_2, ZnO, HfO_2), metal nitrides (e.g., TiN, TaN, WN, NbN), metals (e.g., Ru, Ir, Pt), and metal sulfides (e.g., ZnS). Schematic illustration of an ALD cycle of Ln_2O_3 process is shown as an example in Figure 3.

2.2. Pulsed-Laser Deposition. Pulsed-laser deposition, PLD, is also applied to high-k dielectric film growth owing to its advantages such as relative simplicity, large deposition rate, and low growth temperature [19]. PLD is applicable to almost any material, in particular to compounds that are difficult or impossible to produce in thin-film form by other techniques. The detailed mechanisms of PLD are very complex including the ablation process of the target material

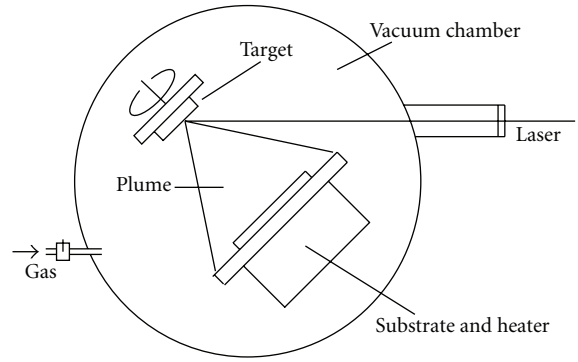

Figure 4: Typical equipment of pulsed laser deposition [14].

by the laser irradiation, the development of a plasma plume with high energetic ions, electrons as well as neutrals, and the crystalline growth of the film itself on the heated substrate. Typical equipment of pulsed laser deposition is shown in Figure 4. The process of PLD can generally be divided into four stages: (1) laser ablation of the target material and creation of a plasma, (2) dynamic expansion of plasma, (3) deposition of the ablation material on the substrate, and (4) Nucleation and growth of the film on the substrate surface. Each of these steps is crucial for the crystallinity, uniformity, and stoichiometry of the resulting film. Deposited HfO_2 and PrO_x films on Si substrates by the PLD method compared their morphology, chemical composition, and crystalline structure, in particular that at the interface [12]. Both

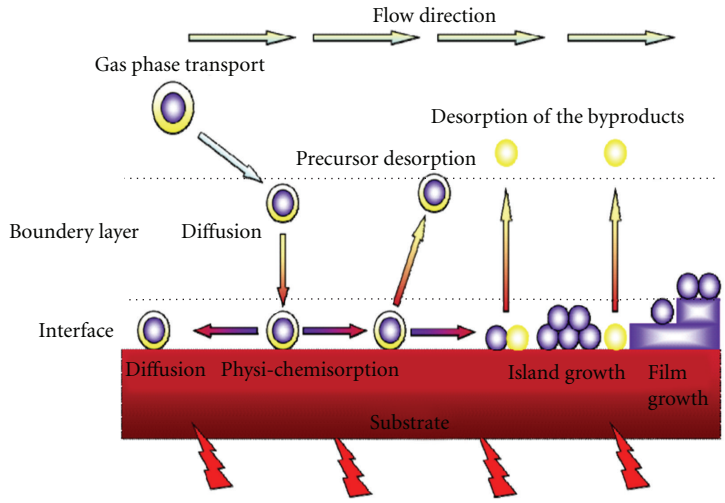

Figure 5: Scheme of precursor transport and reaction processes in MOCVD [12].

HfO_2 and PrO_x films showed grainy structure, the size of which increased with growth temperature. The PrO_x films were found to be much more uniform than HfO_2. The interfaces are significantly different for both materials in that a silicate formation is observed for PrO_x, whereas and a rich abundance of SiO_2 and silicides is found for HfO_2. In addition to PrO_x, several other lanthanoid oxide thin films such as $SmScO_3$, Sm_2O_3, Tb_4O_7, Er_2O_3, and Yb_2O_3 have also been attempted with this method on Si wafers.

2.3. Metal-Organic Chemical Vapor Deposition. Metal-organic chemical vapor deposition, MOCVD, is widely used technique of growth of the thin films [17]. Recently, as high-*k* dielectric materials came under extensive investigation, MOCVD emerged as a viable candidate for high-*k* film deposition on Si. Some oxide precursors used for high-*k* materials have low vapor pressure and low thermal stability, both of which are detrimental to the growth. This problem can be solved by applying liquid injection of precursors dissolved in a solvent. This takes place not in a vacuum, but from the gas phase at moderate pressures (2 to 100 kPa). As such, this technique is preferred for the formation of devices incorporating thermodynamically metastable alloys, and it has become a major process in the manufacture of optoelectronics. Even so, there remain some requirements for the precursors to meet: the precursors should be soluble and stable but not reactive to each other in the same liquid solution. Scheme of precursor transport and reaction processes in MOCVD is demonstrated in Figure 5.

2.4. Others. Molecular beam epitaxy, MBE, is a powerful and sophisticated technique due to its precise control over the growth parameters at the atomic scale [19]. Despite this strength, however, MBE is not very popular for high-*k* dielectric deposition. In order to meet the high-*k* dielectric growth requirements, the MBE system must be modified due to the corrosive oxygen environment, since oxygen reaction with the source materials in the MBE cell creates difficulties. Against this background, various high dielectric oxides have been successfully grown by MBE. Gd_2O_3 has been grown on nearly lattice matched Si substrate by MBE. In solid-source MBE, ultrapure elements such as gallium and arsenic are heated in separate quasi-Knudsen effusion cells until they begin to slowly sublimate. The gaseous elements then condense on the wafer, where they may react with each other. In the example of gallium and arsenic, single-crystal gallium arsenide is formed. The term "beam" means that evaporated atoms do not interact with each other or vacuum chamber gases until they reach the wafer, due to the long mean free paths of the atoms.

Sputter deposition, including RF sputtering and Ion-beam sputtering, is a physical vapor deposition (PVD) method of depositing thin films by ejecting, material from a "target," that is source, which then deposits onto a "substrate," such as a silicon wafer [19]. The plasma is initiated between the cathode and the anode at pressures in the m Torr range by the application of a high voltage that can be either DC or RF. The plasma is sustained by the ionization caused by secondary electrons emitted from the cathode due to ion bombardment which are accelerated into the plasma across the cathode sheath. What differentiates a magnetron cathode from a conventional diode cathode is the presence of a magnetic field. The magnetic field in the magnetron is oriented parallel to the cathode surface. The local polarity of magnetic field is oriented such that E $\times$ B drift of the emitted secondary electrons forms a closed loop. Due to the increased confinement of the secondary electrons in this E $\times$ B drift loop compared to a DC diode device, the plasma density will be much higher, often by an order of magnitude or more, than a conventional DC diode system. Magnetron sputtering is a low-cost and easy control method for film growth, especially suitable for large-scale film deposition. Charge build-up on insulating targets can be avoided with the use of RF sputtering where the sign of the anode-cathode bias is varied at a high rate. RF sputtering works well to produce highly insulating oxide films but only with the added expense of RF power supplies and impedance matching networks. RF magnetron sputtering also can be used to

Table 2: MOCVD, ALD, and PLD feature list.

Deposition technique	MOCVD
Main advantages	MOCVD is not restricted to a line-of-sight deposition which is a general characteristic of sputtering, evaporation, and other PVD processed. Deep trenches, holes, and other complex 3D configurations can usually be coated with relative ease. The deposition rate is high and thick coatings can be readily obtained. MOCVD equipment does not normally require ultrahigh vacuum and can be adapted to many process variations, which makes MOCVD generally more competitive and, in some cases, more economical than PVD.
Main disadvantages	A major issue is the requirement of having chemical precursors (the starting materials) with suitable thermal and chemical properties. This what makes precursor development so challenging and important. There is continuous need to develop novel concepts for the synthesis of improved chemical precursors with tailored physicochemical properties.
Deposition technique	ALD
Main advantages	The main advantages of ALD over other gas-phase deposition techniques include precise film thickness control by simply changing the number of deposition cycles without controlling the dose of the precursor. Similarly, uniform doping is easy to accomplish by replacing, at a desired interval, the growth cycle by a doping cycle. Another advantage and inherent feature of ALD originates from its surface-controlled nature which allows substrates of various sizes and geometries to be conformably coated.
Main disadvantages	A main disadvantage of ALD in certain applications is the fact that it is a relatively slow technique when thicker films, measuring hundreds of nanometers and more, need to be deposited. In addition, the ALD process is entirely dictated by precursor chemistry, which makes the availability of suitable chemical precursors the most critical issue for the successful development of new ALD process. This is especially true for the ALD of rare earth oxides where the very limited number of true ALD processes is mainly due to the lack of suitable precursors. There is a clear demand for novel precursor concepts, which are able to meet the demands of semiconductor industry.
Deposition technique	PLD
Main advantages	One of the major advantages is that the stoichiometry of the target can be retained in the deposition films. This is because the high rate of ablation causes all elements or compounds evaporation at the same time. Deposition of multilayers which involves sequential ablation of multiple targets with a laser beam in a relatively straightforward operation is another key feature of the technique. To achieve this, the deposited material can be easily changed using a rotational multitarget holder. The ability to easily change the deposited material in situ is a unique advantage to PLD which has enabled the development of new materials, including metastable phases and artificial super lattices, as well as the fabrication of novel device structure. Compared with other processes such as chemical-vapor deposition or ion implantation, PLD allows for easy handling, since the laser source is placed outside of reaction chamber. Furthermore, the emission of energetic ions during laser-target-vapor interaction has an important influence on the layer formation; that is, it enables growth of adherent and epitaxial films at lower substrate temperature than other methods.
Main disadvantages	There are some drawbacks about PLD naturally. One of the major problems is the splashing or the particulates deposition on the film. Two main cases for particle formation during laser evaporation are the breakaway of surface defects under thermal shock and splashing of liquid material due to superheating of subsurface layers. Another problem is the lack of uniformity over a large area of the plume, due to the narrow angular distribution of the plume that comes out from the target surface.

sputter electrically insulating materials besides metals and alloys.

In general, each deposition technique has been pursued or developed because it has unique advantage over others. However, each process technology has certain limitations. In order to optimize the desired film characteristics, a good understanding of the advantages and restrictions applicable to each technology is necessary. A table of most popular techniques, PLD, ALD, and MOCVD is concluded (Table 2) and the feature of process methods for thin film deposition is shortly discussed [12, 14].

3. Material and Structure Properties of High-*k* Films

Replacing the silicon dioxide gate dielectric with another material adds complexity to the manufacturing process. Silicon dioxide can be formed by oxidizing the underlying

silicon, ensuring a uniform, conformal oxide and high interface quality. As a consequence, development efforts have focused on finding a material with a requisitely high dielectric constant that can be easily integrated into a manufacturing process. Up to date, a variety of techniques are employed to characterize high-k gate dielectrics. High-resolution microscopic and spectroscopic methods are central in facilitating high-k gate dielectrics to be integrated in CMOS devices and to continue scaling. Besides the traditional and advanced electrical characterization tools, a range of sophisticated novel physical and chemical methods are also utilized to examine the composition, structure, bonding, and electronic properties of next generation CMOS gate stacks. Here, several high-resolution characterized methods by using electrons, ions, and photons, to characterize the film composition and interfacial structures at atomic-scale, are briefly introduced.

3.1. Material and Structure Characterization Techniques. X-ray diffraction (XRD) is a versatile, nondestructive technique that reveals detailed information about the crystallographic structure of natural and manufactured materials [9, 11]. X-rays are electromagnetic radiation with typical photon energies in the range of 100 eV–100 keV. For diffraction applications, only short wavelength X-rays (hard X-rays) in the range of a few angstroms to 0.1 angstrom (1 keV–120 keV) are used. Because the wavelength of X-rays is comparable to the size of atoms, they are ideally suited for probing the structural arrangement of atoms and molecules in a wide range of materials. The energetic X-rays can penetrate deep into the materials and provide information about the bulk structure. Generally speaking thin film diffraction refers not to a specific technique but rather to a collection of XRD techniques used to characterize thin film samples grown on substrates. These materials have important technological applications in microelectronic and optoelectronic devices, where high-quality epitaxial films are critical for device performance. Thin film diffraction methods are used as important process development and control tools, as hard X-rays can penetrate through the epitaxial layers and measure the properties of both the film and the substrate. There are several special considerations for using XRD to characterize thin film samples. First, reflection geometry is used for these measurements as the substrates are generally too thick for transmission. Second, high angular resolution is required because the peaks from semiconductor materials are sharp due to very low defect densities in the material. Consequently, multiple bounce crystal monochromators are used to provide a highly collimated X-ray beam for these measurements.

Medium energy ion scattering (MEIS) is a refinement of the more common technique of Rutherford back scattering spectrometry (RBS), but with enhanced depth and angle resolution [12, 13]. Continued downwards scaling of transistors suggests that soon we will need to develop dielectrics that are only a few atomic layers thick. Characterizing these structures is a major challenge. MEIS is a technique that allows the study of film composition with subnanometer depth resolution. Since MEIS uses the same physics as RBS, it is easy to interpret. But because it uses lower-energy ions and an electrostatic analyser and detector, the depth resolution is greatly improved. In a typical MEIS experiment a collimated beam of monoenergetic (typically 100 keV) light ions (H^+ or He^+) impinges onto a target along a known direction. The energy and angle of the scattered ions are analyzed simultaneously and allow MEIS to measure atomic mass, depth, and surface structure. MEIS has been used to look at unusual dielectrics, like ZrO_2, Al_2O_3, $La_2Si_2O_7$, and other metal oxides. MEIS is a powerful tool for looking at problems such as if these materials react with silicon, and whether they are stable enough to survive CMOS fabrication.

A transmission electron microscope (TEM) uses a highly energetic electron beam (100 keV–400 keV) to image and obtain structural information from thin film samples [16]. The electron microscope consists of an electron gun, or source, and an assembly of electromagnetic lenses for focusing the electron beam. Apertures are used to select imaging modes and to select features of interest for electron diffraction work. The sample is illuminated with an almost parallel electron beam, which is scattered by the sample. In crystalline materials, the scattering takes the form of one or more Bragg-diffracted beams, which are used to form a transmission diffraction pattern. These diffraction patterns can be used to identify unknown phases in the sample. A bright-field image of the sample can be formed by looking at the straight-through, nondiffracted beam. Features in the sample that cause scattering have darker contrast in a bright-field image than those that cause little or no scattering. An electron diffraction pattern can be generated from a particular area in a bright-field image (such as a particle or grain) by using a selected area aperture. Dark-field images are formed from a single diffracted beam and are used to identify all the areas of a particular phase having the same crystalline orientation. A TEM is used to obtain structural information about a sample. TEM imaging is used routinely to examine thinned cross-sections of ICs and electronic devices to observe metal and polysilicon grain structure, crystalline defects in silicon (such as stacking faults and dislocations), diffusion barriers, thin metallization layers, defects in gate oxide layers, and so forth. TEM examination can reveal layer thicknesses and step coverage, show implanted regions, and provide delineation of p/n junctions. Because TEM sample preparation is fairly laborious, TEM analysis is generally reserved for solving those problems that cannot be handled with other tools, such as the scanning electron microscope.

X-ray photoelectron spectroscopy (XPS), also known as electron spectroscopy for chemical analysis, is an analysis technique used to obtain chemical information about the surfaces of solid materials [19]. Both composition and the chemical state of surface constituents can be determined by XPS. Insulators and conductors can easily be analyzed in surface areas from a few microns to a few millimeters across. The sample is placed in an ultrahigh vacuum environment and exposed to a low-energy, monochromatic X-ray source. The incident X-rays cause the ejection of core-level electrons from sample atoms. The energy of a photoemitted core electron is a function of its binding energy and is characteristic of the element from which it was emitted. Energy analysis

of the emitted photoelectrons is the primary data used for XPS. When the core electron is ejected by the incident X-ray, an outer electron fills the core hole. The energy of this transition is balanced by the emission of an Auger electron or a characteristic X-ray. Analysis of Auger electrons can be used in XPS, in addition to emitted photoelectrons. The photoelectrons and Auger electrons emitted from the sample are detected by an electron energy analyzer, and their energy is determined as a function of their velocity entering the detector. By counting the number of photoelectrons and Auger electrons as a function of their energy, a spectrum representing the surface composition is obtained. The energy corresponding to each peak is characteristic of an element present in the sampled volume. The area under a peak in the spectrum is a measure of the relative amount of the element represented by that peak. The peak shape and precise position indicates the chemical state for the element.

A scanning electron microscope (SEM) is a type of electron microscope that images a sample by scanning it with a high-energy beam of electrons in a raster scan pattern [20]. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography, composition, and other properties such as electrical conductivity. In a typical SEM, an electron beam is thermionically emitted from an electron gun fitted with a tungsten filament cathode. Tungsten is normally used in thermionic electron guns because it has the highest melting point and lowest vapour pressure of all metals, thereby allowing it to be heated for electron emission, and because of its low cost. Other types of electron emitters include lanthanum hexaboride cathodes, which can be used in a standard tungsten filament SEM if the vacuum system is upgraded and field emission guns, which may be of the cold-cathode type using tungsten single crystal emitters or the thermally assisted Schottky type, using emitters of zirconium oxide. When the primary electron beam interacts with the sample, the electrons lose energy by repeated random scattering and absorption within a teardrop-shaped volume of the specimen known as the interaction volume, which extends from less than 100 nm to around 5 um into the surface. The size of the interaction volume depends on the electron's landing energy, the atomic number of the specimen, and the specimen's density. The raster scanning of the cathode ray tube display is synchronized with that of the beam on the specimen in the microscope, and the resulting image is therefore a distribution map of the intensity of the signal being emitted from the scanned area of the specimen. The image may be captured by photography from a high-resolution cathode ray tube but in modern machines is digitally captured and displayed on a computer monitor and saved to a computer's hard disk.

Atomic force microscopy (AFM) or scanning force microscopy is a very high-resolution type of scanning probe microscopy, with demonstrated resolution on the order of fractions of a nanometer, more than 1000 times better than the optical diffraction limit [20]. The AFM is one of the foremost tools for imaging, measuring, and manipulating matter at the nanoscale. The information is gathered by "feeling" the surface with a mechanical probe. Piezoelectric elements that facilitate tiny but accurate and precise movements on (electronic) command enable the very precise scanning. In some variations, electric potentials can also be scanned using conducting cantilevers. In newer more advanced versions, currents can even be passed through the tip to probe the electrical conductivity or transport of the underlying surface, but this is much more challenging with very few research groups reporting reliable data. The AFM consists of a cantilever with a sharp tip (probe) at its end that is used to scan the specimen surface. The cantilever is typically silicon or silicon nitride with a tip radius of curvature on the order of nanometers. When the tip is brought into proximity of a sample surface, forces between the tip and the sample lead to a deflection of the cantilever according to Hooke's law. Depending on the situation, forces that are measured in AFM include mechanical contact force, van der Waals forces, capillary forces, chemical bonding, electrostatic forces, magnetic forces (magnetic force microscope), Casimir forces, and solvation forces. The AFM can be operated in a number of modes, depending on the application. In general, possible imaging modes are divided into static (also called contact) modes and a variety of dynamic (or noncontact) modes where the cantilever is vibrated.

Auger electron spectroscopy (AES) is a common analytical technique used specifically in the study of surfaces and, more generally, in the area of materials science [15]. Underlying the spectroscopic technique is the Auger effect, as it has come to be called, which is based on the analysis of energetic electrons emitted from an excited atom after a series of internal relaxation events. The Auger effect is an electronic process at the heart of AES resulting from the inter- and intrastate transitions of electrons in an excited atom. When an atom is probed by an external mechanism, such as a photon or a beam of electrons with energies in the range of 2 keV to 50 keV, a core state electron can be removed leaving behind a hole. As this is an unstable state, the core hole can be filled by an outer shell electron, whereby the electron moving to the lower energy level loses an amount of energy equal to the difference in orbital energies. Surface sensitivity in AES arises from the fact that emitted electrons usually have energies ranging from 50 eV to 3 keV, and at these values, electrons have a short mean free path in a solid. The escape depth of electrons is therefore localized to within a few nanometers of the target surface, giving AES an extreme sensitivity to surface species. Because of the low energy of Auger electrons, most AES setups are run under ultrahigh vacuum conditions. Such measures prevent electron scattering off residual gas atoms as well as the formation of a thin gas layer on the surface of the specimen which degrades analytical performance. Semiquantitative compositional and element analysis of a sample using AES is dependent on measuring the yield of Auger electrons during a probing event. Electron yield, in turn, depends on several critical parameters such as electron-impact cross-section and fluorescence yield. Since the Auger effect is not the only mechanism available for atomic relaxation, there is a competition between radioactive and nonradioactive decay processes to be the primary deexcitation pathway. Despite the advantages of high spatial resolution and precise chemical

sensitivity attributed to AES, there are several factors that can limit the applicability of this technique, especially when evaluating solid specimens. One of the most common limitations encountered with Auger spectroscopy is charging effects in nonconducting samples. When the number of secondary electrons is leaving the sample, charging is different to the number of incident electrons which is raised to a net polarity at the surface. Both positive and negative surface charges severely alter the yield of electrons emitted from the sample and hence distort the measured Auger peaks.

X-ray reflectivity (XRR) is a surface-sensitive analytical technique used in chemistry, physics, and materials science to characterize surfaces, thin films, and multilayers [13]. It is related to the complementary techniques of neutron reflectometry and ellipsometry. The basic idea behind the technique is to reflect a beam of X-rays from a flat surface and to then measure the intensity of X-rays reflected in the specular direction (reflected angle equal to incident angle). If the interface is not perfectly sharp and smooth, then the reflected intensity will deviate from that predicted by the law of Fresnel reflectivity. The deviations can then be analyzed to obtain the density profile of the interface normal to the surface.

3.2. Hf-Based Gate Oxide Dielectrics. Hafnium oxide is currently widely researched as a possible gate oxide insulating layer in CMOS technology. This is due to its high relative permittivity value ($k \sim 20$–25), its large energy band gap (-5.8 eV), and its band offset (-1.3 eV) with respect to the silicon conduction band. Its crystallization temperature can be raised if related silicates (e.g., $HfSiO_4$) or nitrided alloys are fabricated. A potential ALD precursor using the organometallic cyclopentadienyl is also recently investigated by Taechakumput et al. [32]. This precursor shows promising results as an alternative for producing high-quality HfO_2 films with low impurities. For the high-k dielectric HfO_2 films, deposited by liquid injection ALD and postdeposition annealed (PDA) in nitrogen (N_2) ambient, spectroscopic ellipsometric revealed large changes in the complex dielectric function that correlated with the electrical measurements. As the PDA temperature in a nitrogen environment is increased, deep traps can be annealed. It is suggested therefore that the origin of the deep traps in HfO_2 is related to oxygen deficiencies in the film. The Ultrathin HfO_2 films prepared on n-type (100) Si substrates by surface sol-gel process have amorphous structures with a very thin interface layer of 0.5 nm and small surface roughness (0.45 nm) [21]. XPS analyses indicate that the 500°C PDA treatment forms stronger Hf–O bonds, leading to passivated traps, and the interface layer is mainly Hf silicate ($Hf_xSi_yO_z$) between HfO_2 and Si. Figure 6 shows the Hf 4f region of the XPS spectra which consists of the $4f_{5/2}$ and $4f_{7/2}$ components at different binding energies of Hf–O bonds. The EOT value of 0.84 nm has been obtained, which is a low EOT value to date for HfO_2 fabricated by other methods.

Future iterations of highly scaled CMOS technology nodes require alternate materials and structures to meet the projected performance metrics for high-performance and low-power applications. III-V compound semiconductors

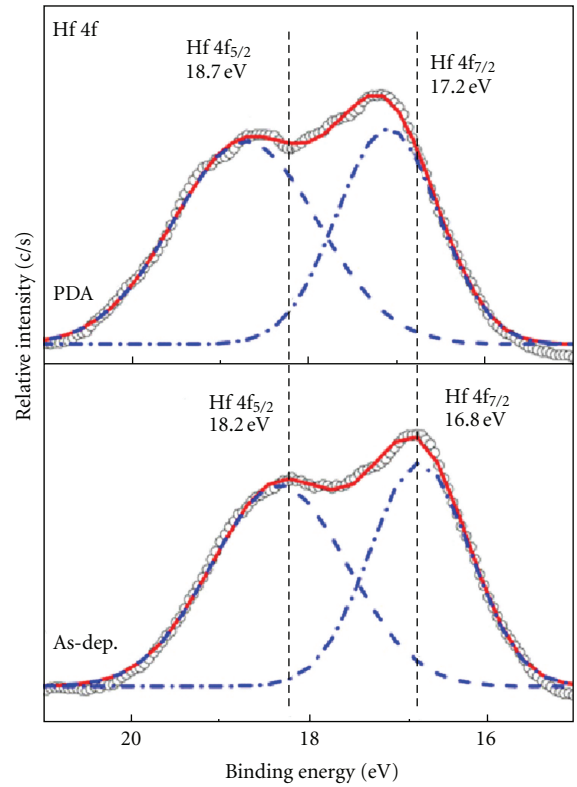

Figure 6: Hf_4f regions XPS spectra of HfO_2 ultrathin films deposited on Si with and without 500°C PDA treatment [21].

are considered as one of the most attractive alternative channel materials to replace silicon and achieve the projected high-performance characteristics. In applications to III-V CMOS fabrication, however, many fundamental problems need to be resolved, including crystallization in HfO_2, increases in EOT, defect formation due to chemical reactions during and after deposition of HfO_2, to name a few. The effects of Al_2O_3 passivation are introduced Al_2O_3 layers on both sides of HfO_2 film on GaAs. The amorphous Al_2O_3 layers conferred enhanced thermal stability and efficiently blocked the diffusion of oxidizing species upon annealing. The $Al_2O_3/HfO_2/Al_2O_3$ high-k dielectric stack in GaAs MOS capacitors significantly improves physical and electrical characteristics compared to HfO_2 alone on GaAs [22]. Figure 7 shows the high-resolution TEM images of 5 nm HfO_2 and Al_2O_3(1 nm)/HfO_2(3 nm)/Al_2O_3(1 nm) high-k gate dielectric stack on GaAs, as deposited and after annealing at 600°C for one minute. The TEM images suggest that the Al_2O_3 passivation layers inhibited the crystallization of the HfO_2 film not only during deposition but also during annealing. $Al_2O_3/HfO_2/Al_2O_3$ high-k dielectric stack in GaAs MOS capacitors significantly improves physical and electrical characteristics compared to HfO_2 alone on GaAs. At elevated temperatures, the amorphous Al_2O_3 layers are effective in inhibiting crystallization of HfO_2. TEM and XPS data supported the improved electrical characteristic of GaAs MOS capacitors with $Al_2O_3/HfO_2/Al_2O_3$ gate dielectric stack.

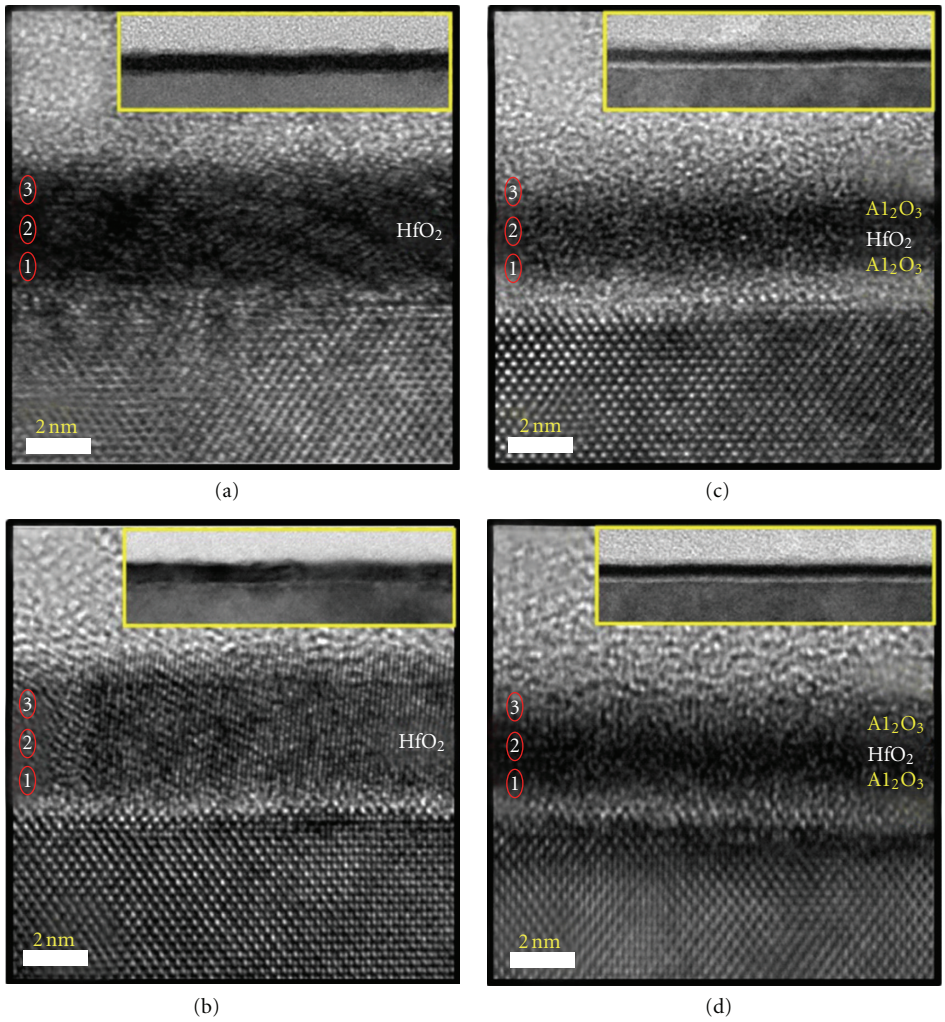

Figure 7: Cross-sectional TEM micrographs of HfO_2/GaAs systems: (a) as-deposited and (b) after annealing at 600°C for 1 min in N_2 ambient. Cross-sectional TEM micrographs of $Al_2O_3/HfO_2/Al_2O_3$/GaAs systems: (c) as-deposited and (d) after annealing at 600°C for 1 min in N_2 ambient [22].

For the thin films of ZrO_2 and HfO_2 [40] which have been deposited by liquid injection MOCVD and ALD using a range of ansa-metallocene precursors, XRD analysis shows that the HfO_2 films deposited by MOCVD are amorphous, whereas the ZrO_2 films deposited by MOCVD were in the tetragonal phase. AES shows that residual carbon is present in all the films and that the films grown by MOCVD contained more carbon (2.4–17.0 at.%) than the films grown by ALD (1.8–2.8 at.%). The dielectric properties of ZrO_2 and HfO_2 films deposited by ALD are evaluated using (Al/MO_2/n-Si) MOS capacitor structures which show that the films had low current leakage densities. Analysis of the molecular structures from XRD and density functional theory calculations shows complete encapsulation of the metal centre by the ligands in the unbridged metallocenes, but a slight opening up of the metal in the ansa complexes, due to tilting of the bridged Cp rings. The complexes have proved suitable for the deposition of ZrO_2 and HfO_2 thin films by liquid injection MOCVD and ALD. The MOCVD and ALD growth data indicate that these complexes deposit oxide films at higher substrate temperatures than unabridged metallocene complexes such as $[(MeCp)_2MMe(OMe)]$. This offers the potential for the ALD of higher density oxide films with a reduction in impurities.

HfO_2 has been shown to crystallize at relatively low temperatures (~400°C). However, it is preferable that gate insulators stay amorphous after a conventional activation annealing (800°C) because it is a concern that grain boundaries may serve as the paths of dopant diffusion and produce a variation of electrical properties. Lanthanum is considered as an interesting alternative dielectric gate for its properties: $k \sim 25$–30 and electric potential gap ~5.5 eV. Moreover La reacts with silica to form a silicate and its silicate is believed to be more stable with respect to silicon and to have a lower dielectric constant. The consequences of lanthanum localization in such stacks on the evolution of the films during the rapid thermal annealing are investigated in term of morphology, crystalline structure, silicate formation, and film homogeneity as a function of depth. Various rapid thermal annealing integrations on the La_2O_3/HfO_2 and

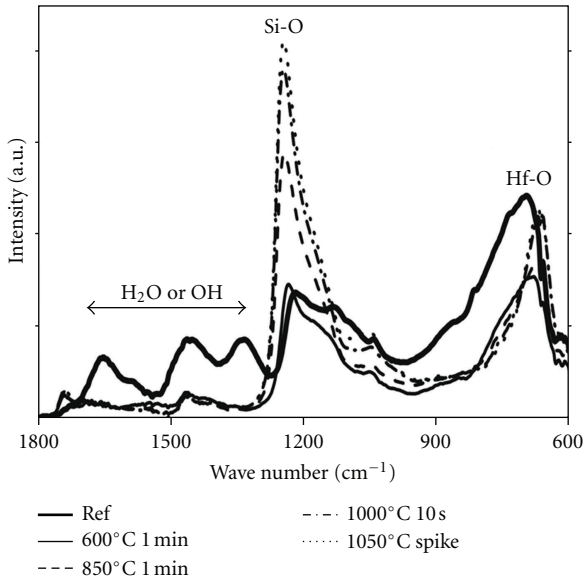

Figure 8: ATR spectra of the HfO_2-La_2O_3 samples before and after thermal annealing [23]. The hydrated La_2O_3 layer disappears with the loss of the peaks attributed to the H_2O-OH vibration. The amorphous structure of the films changes to a quadratic structure from 850°C for the sample La_2O_3-HfO_2 and from 1000°C for the sample HfO_2-La_2O_3.

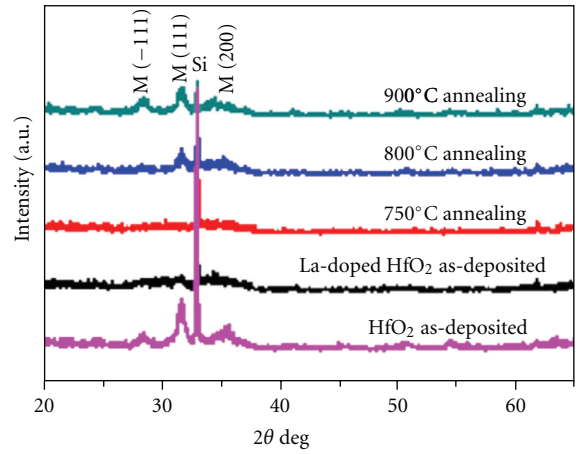

Figure 9: XRD patterns of La-doped HfO_2 films on Si deposited at 600°C for 45 min and annealed at various temperatures [24]. XRD patterns of 50 nm thick La-doped HfO_2 films are deposited on Si at 600°C for 45 min and annealed at various temperatures. The pure HfO_2 film has crystallized as-deposited and the La-doped HfO_2 films deposited at 600°C show amorphous feature. No crystalline peak is observed in 750°C postannealed La-doped HfO_2.

HfO_2/La_2O_3 stacks are deposited by ALD which is reported by Rébiscoul et al. [23]. The morphology, crystalline structure, silicate formation, and film homogeneity are found to be a function of the depth for the consequences of lanthanum localization in such stacks on the evolution of the films during the rapid thermal annealing. The La_2O_3 location has an impact on the temperature of the quadratic phase formation linked to the formation of SiOHfLa silicate and the resistance of the films to dissolution in HF 0.05 wt%. The hydrated La_2O_3 layer disappears as Figure 8 shows with the loss of the peaks attributed to the H_2O-OH vibration. The amorphous structure of the films changes to a quadratic structure from 850°C for the sample La_2O_3-HfO_2 and from 1000°C for the sample HfO_2-La_2O_3. It means that even if the samples present a quadratic structure, this structure is slightly different depending on samples showing that La location has a real impact on the crystalline structure.

The introduction of a slight amount of La into HfO_2 films significantly raises the crystalline temperature to 750°C [24]. The La-doped HfO_2 films have an intrinsic dielectric constant of 28 at 1 MHz with the band gap of 5.6 eV. XPS analyses reveal that the interfacial layer is Hf-based silicate. XRD is explored to characterize the structure of La-doped HfO_2 films. Figure 9 shows the XRD patterns of 50 nm thick La-doped HfO_2 films deposited on Si at 600°C for 45 min and annealed at various temperatures. The pure HfO_2 film has crystallized as-deposited and the La-doped HfO_2 films deposited at 600°C show amorphous feature. No crystalline peak is observed in 750°C postannealed La-doped HfO_2. Evidently, the incorporation of slight amount of La into HfO_2 has enhanced the crystallization temperature of the HfO_2 films to 750°C. A reliable value of EOT around 1.2 nm with leakage current density of 3 A/cm^2 has been obtained. The results indicate that MOCVD-derived La-doped HfO_2 shows promising thermodynamic and electrical properties for next generation MOSFET application.

Physical properties of $La_2Hf_2O_7$ films have been measured and analyzed using MEIS and XRD [25]. The thicknesses of the deposited $La_2Hf_2O_7$ thin films, measured by MEIS, are 8 and 18 nm, respectively, for both as-deposited and PDA samples. The interfacial layer between the $LaHf_2O_7$ dielectric and silicon substrate is observed to be around 1.5 nm in the as-deposited samples. For the PDA samples, the interface layer using MEIS increased to around 4.5 nm thickness, which is attributed to an internal O and La diffusion mechanism to form a La_2O_3-SiO_2 silicate layer [29]. A permittivity of 10 is confirmed using the relationship between CET evaluated and $La_2Hf_2O_7$ physical thickness (8 and 18 nm). XRD is carried out using a Rikagu Miniflex X-ray diffractometer with nickel-filtered radiation for all samples. The XRD analysis of the as-deposited and PDA samples is demonstrated in Figure 10. A crystalline diffraction feature is observed on the 18 nm thin film after PDA. However, no phase transition is shown on the 8 nm thin film after the same PDA, which suggests that it remained essentially amorphous.

It is noteworthy that the eight-coordinate ionic radius of Ce^{4+} is closer to that of Hf^{4+} than the majority of rare earth ions, suggesting that Ce^{4+} will be readily incorporated into the HfO_2 crystal lattice without introducing oxygen vacancies [41]. After annealing at 900°C, $CeHfO_2$ films are transformed from an amorphous state into a stabilized cubic or tetragonal phase. The analysis of the $Ce_{0.17}Hf_{0.83}O_2$ and $Ce_{0.34}Hf_{0.66}O_2$ films by AES shows that carbon contamination is absent at an estimated detection limit of 0.5%. There is a linear relationship between the cerium precursor

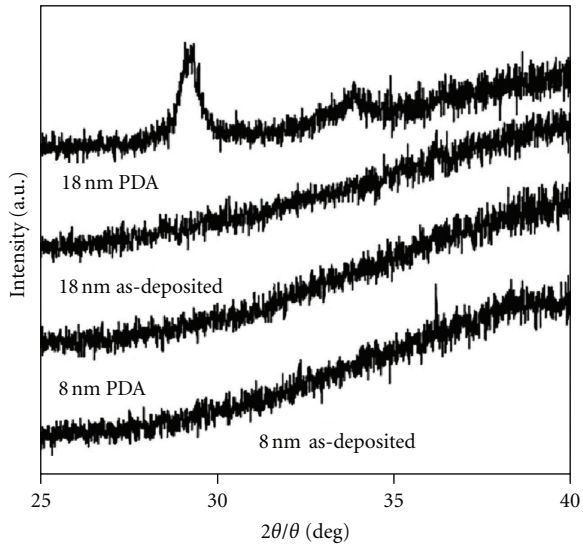

Figure 10: X-ray diffraction data for $La_2Hf_2O_7$ thin films deposited by ALD, and then PDA in N_2 for 15 min at 900°C [25]. The thicknesses of $La_2Hf_2O_7$ thin films are 8 and 18 nm, respectively. A crystalline diffraction feature is observed on the 18 nm thin film after PDA. However, no phase transition is shown on the 8 nm thin film after the same PDA, which suggests that it remained essentially amorphous.

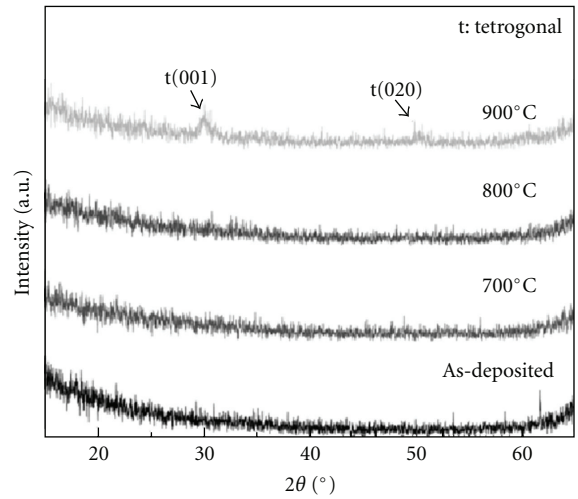

Figure 11: XRD spectra of $Zr_{0.7}Si_{0.3}O_2$ films annealed at different temperatures with RTA process in N_2 for 60 s [26]. $(ZrO_2)_{0.7}(SiO_2)_{0.3}$ films remained amorphous after being annealed at 700 and 800°C, while some diffraction peaks from the tetragonal phase of ZrO_2 appeared for the films annealed at 900°C. No diffraction peak from the crystallized SiO_2 could be found, indicating that part of ZrO_2 particles is separated from Zr-silicate film, while the remainder is still amorphous after annealing at 900°C with RTA process.

mole fraction injected and cerium incorporated in the high-k film. The XRD analysis of all the films grown at 300°C by ALD shows the absence of any significant diffraction features indicating that they are all essentially amorphous as deposited. A cross-section micrograph from a thicker vacuum-annealed sample confirms that the thickness of the interfacial SiO_2 does not increase during vacuum annealing. A small diffraction feature is evident in the XRD data in the as-grown sample; however, annealing transforms the film into a polycrystalline layer of either the cubic or tetragonal phase.

3.3. Zr-Based Oxide Gate Oxide Dielectrics. ZrO_2 is one of the most promising candidates for its high dielectric constant (~20) and large band gap. Unfortunately, the low crystallization temperature of ZrO_2 and the formation of low-k interface layers between high-k films and Si substrates which increase EOT limit its utility in the future CMOS technology. Compared with pure ZrO_2, Zr-silicates have higher crystallizing temperature and are more thermal stable in directly contact with Si. Pseudoternary alloy films of $(ZrO_2)_{0.5}(SiO_2)_{0.5}$, $(ZrO_2)_{0.6}(SiO_2)_{0.4}$, $(ZrO_2)_{0.7}(SiO_2)_{0.3}$, $(ZrO_2)_{0.7}(SiO_2)_{0.3}/(ZrO_2)_{0.5}(SiO_2)_{0.5}$, and $(ZrO_2)_{0.5}$ $(SiO_2)_{0.5}/(ZrO_2)_{0.7}(SiO_2)_{0.3}$ films have been deposited on p-Si(100) substrates by using pulsed laser deposition technique [26]. $(ZrO_2)_{0.5}(SiO_2)_{0.5}$ films have a good thermal stability and remained amorphous after annealing at 800°C in N_2, as indicated by XPS spectra and XRD. Figure 11 shows the XRD patterns of $(ZrO2)_{0.7}(SiO2)_{0.3}$ films deposited on p-Si wafers and annealed in N_2 ambient with RTA process at 700, 800, and 900°C for 60 s, respectively. $(ZrO2)_{0.7}(SiO2)_{0.3}$ films remained amorphous after being annealed at 700 and 800°C, while some diffraction peaks from the tetragonal phase of ZrO_2 appeared for the films annealed at 900°C. No diffraction peak from the crystallized SiO_2 could be found, indicating that part of ZrO_2 particles separated from Zr-silicate film, while the remainder is still amorphous after annealing at 900°C with RTA process. In order to investigate the chemical-binding states in the interface layers of Zr-silicates films with Si substrate, XPS is employed. The Zr 3D XPS spectra of the films before and after annealing with rapid thermal anneal process at 800°C are compared.

As-deposited ZrO_2/La_2O_3 film stacks have relatively dielectric constant of 24 which is increased to a value of 35 after annealing at 500°C due to the stabilization of tetrago -nal/cubic ZrO_2 phases [27]. This effect depends on the absolute thickness of ZrO_2 within the dielectric stack and is limited due to possible interfacial reactions at the oxide/Ge interface. The XRD analysis, as shown in Figure 12 for a 4 nm La_2O_3/6 nm ZrO_2 stack on (100) Ge, before and after PDA at 600°C in Air is performed. The as-deposited sample does not show any distinct peak in the XRD spectra, whereas the sample after PDA shows a clear peak that can be assigned to very high-k cubic (c-) and/or tetragonal (t-) ZrO_2 phases. The same experiments on (100) Si substrates and obtained very similar results from the XRD-analyses are similar to perform.

It is anticipated by Gaskell et al. [42] that at certain La concentrations the material would have a relatively high dielectric constant and that it would remain amorphous to high temperature. In addition, by analogy with HfO_2, the addition of La may stabilize the cubic or tetragonal phases

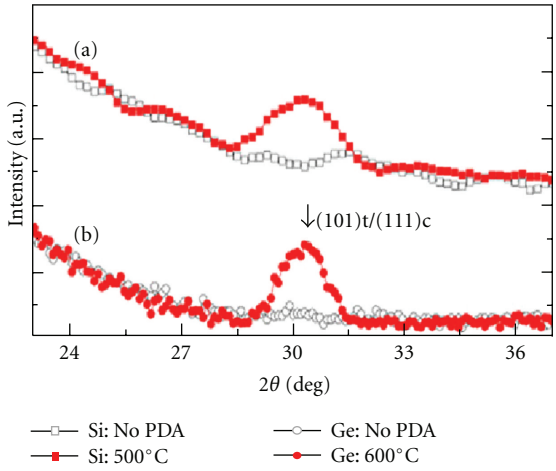

FIGURE 12: XRD spectra for (a) a 4 nmLa_2O_3/6 nmZrO_2 dielectric stack on Si, before and after PDA at 500°C in air, and for (b) a 4 nm La_2O_3/6 nm ZrO_2 dielectric stack on Ge, before and after PDA at 600°C in air [27]. The as-deposited sample does not show any distinct peak in the XRD spectra, whereas the sample after PDA shows a clear peak that can be assigned to very high-k cubic (c-) and/or tetragonal (t-) ZrO_2 phases.

of ZrO_2 which are expected to have higher k values than the more thermodynamically stable monoclinic phase. At lower La atomic fractions ($x = 0.22$) thin films of lanthanum zirconium oxide $La_xZr_{1-x}O_2$ are stabilized in the cubic phase after annealing at 700°C in air. At higher La atomic fractions ($x > 0.35$), the films remain amorphous after annealing. The physical properties of $LaZrO_2$ and $CeHfO_2$ thin films are researched implementing AES, XRD, MEIS, XTEM, and AFM [43]. All as-deposited films are amorphous and contained no diffraction peaks in XRD data. For the annealed samples, a La concentration stabilized a mixed phase of zirconia of either the tetragonal or cubic phase, with some diffraction features from the monoclinic phase and the tetragonal/cubic phase, and cannot be unambiguously determined by XRD. Increasing the level of doping stabilizes the tetragonal or cubic phase and no monoclinic content is found.

3.4. Aluminate Gate Oxide Dielectrics. HfO_2 film as a candidate of high-k dielectric materials has been extensively studied. The main challenge is the formation of interfacial layer at high-k/Si interface during the deposition/annealing process, and interfacial layer was composed of SiO_x, Hf-silicates, or Hf-silicides. These by-products of processing suppress the effective dielectric constant and degrade the electrical performances of devices. Recently, Al_2O_3 is used as a reaction blocking layer for HfO_2 due to its high-temperature thermal stability. HfO_2 gate dielectric films with a blocking layer of Al_2O_3 inserted between HfO_2 layer and Si layer (HfO_2/Si) are treated with rapid thermal annealing process at 700°C. The interfacial structure and electrical properties are researched by Cheng et al. [28]. The results of XPS of Figure 13 show the interfacial layer of SiO_x transformed in SiO_2 after the annealing treatment, and Hf-silicates and Hf-silicides are not detected. The results of high-resolution TEM indicate that the interfacial layer is composed of SiO_2 for the annealed film with blocking layer. High-density RONs have been prepared on ALD Al_2O_3 films by magnetic sputtering and PDA [44]. The chemical composition of the resulting nanodots is analyzed by XPS, revealing coexistence of Ru, RuO_2, and RuO_3. This is attributed to chemical reaction between Ru and Al_2O_3, as well as Ru oxidization incurred by trace oxygen in the annealing ambient during rapid thermal anneal. Various MOS capacitors with RONs embedded into ALD Al_2O_3 as an insulator have been fabricated using a high work function Pd electrode. HfO_2 dielectric films with blocking layers of Al_2O_3 are deposited on high resistivity silicon-on-insulator, and the interfacial properties are reported [45]. Energy dispersive XRS and XPS confirmed that blocking layer weakened Si diffusion and suppressed the further growth of HfSiO. A blocking layer of Al_2O_3 inserted between HfO_2 and HRSOI would control the diffusion of Si, suppress the formation of Hf-silicates, lead to a SiO_x-like interface layer of 1 nm, keep the interface smooth, and keep HfO_2 amorphous during post deposition annealing.

Although ZrO_2, HfO_2, and their associated silicates and aluminates have been the most intensively investigated high-k materials, there has been much recent interest in the lanthanide oxides. The lanthanide aluminates, $MAlO_3$ (M = Pr, Nd), are promising high-k materials, as they combine the advantages of the high permittivity of the lanthanide oxide with the chemical and thermal stability of Al_2O_3. Furthermore, they remain amorphous up to high temperatures, leading to a large reduction in leakage current relative to polycrystalline M_2O_3 films and to inhibition of the growth of a SiO_2 interfacial layer during CMOS processing. AES shows that all the praseodymium aluminate ($PrAlO_x$) and neodymium aluminate ($NdAlO_x$) films [46] are high pure, with no carbon detectable. XRD shows that the $PrAlO_x$ and $NdAlO_x$ films remained amorphous up to temperatures of 900°C. Films grown by ALD are all Pr- or Nd-deficient, but near-stoichiometric films of $PrAlO_x$ (Pr/Al ~ 0.76) and $NdAlO_x$ (Nd/Al ~ 0.87) are obtained by MOCVD at deposition temperatures of 500 and 450°C, respectively. The hafnium (HfO_2), zirconia (ZrO_2), lanthanum aluminate ($LaAlO_3$), and neodymium aluminate ($NdAlO_3$) high-k thin films are characterized by XTEM [21]. While the thickness of the native SiO_2 interfacial layer between the high-k thin film and Si-substrate is approximately 1.5 nm, all high-k dielectric layers considered were 16 nm in thickness as measured using XTEM shown in Figure 14.

3.5. Rare Earth Gate Oxide Dielectrics. In order to satisfy the demand for higher performance and integration density in microelectronics, the scaling of MOSFETs becomes more and more aggressive. A promising class of materials for high-k applications is the rare earth scandates because of their favorable material properties. For single crystals of these ternary oxides, dielectric constants of 20–35 depend on the lattice direction. An optical band gap larger than 5 eV is obtained for thin amorphous films grown by PLD [40]. In contact with silicon the amorphous phase of $LaScO_3$

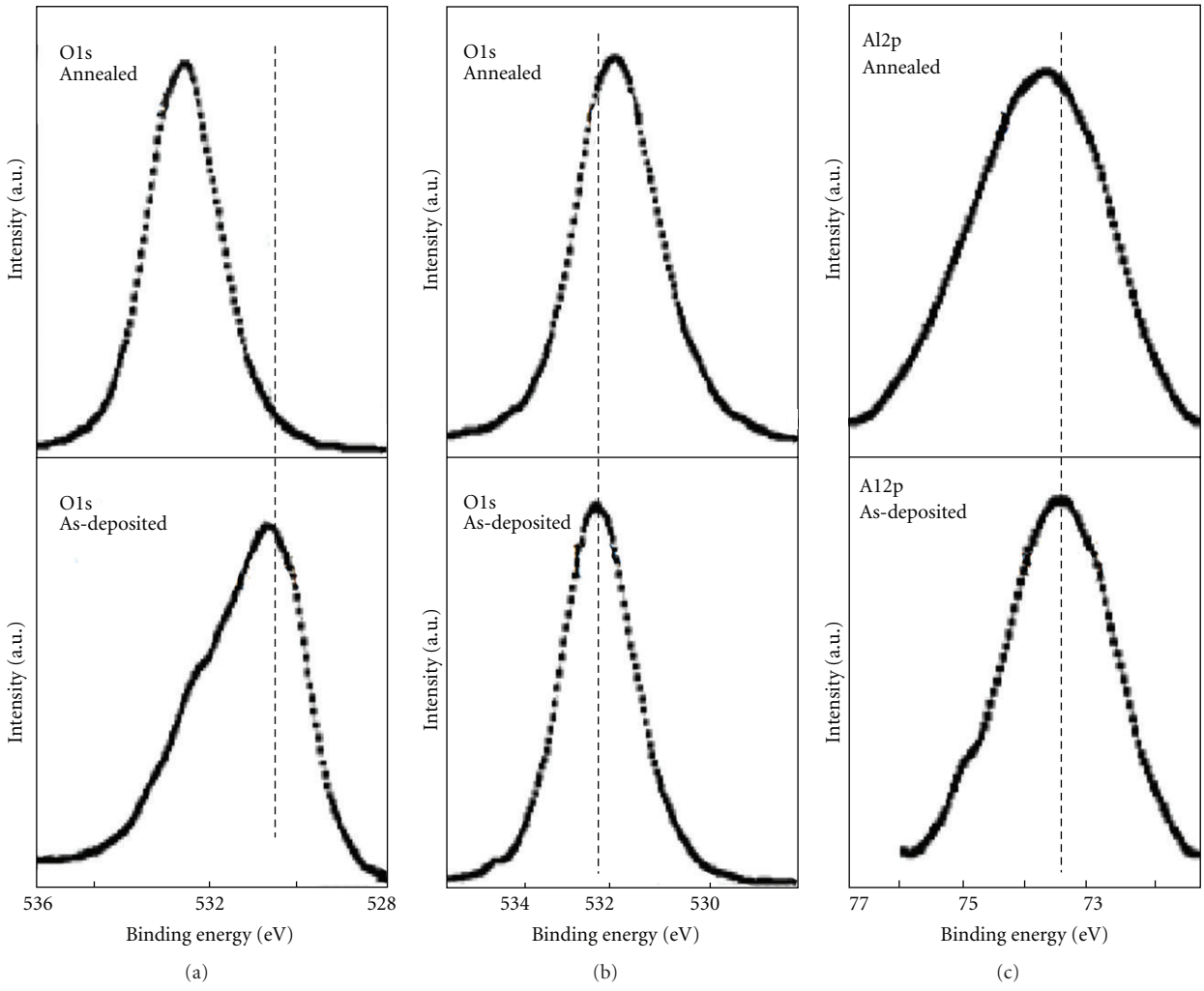

Figure 13: XPS spectra for the as-deposited film and the annealed film, respectively: (a) O1s spectra with a blocking layer, (b) O1s spectra without blocking layer, and (c) Al2p spectra [28].

is stable up to 800°C while $GdScO_3$ thin films remain amorphous up to 1000°C. $GdScO_3$ has been exemplarily selected to investigate the deposition of thin films with an unconventional deposition technique for such a material, because of little differences in the morphological and electrical properties of $DyScO_3$ and $GdScO_3$ and their superior thermal stability [29]. Measurements with Rutherford back scattering spectrometry, high-temperature XRD, XRR, TEM, and AFM are performed. A stoichiometric transfer of material from the source to the substrate in high vacuum could be demonstrated. Homogeneous, amorphous, and smooth films stable up to 1000°C are obtained. Data of a 20 nm thick $GdScO_3$ film deposited at 600°C on an HF last surface are obtained. The surface is very smooth as indicated by AFM measurements (Figure 15). A peak-to-valley roughness of about 1 nm and RMS roughness of below 0.1 nm for film thicknesses up to 20 nm within a scan size are revealed. Obviously the layer remains amorphous up to 1000°C. At 1100°C, phase segregation occurs and $GdScO_3$ crystallites start to form.

Er_2O_3 is an attractive candidate since it has a relatively high dielectric constant, large conduction band offset with Si (about 3.5 eV), and is chemically stable in contact with Si. Amorphous Er_2O_3 films on Si (001) by reactive evaporation with annealing at various temperatures in oxygen ambients are studied by Ze-Bo et al. [30]. It is found that the film annealed at 450°C for 30 min results in a significant improvement in the morphology and electrical properties, and at the same time the interfacial layer thickness does not increase. The amorphous gate dielectric has more advantages than polycrystalline and single-crystalline materials because polycrystalline dielectrics will lead to higher leakage current due to the polycrystalline grain boundaries, and the epitaxial growth of high-k oxides is technically difficult and expensive. Cross-sectional high-resolution TEM (Figure 16) is performed to certify the amorphous structure of the Er_2O_3 film annealed in O_2 ambience at 700°C and acquire the interfacial information between Er_2O_3 and Si. A uniform amorphous structure without obvious crystallization is presented in the Er_2O_3 film. The XRD and the cross-sectional high-resolution

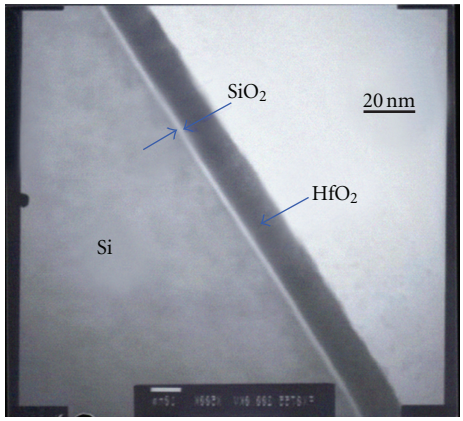

Figure 14: A XTEM image of HfO_2/SiO_2 stack. The thickness of interfacial layer is 1.5 nm (assumed to be SiO_2) and the high-k layer is l6 nm [21].

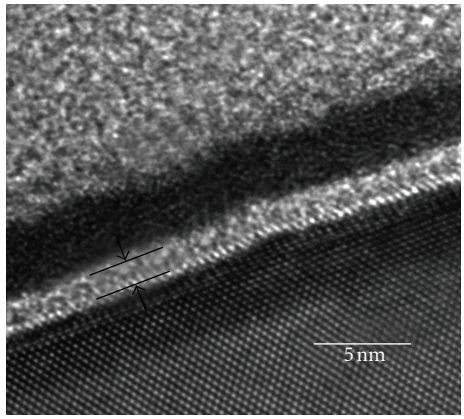

Figure 16: A cross-sectional high-resolution TEM image of the Er_2O_3 film annealed at 700°C for 30 min in O_2 ambience. The thickness of the interfacial SiO_2 layer is estimated to be around 1.6 nm [30].

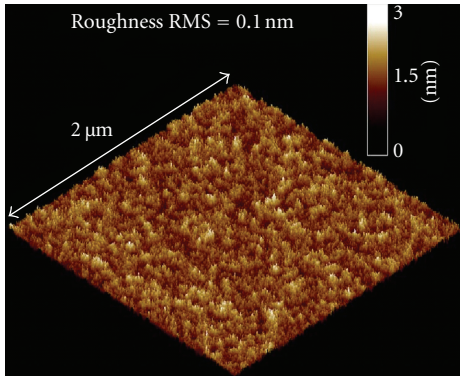

Figure 15: AFM scan of an ~20 nm thick GdScO3 film: the peak-to-valley value 1 nm, and the RMS roughness 0.1 nm [29].

TEM measurement reveals that the films are amorphous even after thermal annealing up to 700°C in O_2 ambience. Annealing at 450°C is the optimal condition for the growth of Er_2O_3 high-k dielectric films, and the film exhibits high capacitances and low leakage current densities.

High-k/Si stacks have often been observed to degrade channel mobility due to phonon scattering and coulomb scattering. The mobility can be enhanced by the introduction of an interfacial layer. The channel mobility is improved after high-temperature annealing, which is due to the formation of interfacial oxides. High electron mobility can be achieved by careful optimization of a conventional, self-aligned CMOS process [38]. By using high-concentration ozone oxidation at low temperature, the Hf-silicate interface layer between HfO_2 and silicon substrate is effectively controlled [47]. Thermal stability, interfacial structure if amorphous $(La_2O_3)_{0.5}(SiO_2)_{0.5}$ (LSO) films deposited by using pulsed deposition on Si, and NH_3-nitrided Si substrates are comparatively researched [31]. The LSO films keep the amorphous state up to a high annealing temperature of 900°C. Figure 17 shows the effects of the postannealed on the interfacial structure of the LSO/p-Si structures with and without NH3 nitridation treatment before LSO deposition. The surface nitridation of silicon wafer using NH_3 can result in the formation of the passivation layer, which effectively suppresses the excessive growth of the interfacial layer between LSO film and silicon wafer after high-temperature annealing process using high-resolution TEM observation and XPS analyses.

4. Electrical Properties of High-k Films

Since leakage limitation constrains further reduction, an alternative method to increase gate capacitance is altering k by replacing silicon dioxide with a high-k material. In such a scenario, a thicker gate layer might be used which can reduce the leakage current flowing through the structure as well as improving the gate dielectric reliability. Other key considerations include band alignment to silicon (which may alter leakage current), film morphology, thermal stability, maintenance of a high mobility of charge carriers in the channel, and minimization of electrical defects in the film/interface. Electrical properties of high-k dielectric films and their integration with the conventional CMOS processing are the main topics of research now. The high-k dielectric materials and related techniques are crucial for continuing the Si-based scaling engineering. Although many investigations have been devoted to different aspects of the preparation and properties of high-k dielectrics and their integration with conventional Si devices, there are still many obstacles that need to be conquered. In the context of compatibility with the Si MOSFET technology, many challenges are as follows: (1) incompatibility with annealing temperatures used for activating poly-Si gates; (2) relatively poor quality, which causes charge trapping and makes the Si MOSFET gate unstable; (3) channel mobility degradation; and (4) threshold voltage shift induced by high-k material [19]. The high-k films listed in this section have been researched and in recent years to provide solutions for the challenges encountered and provide inspiration for future work.

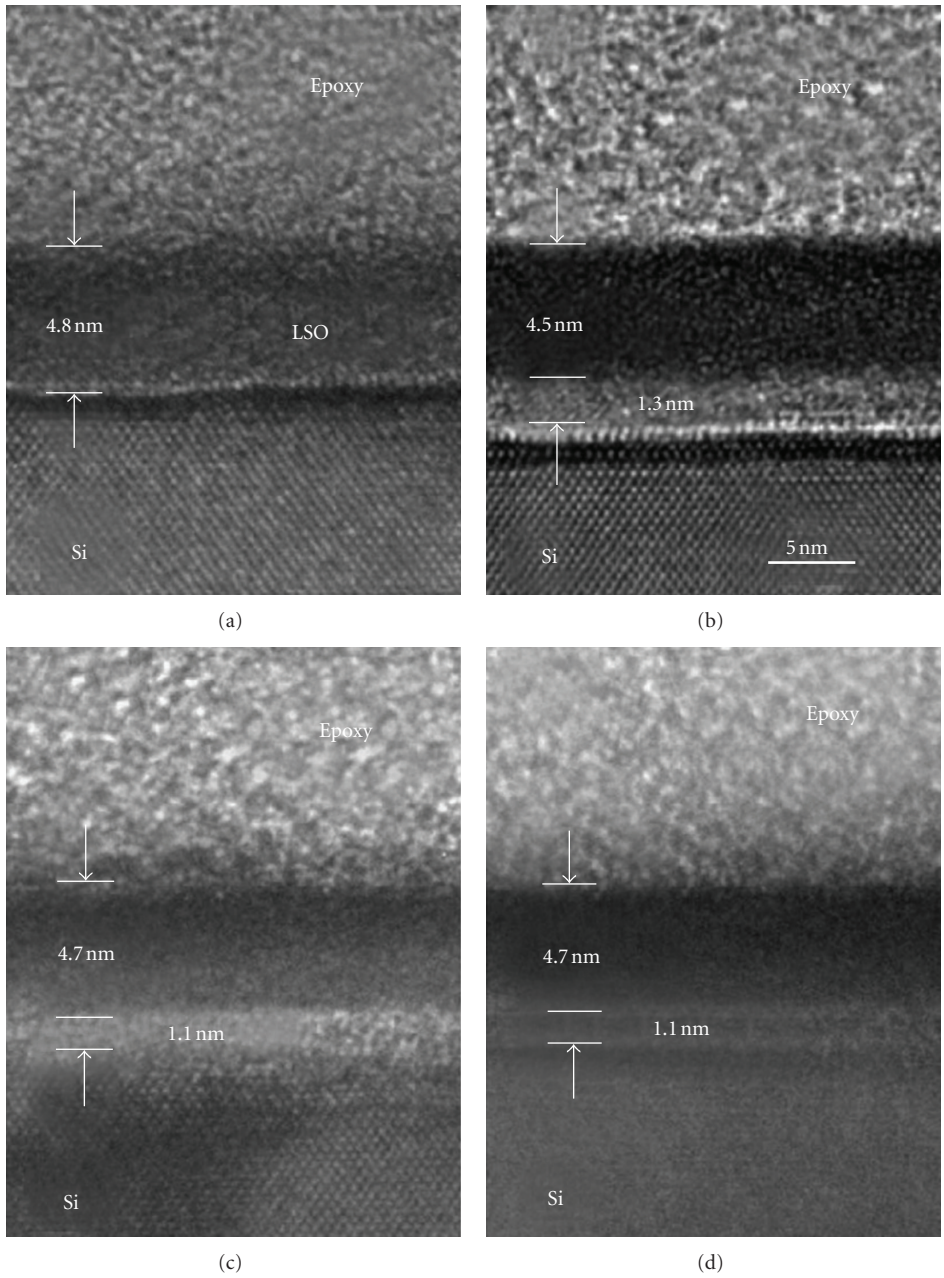

FIGURE 17: High-resolution TEM images of $(La_2O_3)_{0.5}(SiO_2)_{0.5}$ films deposited on Si (100) substrate: (a) as-deposited, (b) annealed at 750°C in N_2 for 40 s, and on nitrided Si (100) substrate: (c) as-deposited, (d) annealed at 750°C in N_2 for 40 s [31].

4.1. Hf-Based Gate Oxide Dielectrics

4.1.1. Hafnium Oxide. Hafnium oxide gate dielectrics have been prepared by various techniques, such as physical vapor deposition (radio-frequency and magnetron sputtering, ion beam sputtering, molecular beam epitaxy, laser ablation), solution deposition (sol-gel, metal-organic decomposition), and MOCVD and ALD. Of these techniques, MOCVD and ALD are particularly well suited to modern manufacturing methods for microelectronics [16]. Ultrathin HfO_2 films are prepared on n-type (100) Si substrates by surface sol-gel process [21]. A series of analytical techniques are implemented to characterize the structure, surface morphology, and electrical properties of ultrathin HfO_2 films on Si. For Pt/HfO_2/Si after 500°C PDA treatment, the leakage current density is 0.7 Acm^{-2} at V_{fb} = +1 V. The current conduction mechanism varies from Schottky-Richardson emission to Fowler-Nordheim tunneling at an applied higher positive voltage due to the activated partial traps remaining in the HfO_2 films. For the high-k dielectric HfO_2 films, deposited by liquid injection atomic layer deposition (LI-ALD) and PDA in nitrogen (N_2) ambient [32], I-V results also show that N_2-based PDA enhances the average energy depth of the shallow trapping defects. This corresponds

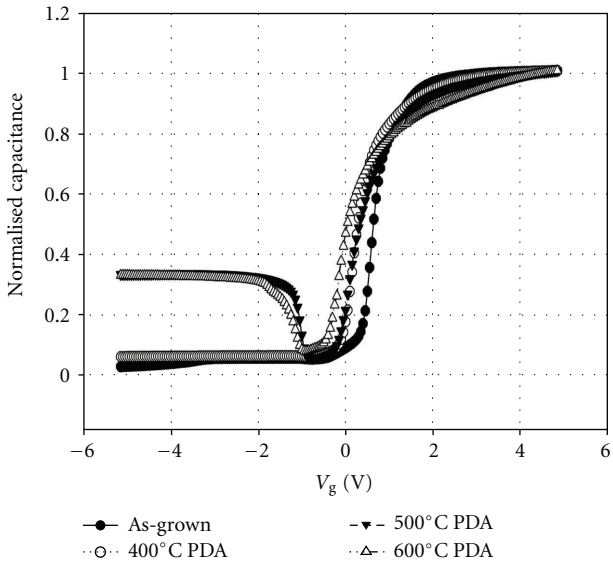

Figure 18: Effect of postdeposition annealing on normalized C-V characteristics (positive sweep) [32].

to the measured increase in MOS C-V hysteresis and interface states density. C-V characteristics, demonstrated in Figure 18, show clear accumulation, depletion, and inversion regions. However, the annealed samples with PDA temperature greater than 500°C show a different behavior in the inversion region. This is probably due to an enhanced minority carrier generation of Hafnium-related species (holes, in this case) at or near the oxide-silicon interface after PDA. In the present case, the flat-band voltage shift for the as-deposited sample is diminutive, indicating a small amount of fixed oxide charge in the oxide. However, it is observed that the flat band voltage shift negatively as PDA temperature increased. This indicates that negative fixed oxide charges could be annealed out by the PDA or they are compensated by nitrogen-induced positive fixed oxide charges generated during postdeposition annealing. The dielectric constant (k), calculated from accumulation capacitance assuming a SiO_2 interlayer, is $k \sim 17$-18.

A 5 nm epitaxial cubic phase HfO_2 layer as gate dielectrics is grown on Si substrates by PLD and then these samples are annealed at 900°C in N_2 [48]. Magnetron sputtering is used to deposit 0.2 mm Ru dots for contact electrodes. The leakage current density of Ru/HfO_2/Si/Ag MOS capacitors has been improved by six orders of magnitude through annealing at 900°C in N_2. Since the interface layer thickness has not been found to change much after high-temperature annealing, this improvement in leakage current may be due to the enhanced phonon-energy coupling and passivation of interfacial bonds. The HfO_2 gate insulators show excellent electrical properties with a k value of 26 and leakage current of 5×10^{-6} Acm^{-2} at -1 V. The lower capacitance for the samples without annealing is likely due to the interface defects. C-V characteristics were improved in both the accumulation and the depletion regions for the samples annealed at 900°C for 5 min in N_2, which results in the passivation of interfacial bonds during annealing. The k value is significantly higher than that of monoclinic pure HfO_2 ($\sim$17), which exhibits the advantage of cubic HfO_2 in dielectric characteristics. Flat band voltage shift in the C-V curves for the annealed samples has been observed at frequency of 1 MHz, which is likely caused by the complex bonding of mixed oxides doped with nitrogen.

4.1.2. Alumina as Blocking Layer for Hafnium Oxide. The main challenge for HfO_2 film as a candidate of high-k dielectric is the formation of interfacial layer at high-k/Si interface during the deposition/annealing process. These by-products of processing reduce the effective dielectric constant and degrade the electrical performances of devices. Al_2O_3 has been used as a reaction blocking layer for HfO_2 due to its high-temperature thermal stability. The effect of Al_2O_3 blocking layer is to suppress the growth of IL at Si interface. Al_2O_3 layer could also control the growth of Hf-silicates and Hf-silicides during postdeposition annealing. HfO_2 dielectric films with blocking layers of Al_2O_3 are deposited on high-resistivity silicon-on-insulator (HRSOI), and the electrical properties are reported by Cheng et al. [45]. Electrical measurements indicate that there was no hysteresis observed in capacitance-voltage curves, and flat band shift and interface state density are 0.05 V and 1.3×10^{12} Acm^{-2}, respectively. Electrical performance is improved including the enhancement of gate capacitance density and the reduction of fixed charges density. Therefore, the introduction of HfO_2 dielectric films with blocking layers of Al_2O_3 is a possible route to improve thermal stability and electrical property of high-k gate dielectric stacks on HRSOI wafers.

Compared to HfO_2 gate dielectric, significant improvements in interfacial properties as well as electrical characteristics are found by constructing an $Al_2O_3/HfO_2/Al_2O_3$ dielectric stack by Suh et al. [22]. The measured C-V hysteresis values are 42 mv for both HfO_2 and as low as 15 mv for $Al_2O_3/HfO_2/Al_2O_3$ in the as-deposited states. Upon annealing in N_2 ambient at 500°C, the EOT and the hysteresis values are increased for the HfO_2/GaAs samples, while the $Al_2O_3/HfO_2/Al_2O_3$ samples show far more stable characteristics. For the $Al_2O_3/HfO_2/Al_2O_3$ samples, however, the increase in the EOT value is substantially lower, from 1.4 to 1.6 nm, and no major change in hysteresis is observed after annealing. Since the passivation of the Al_2O_3 layer prevents interfacial oxide and trap charge formation, it aids in reducing the increasing rate of equivalent oxide thickness as well as capacitance-voltage hysteresis.

Typical capacitance-voltage curves of MIS HfO_2 gate dielectric films with a blocking layer of Al_2O_3 inserted between HfO_2 layer and Si layer (HfO_2/Si) capacitors are measured at 1 MHz by Cheng et al. [28]. The negative value of fixed charge perhaps results from the negatively charged Al_3^+ ions with the tetrahedral coordination, which are in contact with the O atoms of HfO_2 and SiO_2. It is indicated that Al atoms diffused into HfO_2 and SiO_2 layer. The improvement of electrical performance is mostly likely because blocking layer prevents the diffusion of Si atoms, keeping interfacial layer composition of SiO_2, and

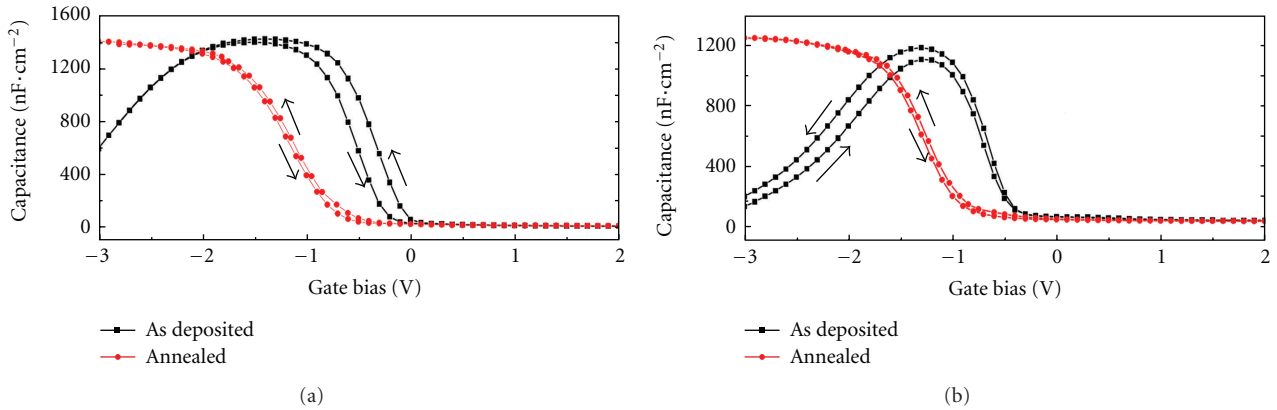

FIGURE 19: Capacitance characteristics of MOS capacitors made of the as-deposited film and the annealed film, respectively: (a) with a blocking layer and (b) without blocking layer [28].

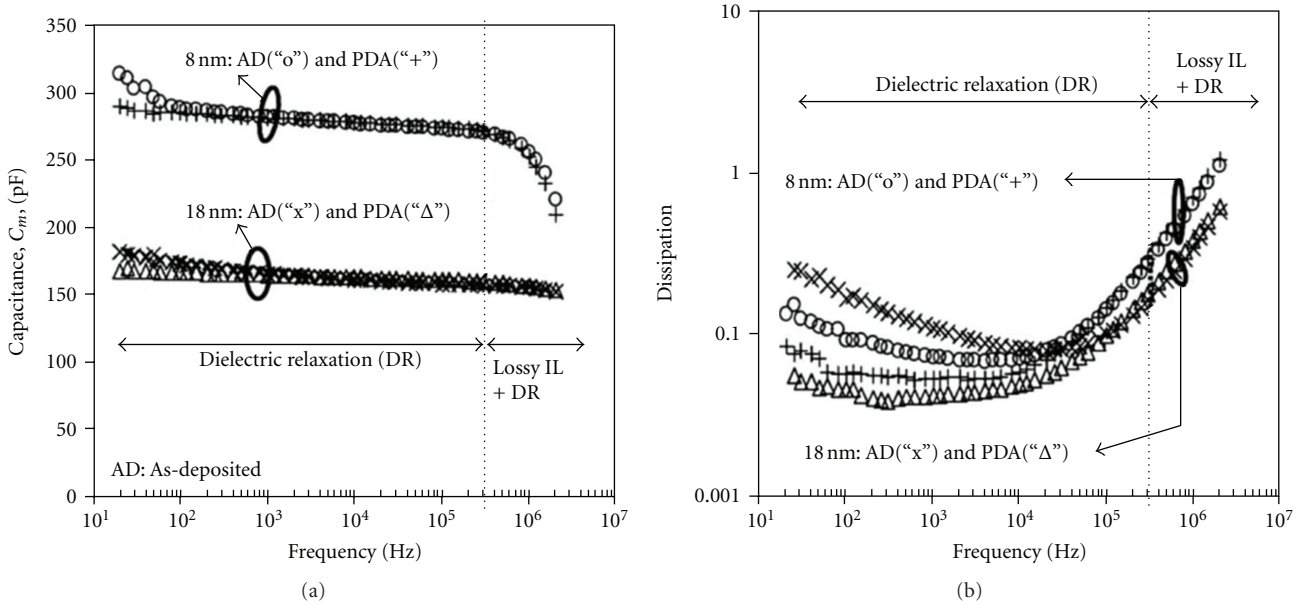

FIGURE 20: Measured capacitance C_m and dissipation for as-deposited and PDA samples against frequency at the strong accumulation region [25].

leading to an optimal SiO_2/Si interface. Therefore, though the annealing treatment increased the thickness of interfacial layer, it also makes the films denser, reducing defect density, and slowed interface state density, leading to a negligible hysteresis and a flat accumulation capacitance region. The result of the electrical measurements indicated that the equivalent oxide thickness decreased to 2.5 nm and the fixed charge density decreased to 4.5×10^{11} Acm^{-2} in comparison with the same thickness of HfO_2 films without the blocking layers. Typical capacitance-voltage (C-V) curves of MIS capacitors are shown in Figure 19. The Al_2O_3 layer effectively prevents the diffusion of Si into HfO_2 film and improves the interfacial and electrical performance of HfO_2.

4.1.3. Doped Hafnium Oxide. HfO_2 is one of the most promising dielectrics for the replacement of SiO_2 in MOSFETs, but it has been found that crystallization occurs at ~ 500°C for pure hafnium. Doping with La increases the crystallization temperature. The electrical properties of the $LaHf_2O_7$ thin films are monitored using high-low-frequency C-V, capacitance-frequency, and current-voltage measurements [25]. In order to perform the C-V, C-f, and I-V measurements, metal gate electrodes are evaporated onto the samples at room temperature to form metal-oxide-semiconductor capacitors (Au/$LaHf_2O_7$/IL/n-Si). Figure 20 shows the change of MOS capacitance dispersion: T against frequency when measured in the strong accumulation region. The measured capacitance consists of two parts: the $LaHf_2O_7$ layer capacitance and interlayer (IL) capacitance. In the higher-frequency range (above 0.3 MHz), as shown in Figure 20, the dispersion became severe for the 8 nm $LaHf_2O_7$ thin film, but not for the 18 nm thicker $LaHf_2O_7$

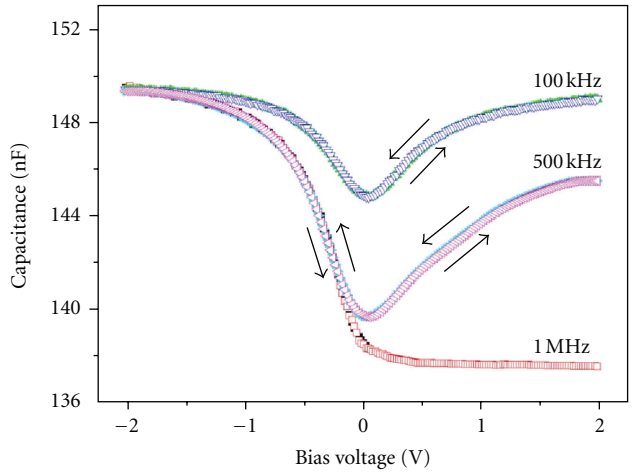

Figure 21: C-V characteristics of YSH film at different test frequencies [33].

film. Therefore, PDA reduces frequency dispersion in the lower-frequency range for oxides with different thicknesses [29]. Crystallization is present in the thicker film revealing that crystallinity is not a necessary factor leading to frequency dispersion or dielectric relaxation, both of which may relate to crystalline grain size.

HfO_2 exhibits a higher permittivity in the cubic ($k \sim 29$) or in the tetragonal ($k \sim 70$) structures than in the monoclinic one. The cubic and tetragonal phases of HfO_2 are metastable at atmospheric pressure and generally require high temperatures to achieve the monoclinic to tetragonal (~1700°C) or tetragonal to cubic (~2700°C) phase transformations. However, the cubic and tetragonal phases of HfO_2 can be stabilized by the addition of yttrium or the lanthanide elements (e.g., La, Gd, Dy, and Er). As-deposited films of $CeHfO_2$ show low hysteresis voltages and negligible flat band voltage shifts [41]. After annealing to form the crystalline cubic or tetragonal phase, the relative permittivity increases from 25 to 32 at 100 kHz. The relative permittivity of 32 is extracted from the accumulation capacitance at 100 kHz, taking into account the presence of a 2.1 nm SiO_2 interlayer. The permittivity of 32 shows an increase from a 25 obtained from the as-grown sample, which is attributed to the transformation from an amorphous to crystalline phase. A k value of 19 is calculated from undoped HfO_2 using the same precursor.

Samples of cubic HfO_2 stabilized with 6 mol% Y_2O_3 (YSH) films were also investigated [33]. The capacitance versus voltage (C-V) curve shown in Figure 21 is measured at various frequencies for the YSH films. A negative flat band voltage about −0.46 V and a very small loop hysteresis are observed in the YSH films, both of which result from the positively trapped charges possibly being related to the oxygen vacancies in the interfacial layer or in the oxide. With various test frequencies, all the samples show frequency dispersion in the depletion region in the C-V curve. This may be attributed to the frequency-dependent polarization, which arises from the traps in the interfacial layer, and the likelihood each interface trap level distributed throughout the Si band gap has a different response time. The film shows a small accumulation variation between 100 kHz, 500 kHz, and 1 MHz, which suggests that the film has a small interface, trapped charge density. The EOT of the YSH films is determined by the capacitance in the accumulation mode from C-V curves. The EOT is equal to 1.1 nm and the effective dielectric constant is up to 27.2. Considering that the dielectric constant of pure HfO_2 is about 22, it is pronounced that the Y_2O_3-doping could increase dielectric permittivity of HfO_2 obviously, despite the fact that Y_2O_3 has a lower value than HfO_2. The leakage current density of the YSH film is 2.02×10^{-4} A/cm^2 at a gate bias voltage of 1 V, while the value derived from the pure HfO_2 film is about 10^{-2} A/cm^2 at the same condition. This structure of the nanocrystals embedded in amorphous oxide has the ability to store some charges. This is probably the reason that the YSH film reveals higher dielectric constant and lower leakage current than that derived from complete crystalline cubic or amorphous monoclinic HfO_2 because of the crucial role of the amorphous film in the insulating properties. All in all, this is an useful approach to control the dielectric properties of hafnium-based oxide films and could be extended to other conditions, such as variable Y_2O_3 content and film deposition method.

Small percentages of dopant elements have been demonstrated to stabilize the cubic fluorite and tetragonal phases of HfO_2, thus enhancing its dielectric constant, which is investigated by Wiemer et al. [34]. The case of Er-doped HfO_2 (Er-HfO_2) is of particular interest since Er has high electronegativity and one of the lowest ionic ratios of the lanthanide series, resulting in a limited tendency to hydroxylation. Incorporation of Er by reactive sputtering (Er ~ 30%) and physical vapor deposition of Er-doped HfO_2 (Er~10–20%) lead to highvalues (~28–30) associated with low EOT and low leakage currents. Er-doped HfO_2 (Er ~ 15%) films may be grown by atomic layer deposition on Si (100). In Er-doped HfO_2, the stabilization of the cubic structure, together with the effect of the high polarizability of $Er3^+$, allows a dielectric constant of ~33 after annealing at 900°C. The insertion of Er within the metallic sublattice of HfO_2 reduces the net density of fixed charges, due to the creation of oxygen vacancies. For similar equivalent oxide thickness, lower leakage currents are measured for Er-doped HfO_2 than for HfO_2. Figure 22 shows the gate leakage current densities of Er-HfO_2 and HfO_2. For similar EOT values, doping with Er decreases the leakage current, due to the increased physical thickness. However, this decrease is not so strong, probably because the oxygen vacancies can serve as traps for Poole-Frenkel conduction.

Doping HfO_x with an appropriate amount of zirconium (Zr) can increase its crystallization temperature, decrease its EOT, lower its leakage current, and improve other electrical properties [49]. A ZrHfO film was deposited on the SiO_2 layer by cosputtering from separate Hf and Zr targets (at 60 and 24 W, resp.) with 13.56 MHz rf magnetron sputtering guns in air/O_2 (1 : 1) at 5 m Torr. The stack has an EOT ~1.7 nm and a flat band voltage ~0.03 V. A high-quality interface layer, such as SiO_2 or SiO_xN_y, between a silicon

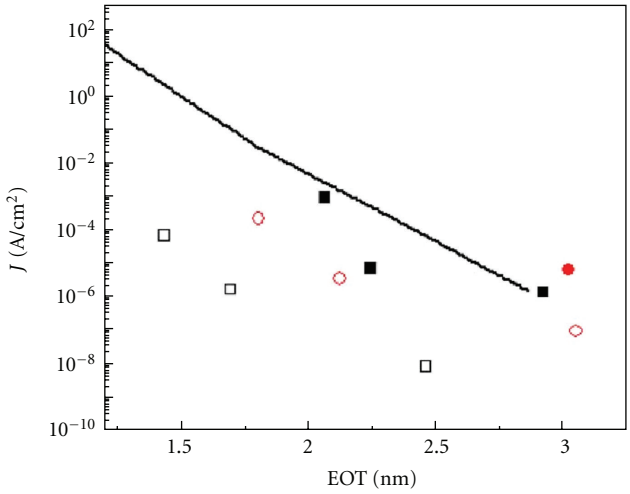

Figure 22: J versus EOT for HfO_2 (circles) and Er-HfO_2 (squares). Open symbols: as-grown, full symbols: annealed at 900°C. The curve for SiO_2 is also displayed [34].

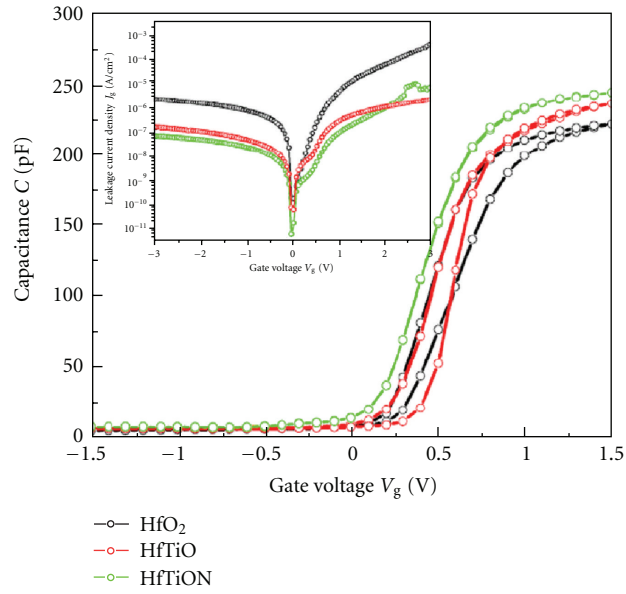

Figure 23: A C-V characteristics of HfO2, HfTiO, and HfTiON gate dielectric MOS capacitors. Inset shows the J_g-V_g characteristics of all the samples [35].

substrate and a high-k film is important to the properties of ultrathin gate dielectrics. However, the failure mode and degradation mechanism of the stacked structure might be different from those of the high-k films alone.

Compared with pure HfO_2, doped HfO_2 with an opti mum concentration of Gd_2O_3 as MOS gate dielectric exhibited a lower leakage current, thinner EOT, and less fixed oxide charges density [50]. The k value of Gd_2O_3 doped HfO_2 can exhibit either increased or decreased trends. When the concentration of Gd_2O_3 is beyond a value, K decreases due to lower k (~20) of Gd_2O_3. Besides, compared with HfO_2, Gd_2O_3-doped HfO_2 samples exhibit a maximum positive shift of flat band voltage ~0.8 V which can be explained by additional fixed charge, due to the Gd doping.

4.1.4. Titanium Incorporation. One of the possibilities to improve an Hf-based dielectric permittivity consists in adding another metal. Recently, Ti is added into the Hf-based dielectrics to achieve a higher k value, remarkable thermal stability, and improve electrical properties [35]. Nitrided HfTiO is been extensively examined and improved thermal stability, and excellent dielectric properties have been obtained when compared to Hf titanate. NO-nitrided HfTiON gate dielectric MOS capacitors show excellent electrical properties and reliability and gives a k value of 18.9. Reduction in the optical band gap by 0.6 eV, with valence- and conduction-band offset decreasing by 0.58 and 0.02 eV, respectively, has been detected. Figure 23 shows typical high-frequency C-V characteristics of HfTiO and HfTiON gate dielectric MOS capacitors. Compared to the undoped HfO_2 samples, HfTiO sample exhibits an increased accumulation capacitance, which can be attributed to the suppressed interfacial layer growth confirmed. For an HfTiON sample, the accumulation capacitance also demonstrates a slight increase compared to that of HfTiO. This is because nitrogen incorporation is favorable for preventing the growth of interlayer and attributes to the improved interface quality. Compared to HfO_2 and HfTiO, the HfTiON sample has the smallest positive flat band shift, corresponding to least negative oxide charges, which can come from either singly and doubly negatively charged interstitial oxygen atoms, or broken Hf–O bonds localized at the O atoms. As a result, the improved C-V characteristics and reduced leakage current have been achieved from HfTiON gate dielectric MOS capacitor attributed to the nitrogen-induced reduction in oxygen-related traps and the improved interface quality. In spite of the nitrogen-induced reduction in the band offset, the sufficient barrier height still makes sputtering-derived HfTiON films promising high-k gate dielectric candidates taking advantage of the improved physical and electrical performance.

4.1.5. Hf-Si Mixed Oxide. HfSiO(N) has been considered as one of the most promising candidates because of its wide band gap, thermal stability, and suppression effects of boron penetration and crystallization [51]. However, there remain critical issues to be solved in metal/high-k systems, for instance, to control the threshold voltage after high-temperature thermal annealing performed for dopant activation. Since threshold voltage for CMOS devices can be tuned by such insertion of La and Al oxide in the high-k layer, the development of guidelines for control of effective work functions is demanded. In order to design device structures of optimum threshold voltage, it is necessary to understand the chemical states and electronic structures at the high-k/SiO_2 interfacial layer after high-temperature annealing processes.

A stable SiO_2/HfSiO:N/WSi_x/poly stack after a 1050°C spike junction annealing, with an EOT around 1.2 nm and a two-decade reduction in leakage current as compared to SiO_2

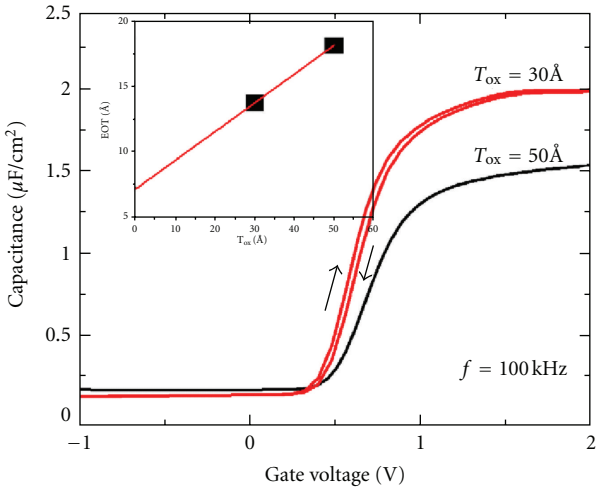

FIGURE 24: Capacitance-voltage (C-V) characteristics at a frequency of 100 kHz and the EOT-T_{ox} plot (inset) to extract the permittivity (17.7) of $HfSiO_2$ and electrical thickness (7 Å) of the interfacial oxide [36]. The equivalent oxide thicknesses (EOTs) of $HfSiO_2$ are calculated to be 13 Å and 18 Å for the physical oxide thicknesses (T_{ox}) of 30 Å and 50 Å, respectively. The thickness of the interfacial layer extrapolated from the intercept in the inset is 7 Å.

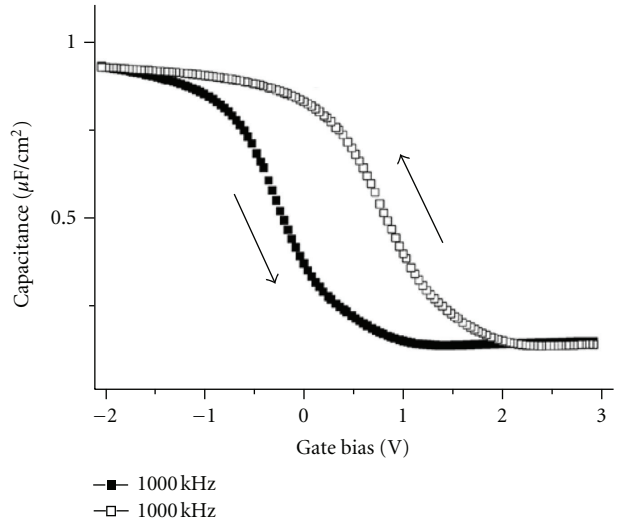

FIGURE 25: C-V hysteresis characteristics for the HfO_2/p-Ge(100) [37].

dielectric, is introduced by Gassilloud et al. [52]. A nominal ~1.2 nm EOT is indeed obtained on 0.8 nm SiO_2/2.3 nm HfSiO:N (700°C postnitridation annealing) by depositing the optimized WSi_x 3 recipe. The leakage current can be drastically improved after high-temperature postnitridation annealing (1050°C spike) with a reduction in leakage current of approximately two orders of magnitude ($\times 10^{-2}$). Besides, the low leakage current ($\times 10^{-2}$) is maintained when TiN intercalation layer is removed (WSi_x/polysilicon stack), whereas a slight degradation of EOT (<0.1 nm) is observed.

Fully strained $Si_{0.75}Ge_{0.25}$ MOS capacitors with $HfSiO_2$ high-k gate dielectric and TaN metal gate have been fabricated on Si substrates [36]. $HfSiO_2$ high-k gate dielectrics exhibit an equivalent oxide thickness of 13–18 nm with a permittivity of 17.7 and gate leakage current density lower than SiO_2 gate oxides by >100. Figure 24 shows C-V characteristics of MOS capacitors with $HfSiO_2$ gate dielectrics deposited on fully strained $Si_{0.75}Ge_{0.25}$ epitaxial films. The permittivity of the interfacial oxide is ~5.5. The C-V hysteresis of 30 mV is measured for 3 nm $HfSiO_2$ at a frequency of 100 kHz. Low interface trap of $\sim 4 \times 10^2/cm^2$ is extracted using charge pumping method from transistors with identical gate stack of $HfSiO_2$/SiGe. In SiGe MOS capacitors with high-k $HfSiO_2$ dielectrics, the interfacial oxide consists primarily of SiO_2. The high-k $HfSiO_2$ dielectrics exhibit excellent C-V characteristics with an EOT of 1.3 nm which are sufficient for implementing high mobility MOSFETs using compressively strained SiGe channels in future CMOS technology.

4.1.6. Germanium Substrates. Germanium has been introduced as channel material due to its high mobility for both electron and holes as compared to silicon. It is found that for suitable future scaling, a dielectric with K over 40 is preferred [37]. The bulk rutile crystalline phase of TiO_2 exhibiting very high-k value of 80 makes it a promising candidates for gate dielectric. Proper passivation of the Ge surface is required before it can be used as a channel material. TiO_2 grown by PE-ALD exhibited a k value of 50 ± 5. An EOT of 0.9 nm is obtained for the TiO_2(3 nm)/HfO_2(1.2 nm)/GeO_2 (0.7 nm)/Ge capacitor with very low leakage current density of 2×10^{-7} Acm^{-2} at the flat band voltage equal to 1 V. Very high leakage current is observed for the TiO_2/Ge capacitors, which is consistent with low conduction band offset for TiO_2 with respect to Ge. Well-behaved C-V curves are observed for all the capacitors without significant frequency dispersion, stretch-out, or bumps in the depletion region. The C-V characteristics also show evidence of inversion with a minority carrier response at low frequency and a flat minimum capacitance at high frequency. This indicates the efficient electrical passivation of the Ge interface. The C-V hysteresis characteristics for the Pt-gated MOS capacitances without and with O_2 plasma passivation are shown in Figure 25. Very large C-V hysteresis about 900 mV is observed for the capacitors without passivation while significantly reduced hysteresis below 30 mV is obtained for the capacitors with O_2 plasma passivation. The hysteresis is caused by the intermixing of GeO_x and HfO_2. By using O_2 plasma pretreatment directly prior to ALD process, a uniform and stable GeO_2 IL is created due to the high reactivity of O radicals and also the absence of air break in between the passivation and ALD process. C-V hysteresis is below 30 mV for the TiO_2/HfO_2/GeO_2/Ge capacitors. Relatively low minimum density of interface states about 5×10^{11} eV^{-1} m^{-2} is obtained, suggesting the potential of HfO_2/GeO_2 passivation layer for the application of TiO_2 as gate dielectric for both p- and n-type Ge channels.

High-carrier-mobility Ge- and SiGe-based MOSFET with high-k gate dielectrics have been extensively studied to further scale down the size of the devices while increasing

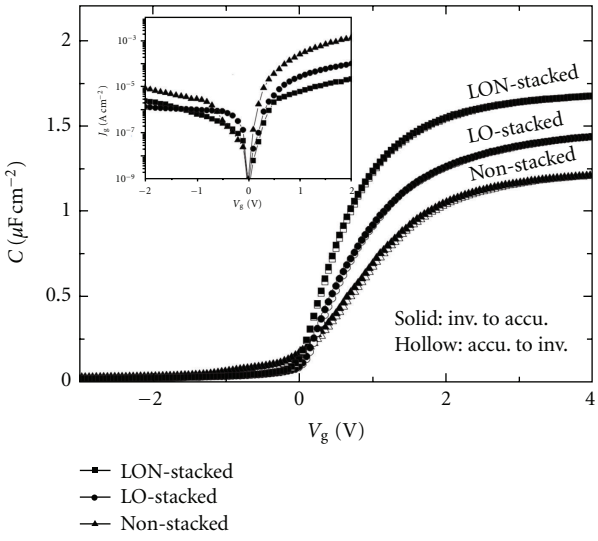

Figure 26: HF C-V curve for the LON-stacked, LO-stacked, and nonstacked samples [38]. The inset shows their gate-leakage current versus gate voltage.

their operating speed. However, the parasitically grown unstable low-k Ge oxide (GeO_x) at the HfO_2/Ge interface and Ge diffusion into HfO_2 film cause degradation of the gate dielectric, thus deteriorating the device performances. More recently, rare-earth metal oxides have attracted attention as another class of materials which offered good passivation of Ge because the rare-earth metal oxides reacted strongly with Ge to form stable interfacial layer. La_2O_3 is another rare-earth metal oxide which exhibited better interface quality with Ge and larger band gap (~5.5 eV). Furthermore, its nitride (LaON) exhibited better thermal stability than La_2O_3 on Si and could suppress the out-diffusion of Si. Better electrical characteristics can be achieved for Ge MOS device with HfO_2/LaON stack gate dielectric than its counterpart with HfO_2/La_2O_3 stack gate dielectric [38]. Stacked gate dielectrics of HfO_2/LaON and HfO_2/La_2O_3 are also deposited by sputtering LaON or La_2O_3 (1 nm nominal thickness based on precalibrated deposition rate) on Ge substrate as interlayer, followed by the deposition of a HfO_2 layer (~9 nm) by sputtering an Hf target at a power of 25 W in air and O_2 (denoted as LON-stacked and LO-stacked samples, resp.). The C-V curves of both LON and LO samples are smooth and have very small hysteresis, indicating negligible slow rates in the dielectric and near the interface. It is also noteworthy that a buffer layer (LaAlO) seems to be formed between the Al gate and La_2O_3 dielectric, which agrees with observation and has a bad effect on the k value. Obviously, the slope of C-V curve in the deletion region for the two stacked samples which is shown in Figure 26 is much larger than that of the nonstacked samples, indicating less interfacial traps created. For the LON-stacked sample, this could be explained by the fact that LaON has good interface properties with Ge, and furthermore, LaON can act as a barrier layer against Ge out-diffusion or O and Hf in-diffusions, thus suppressing generation of interfacial defects. The LON-stacked samples exhibit the smallest interface-state density and thus best interface quality. Negative oxide charge density of the LO-stacked and nonstacked samples should mainly result from Ge diffusion into the dielectric plus large interface-state density while negative oxide charge density of the LON-stacked sample should be mainly attributed to acceptor-like interface states. It is found that the LON-stacked samples have the largest k value of 19.2 due to suppressed growth of low-k GeO interlayer and the larger k value of LaON itself. The LON-stacked and nonstacked samples have the smallest and largest gate leakage current, respectively.

The electron properties and high-field reliability of HfTa-based gate dielectric MOS devices with and without AlON interlayer on Ge substrate are investigated by Xu et al. [62]. The MOS capacitor with HfTaON/AlON stack gate dielectric exhibits low interface state/oxide-charge densities, low gate leakage, small CET about 1.1 nm, and high dielectric constant about 20. Distortion is observed in the region from depletion to inversion of the C-V curves for the two samples without the AlON interlayer but does not exist for the two samples with AlON interlayer. This difference is obviously associated with the AlON interlayer. For the HfTaO samples, significant interfacial defects are probably created due to formation of GeO_x or strong interdiffusion and reaction between the HfTaO dielectric and Ge substrate due to the absence of AlON interlayer, which is illustrated to some extent by the rough interface. All of these should be attributed to the blocking role of the ultrathin AlON interlayer against inter-diffusions of Ge, Hf, and Ta and penetration of O into Ge substrate, with the latter effectively suppressing the unintentional formation of unstable poor quality low k GeO_x and giving a superior AlON/Ge interface. Moreover, incorporation of N into both the interlayer and high-k dielectric further improves the device reliability under high field stress through the formation of strong N-related bonds.

Although Ge is in the same group as Si, its native oxide is unstable and water soluble. As a result, high-k dielectric materials such as HfO_2, ZrO_2, and HfTaON are used as the gate dielectric of Ge MOS devices. Ge p-MOS capacitors with HfTiON gate dielectric are deposited by sputtering method by Li et al. [39]. Predeposition fluorine plasma treatment and postdeposition fluorine plasma annealing are implemented to improve the electrical and reliability properties of Ge p-MOS capacitors. Figure 27 shows the high-frequency C-V curve for the samples. It is clearly shown that the accumulation capacitance of the Post-F sample is slightly larger than the control sample due to suppressed GeO_x growth during the postdeposition annealing by F incorporation. This is because fluorine with higher electronegativity than oxygen is a good passivant for defects at the high-k/Ge interface, thus suppressing the growth of GeO_x. The interface quality with lower interface-state density and less frequency dispersion is improved, and also reliability properties with smaller increases of oxide charge and gate leakage after high-field stressing are enhanced. Compared with predeposition fluorine-plasma treatment, postdeposition fluorine plasma annealing achieves higher quality of high-k/Ge interface such

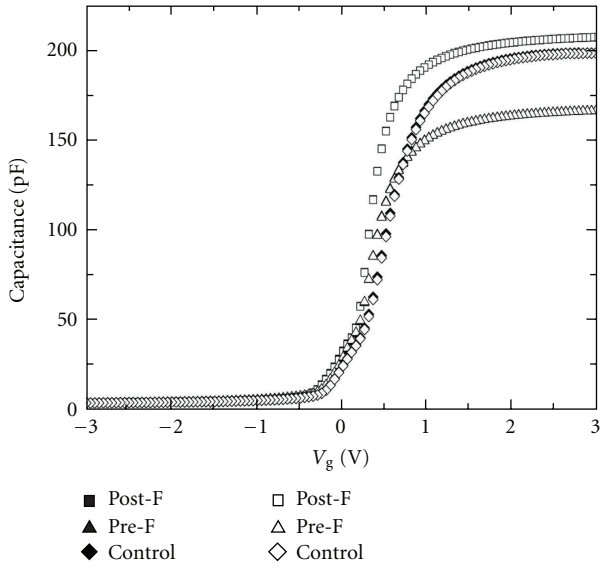

Figure 27: High-frequency (1 MHz) C-V curve of the Ge MOS capacitors swept in two directions (solid for depletion to accumulation; open for accumulation to depletion) [39].

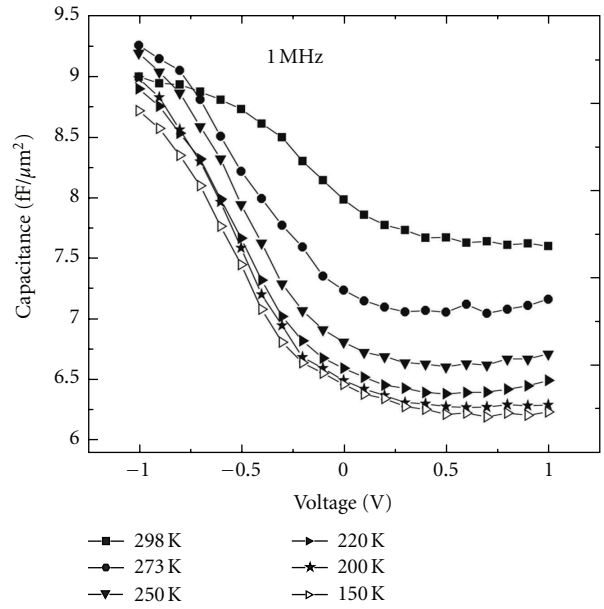

Figure 28: C-V characteristics at different temperatures at 1 MHz frequency for TiAu/HfO_2/GaAs samples [53].

as lower interface-state density, higher dielectric constant, and lower-stress-induced gate leakage current, which is due to fluorine passivation effects of both the oxygen vacancies in the dielectric and the dangling bonds at the Ge surface.

4.1.7. Gallium Arsenide. Gallium arsenide (GaAs) channels of MOS transistor are being considered for their high electron mobility [53]. However, HfO_2/GaAs interface properties seem to limit the performance of transistors because of formation of a poor quality interfacial layer. The interface layer leads to an increased concentration of interface states. The nature and properties of these interface states, therefore, needs to be understood such that the interface quality can be improved. It is further required to understand the types of traps and their position in the band gap and their interaction with carriers. Use of low temperature in the range of 298–150 K allows evaluating the nature of the interface defects and their relative energy levels. The interface defect response at the high-k and GaAs interface using TiAu/high-k/GaAs MOS capacitor is evaluated at low temperature. The interface behavior of the metal/high-k/p-GaAs is analyzed using C-V, I-V, and conductance measurements. The C-V characteristics as function of temperature at 1 MHz frequency for TiAu/HfO_2/GaAs samples are shown in Figure 28. It is clearly visible that in case of 1 MHz frequency as temperature is decreased from 298 to 150 K, the inversion capacitance decreases due to an increase in time constant of the interface traps. The difference therefore is due to interface trap capacitance. The characteristics of TiAu/high-k/GaAs samples suggest that the defect-enhanced trap time constant increases as the temperature decreases and only fast interface states take part on the conduction process at low temperatures. As detrapping time increases for interface traps within the semiconductor band gap, the inversion capacitance decreases with temperature. Characteristics such as leakage current density and interface state density for two different gate metals suggest that metal HfO_2 interaction plays a role in determining the quality of dielectric and their interface.

4.2. Zr-Based Gate Oxide Dielectrics

4.2.1. Zirconium Oxide. To increase the gate capacitance within the allowable gate leakage current for sub-100 nm CMOS technology, replacement of conventional SiO_2 or Si oxynitride-based gate dielectrics is imminent. From the applications point of view, the thermal stability and interfacial properties of ZrO_2 make it an attractive candidate since it has a high dielectric constant (k = 15–22), high breakdown field (15–20 MV/cm), and a large band gap (5–7 eV). Ultrathin ZrO_2 films have been fabricated at room temperature using zirconium tetra-tert but oxide on strained-Si heterolayers by microwave PECVD system by Bera et al. [54]. Interfacial and electrical properties of Al/ZrO_2/strained-Si MOS capacitors have been characterized via C-V, which is shown in Figure 29 and C-V techniques. The C-V characteristics exhibit frequency dependence due to presence of interface traps in the ZrO_2/strained-Si interface. Continuum trap model is implemented in modeling of strained-Si/ZrO_2 MOS capacitors. The interface trap density and corresponding time constant have been determined using the conductance method.

4.2.2. Doped Zirconium Oxide. Zirconia has attracted much interest as an alternative high-k material due to its high dielectric constant (~25), wide energy band gap (~5 eV), and good mechanical and chemical stability on Si. However, ZrO_2 is not completely chemically or thermally stable on

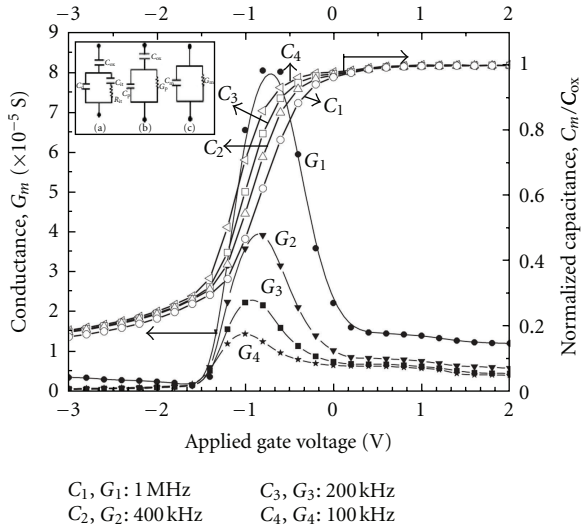

Figure 29: High-frequency C-V and G-V characteristics of as-deposited ZrO_2, in the inset equivalent circuit diagram of strained-Si/ZrO_2/Al structure for conductance measurements [54].

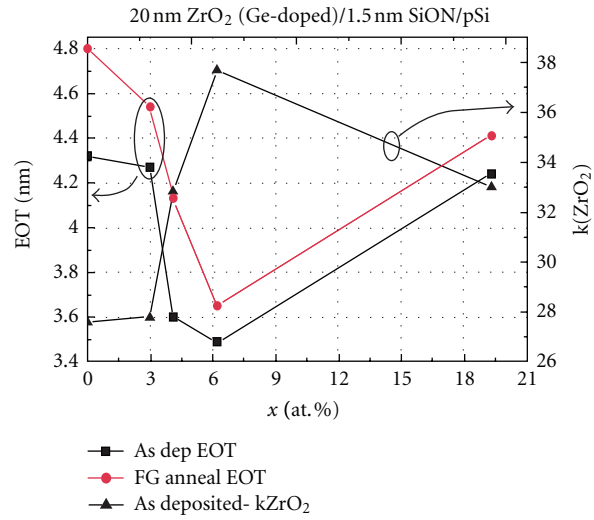

Figure 30: EOT and k values determined form the C-V curves in the accumulation capacitance mode as functions of Ge content (x) for the as-deposited and after forming gas-annealed ZrO_2 samples [55].

silicon, which crystallizes at relatively low temperatures (~400–500°C) leading to current leakage along the polycrystalline grain boundaries and promotes the formation of a lower permittivity SiO_2 layer during the high temperatures (~900°C) involved in CMOS processing. One solution is to deposit a mixed oxide film, which remains amorphous up to high temperature (~800–900°C), leading to reduced leakage currents, and inhibits the formation of the SiO_2 interlayer [63]. Thin films of lanthanum zirconium oxide, $La_xZr_{1-x}O2$ deposited, show good dielectric properties with low hysteresis voltages and negligible flat band voltage shifts. The relative permittivity k ranged from 11 to 14 with leakage current densities at 1 MV cm^{-1} in the range from 2.6×10^{-6} to 5.3×10^{-7} Acm^{-2}. Concerning $LaZrO_2$ and $CeHfO_2$ thin films [43], Au contacts are deposited onto the films to form MOS capacitors and backside Al contacts are deposited to allow electrical characterization for high- to low-frequency C-V, and C-f measurements. The undoped ZrO_2 and HfO_2 films show a small frequency dispersion and substantially large frequency dispersion is found during C-V measurements on the annealed sample of $CeHfO_2$ thin films. The level of enhancement is firmly associated to the doping level. The highest dielectric constants are observed with lightly doped films, with a doping level of around 10% for both material samples. Dielectric constants of 39 and 33 are calculated for $LaZrO_2$ films and $CeHfO_2$ films.

The dielectric permittivity of the Ge-doped ZrO_2 thin films shows pronounced correlation with the structure details of the oxide film and is increasing with Ge content to a maximum value of 37.7, which is obtained for 6.2% at Ge-doped sample grown at 225°C [55]. Figure 30 shows the variation of EOT and ZrO_2 k values versus Ge content for the as-deposited and forming gas-annealed samples. The k value increases as the Ge content increases up to 6.2 at. % and then further decreases up to 19.3 at. %. This increase is attributed to the coexistence of the monoclinic and tetragonal zirconia phases in the deposited oxide. By doping ZrO_2 films with Ge, the k value increases and reaches its maximum value of 37.7 ± 2 for $x = 6.2$ at. %. The dielectric permittivity enhancement upon doping is attributed to the increase in ZrO_2 with very high-k value at low deposition temperatures and with excellent thermal stability could be beneficial for the integration of this dielectric in scaled devices requiring low equivalent oxide thickness.

The electronic availability of ZnO thin films, which serve as a semiconductor material for MOS capacitors with HfO_2 gate dielectric, is investigated [64]. High-frequency (1 MHz) C-V and I-V characteristics of ZnO-based MOS capacitors are researched. The leakage current is about 1.7×10^{-6} A as gate voltage is 1 V; this is a low leakage current due to good quality of HfO_2 thin films. Good electrical characteristics can be obtained on ZnO substrates with high-k HfO_2 gate dielectrics. The ZnO capacitors can exhibit high thermal and electronic stabilities. The EOT of HfO_2 gate dielectrics measured by the C-V method is about 4 nm. I-V and C-V characterizations have shown that the HfO_2 thin films have low leakage current density and high dielectric constant. ZnO MOS capacitors with HfO_2 gate dielectric have good thermal and electronic stabilities. The smooth HfO_2 gate dielectric surface and small trap state densities near the gate dielectric/channel interface are primary reasons for high thermal and electronic stabilities of ZnO MOS capacitors.

4.2.3. Germanium Substrate. As alternative to Si in high-speed logic devices, Ge is widely considered due to its higher carrier motilities [65]. High dielectric constant material is a promising strategy for ultra-scaled logic devices with coupling Ge channel. Among high-k oxides, ZrO_2 has been proved to be a promising insulator. La-doped ZrO_2 thin films grown by O_3-based atomic layer deposition directly on

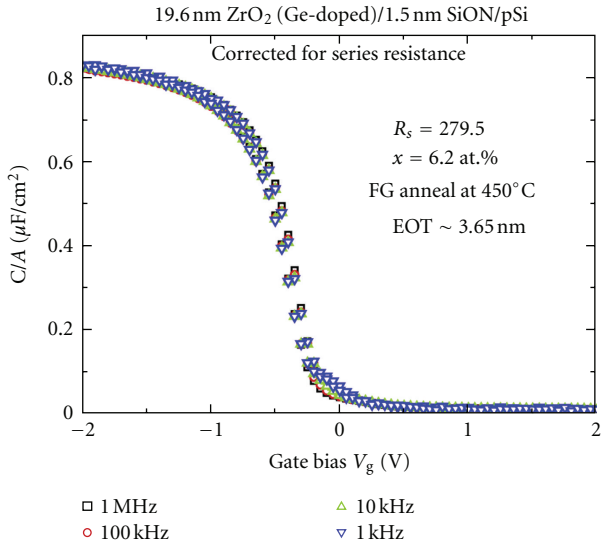

Figure 31: Selected C-V curves of $Pt/ZrO_2/SiON/Si$ capacitors with ZrO_2 dielectric doped with 6.2 at.% Ge and forming gas annealed at 450°C for 20 min [56].

Ge(100) exhibit a dielectric constant of 29. Combination of a direct O_3-based ALD of La-ZrO_2 and RTA can lead to a k of 40 presented. It is proved that Ge atoms are supplied by the substrate and penetrate into the oxide upon annealing. Only weak-frequency dispersion is observed in both accumulation and depletion, indicating a relatively low interface density ($\sim 8 \pm 1 \times 10^{11}$ eV^{-1} m^{-2} evaluated with the Hill-Coleman method at 500 kHz). A clockwise hysteresis of 550 (as-grown) and 850 (annealed) mV is measured. C-V curves appear more stretched and only a moderate increase of the interface density up to $\sim 2 \pm 1 \times 10^{12}$ eV^{-1} cm^{-2} is observed. Ge diffusion occurs without affecting the interfacial details qualified by a germanate-like region and an acceptably low interface density value.

Intentional doping of Ge into ZrO_2 at low deposition temperatures (225°C) leads to a k value enhancement allowing physical thickening of the dielectric [56]. A maximum k value of 37.7 can be obtained at low Ge concentrations (6.2 at %). ZrO_2 and Ge-doped ZrO_2 films are prepared, in an MBE chamber, by atomic oxygen beam deposition on SiON/pSi and $LaGeO_x$/Ge substrates at 225°C. Both types of substrates are chemically stable upon ZrO_2 deposition. Structural analysis shows that the permittivity enhancement can be explained by the increase of the tetragonal distortion upon Ge doping. Figure 31 depicts C-V curves for a MOS capacitor from the forming gas-annealed Ge-doped ZrO_2 film (x = 6.2 at.%) taking into account the series resistance correction. It is shown that the capacitor has good electrical characteristics in terms of hysteresis, frequency dispersion and stretch-out, allowing for a reliable estimation of k-value assuming a nominal SiON interface layer thickness of 1.5 nm.

Ultrathin ZrO_2/La_2O_3 high-k dielectric stacks by ALD on germanium substrates have been formed [66]. Interfacial layer-free oxide stacks with a relative dielectric constant of 21 and equivalent oxide thickness values as low as 0.5 nm are obtained. Metal oxide semiconductor capacitors with platinum as the gate electrode exhibit well-behaved C-V characteristics. Well-behaved C-V characteristics with no significant hysteresis are obtained. The thicker oxides show almost no frequency dispersion, except a frequency-dependent flat band shift, which originates from the interface traps and may be a consequence of a weak Fermi level pinning. The leakage current densities in the range of 0.01–1 A/cm^2 as well as the interface density in the range of $\sim 3 \times 10^{12}$ eV^{-1} cm^{-2} are very encouraging in view to a proper field effect operation. These results strongly recommend ZrO_2/La_2O_3 dielectrics fabricated by this approach for future Ge-based MOS technology.

The application of these usually heterogeneous oxides opens the way to reconsider other semiconductors with intrinsically higher carrier motilities—as, for instance, germanium (Ge)—for the use in integrated circuits. However, a major technological drawback to the use of Ge is the difficulty to passivate its surface or—in other words—to minimize the interface trap density. La_2O_3 is mainly deposited in combination with a second high-k oxide, like Al_2O_3, HfO_2, or ZrO_2. Addressing the ALD of La_2O_3 on Si, promising results have been shown for the growth of $LaAlO_3$ and HfO_2/La_2O_3 stacks, by using tris-lanthanum in combination with water and with ozone, respectively. Summarizing the C-V measurements of ZrO_2/La_2O_3 film [27], the following observations are made independently of the applied annealing gas atmosphere: (1) no distinctive change of the oxide capacitance and hence of the resulting EOT during PDA at 400°C, (2) an increase of capacitance of the oxide and hence a decrease of EOT in the order of 0–20% during PDA at 500°C, and (3) a distinctive charge of the oxide capacitance and hence a decrease of EOT in the order of 50–60% during PDA at the 600°C for ZrO_2 thickness of greater than 5 to 6 nm. From the slope of the linear fits we obtain a relative dielectric constant k of 24 ± 2 for as-deposited stacks and 35 ± 2 for stacks annealed at 500°C in $N_2 : H_2$ = 90 : 10. The adequate processing leads to very high-k dielectrics with EOT values below 1 nm, leakage current densities in the range of 0.01 A/cm^2, and interface trap densities in the range of from 2 to 5 × 10^{12} eV^{-1} cm^{-2}. C-V measurements of two different MOS capacitors are compared on high frequency (50 kHz and 500 kHz) before and after PDA at 600°C. In the case of a type II stack (~6 nm of ZrO_2), a pronounced increase of the oxide capacitance and hence a decrease of the resulting EOT after the PDA can be observed, whereas in the case of a type I stack (~1 nm of ZrO_2), the opposite behaviour is shown.

4.2.4. Zr-Hf and Zr-Si Mixed Oxide. Hf-Zr mixed high-k oxide films obtained by the oxidation and annealing of multilayered metal films show the improved dielectric constant (k) and the raised crystallization temperature [57]. Comparing with HfO_2 and ZrO_2 gate dielectric, the crystallization temperature of Hf-Zr mixed oxides is raised by more than 200°C. Zr oxide has more fully oxidized stoichiometry than Hf oxide, irrespective of annealing temperatures using

AES and XPS. The thickness of an interfacial layer located between Hf-Zr mixed oxide and Si substrate also increases as annealing temperature increases. Especially, the thin SiO_x interfacial layer starts to form if annealing temperature increases over 700°C, deteriorating the equivalent oxide thickness. Two distinctive amorphous layers are formed: Hf-Zr mixed oxide is formed on top of the silicate. The thickness of silicate layer and therefore EOT value are dependent on annealing temperature. In Figure 32, the C-V curve of the only oxidation sample (i.e., closed squares) results in a hysteresis window, which is known to be caused by the incomplete oxidation of Hf or Zr metal atoms. We believe that the metallic bonds which have not been fully oxidized are repaired during the annealing process, so that the hysteresis window disappears. The data shown in Figure 33 also indicate that the accumulation capacitance decreases as the annealing temperature increases. This phenomenon can be explained by the formation of the SiO_x layer due to the high-temperature annealing over 700°C. The negatively charged defects located in the oxidation only samples are reduced by the annealing process, causing the flat-band voltage shift toward the negative gate voltage. The shift of flat-band voltage toward the negative voltage through the reduction of negatively charged defects by annealing is also observed in Zr-based gate dielectrics.

ZrSiO films with higher Zr concentration suffered the phase separation to precipitate ZrO_2 and form the interfacial layer with a lower dielectric constant with Si substrate [26]. The good thermal stability of $(ZrO2)_{0.5}(SiO2)_{0.5}$ film is also shown by the C-V curve. The Zr-Si-O film with the bilayer structure $(ZrO2)_{0.7}(SiO2)_{0.3}/(ZrO2)_{0.5}(SiO2)_{0.5}$/Si shows the lowest EOT and the good quality of the interface. The electrical properties show that the bilayer ZrSiO film is of the lowest equivalent oxide thickness and good interface with Si substrate.

4.3. Aluminate Dielectrics

4.3.1. Aluminum Oxide. Intensive research efforts are currently going on to develop MOS transistors formed on high-mobility III-V channel materials to extend the CMOS technology beyond this limit along the line of the so-called "More Moore" approach on the Si platform. The key point is realization of high-performance high-k MOS gate stacks on III-V materials. As the surfaces of III-V materials are known to be very difficult to passivate due to strong tendency of Fermi level pinning at insulator-semiconductor interfaces, therefore, a new method of direct deposition of high-k insulators such as Al_2O_3 on III-V semiconductors has recently become a popular solution. As compared with the MIS structures without Si interface control layer, high-k Al_2O_3 MOS structure with the Si interface control layer [68] improved the electrical interface quality, a great deal for both GaAs and InGaAs, reducing frequency dispersion of capacitance, hysteresis effect, and interface state density. A minimum value of interface state density of $2 \times 10^{11}\,eV^{-1}\,cm^{-2}$ is achieved for both GaAs and InGaAs. However, the range of bias-induced surface potential excursion within the band gap is very different,

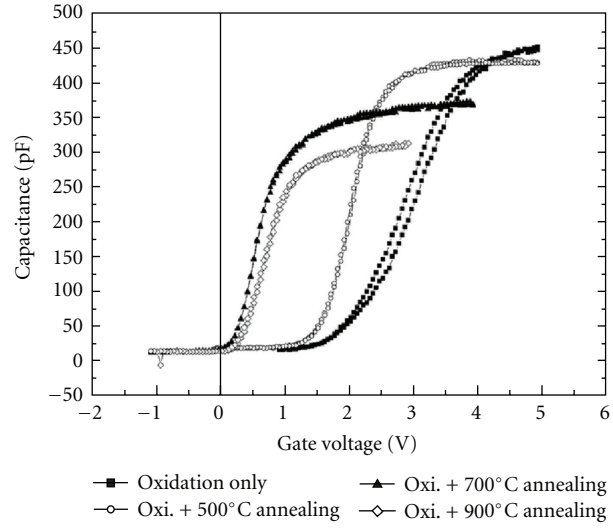

Figure 32: HF C-V curves of the samples oxidized at 500°C in furnace followed by annealing at various temperatures in RTP. Note that the capacitance value reduces as the annealing temperature increases. No hysteresis phenomenon is observed when Hf-Zr mixed oxide films are annealed [57].

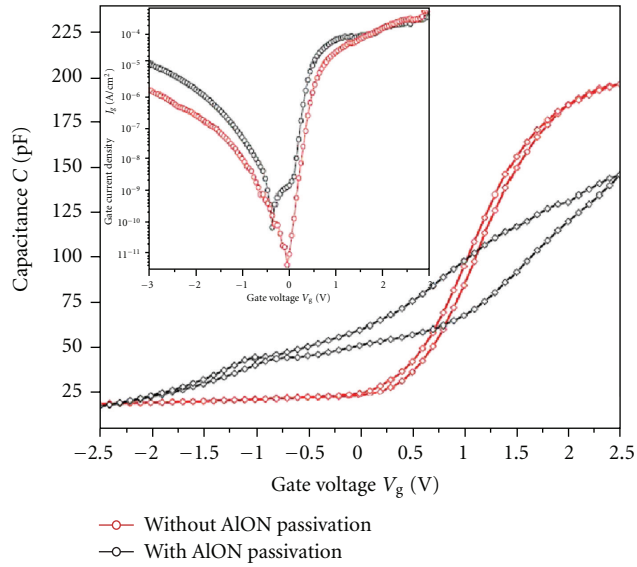

Figure 33: C-V characteristics of GaAs p-MOS capacitors with and without interfacial passivation [58].

making formation of electron layer by surface inversion possible in InGaAs, but not possible in GaAs. The difference is explained by the disorder-induced gap state model. It is found that all the capacitors with RONs on ALD Al_2O_3 films by magnetic sputtering and PDA exhibit much larger hysteresis window than those without any nanodots for a gate sweeping voltage range of −5 V to +5 V [44]. This reveals that the embedded RONs cause remarkable memory effects. The C-V characteristics of the GaAs MOS diodes having ALD Al_2O_3/GaAs and ALD Al_2O_3/Si interface control layer/GaAs interfaces are compared. The resulting

C-V hysteresis window and effective injected charge density exhibit significant dependence on the configuration in the case of low gate voltage, but become approximately equal for high gate voltage, but become approximately equal for high gate voltage. This is due to the different tunneling barriers associated with the direct tunneling mechanism dominating under low gate voltage and the Fowler-Nordheim tunneling mechanism under high gate voltage. It is seen that the charge injection occurs dominantly at initial programming and erasing stages; for instance, the injection speeds of charges are close to $1.3 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{us}^{-1}$ and $1.0 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{us}^{-1}$ in the case of 5~10 s programming and erasing time, respectively. A memory window as large as 3.7 V is achieved for programming/erasing at a low voltage of ±7 V for 0.1 ms. At the same time, superior charge retention characteristics are observed.

$In_xGa_{1-x}As$ III-V compound semiconductor MOSFETs have become a popular topic recently due to the higher drift velocity and lower effective mass of the $In_xGa_{1-x}As$ materials [47]. $In_xGa_{1-x}As$ materials have great potential to meet the high-performance requirements due to their high mobility in comparison with silicon. However, the major problem using of III-V compound semiconductor devices for low-power logic application is the lack of high-quality high-k dielectric with low interface trap density. Al_2O_3 gate dielectric has high band gap energy about 9 eV, high breakdown field from 5 to 10 MV/cm, high dielectric constant from 8.6 to 10, and high thermal stability up to at least 1000°C; also it remains amorphous under typical process conditions. The C-V and J_g-V_g characteristics of ALD $Al_2O_3/In_xGa_{1-x}As$ /n^+-InP heterostructure with different In contents of 0.53, 0.7, and 1.0 are presented. From C-V measurement results, the inversion of the MOS capacitor increases efficiently with In content. A strong inversion for Al_2O_3/InAs capacitor is observed even at 1 MHz ac signal due to the higher drift velocity and the shorter minority response time of InAs compared to $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$. The ALD $Al_2O_3/In_xGa_{1-x}As$ capacitors also show very low gate leakage current density in the 10^{-8} A/cm^2 range which demonstrates a low trap density inside ALD Al_2O_3 dielectric. Overall, these results indicate that Al_2O_3/InAs capacitor which has high inversion charge density with low leakage current is an attractive candidate for high-performance low-power logic device applications.

4.3.2. Doped Aluminate. The lanthanide aluminates, $MAlO_3$ (M = La, Pr, Gd, Nd, etc.), are promising high-k materials, as they combine the advantages of the high permittivity of the lanthanide oxide with the chemical and thermal stability of Al_2O_3. Furthermore, they remain amorphous up to high temperatures (e.g., $LaAlO_x$ remains amorphous up to 850°C), leading to a large reduction in leakage current relative to polycrystalline M_2O_3 films and to inhibition of the growth of a SiO_2 interfacial layer during CMOS processing [46]. The electrical properties of the praseodymium aluminate ($PrAlO_x$) and neodymium aluminate ($NdAlO_x$) films are assessed using C-V and I-V on MOS capacitors. Excellent electrical characteristics are obtained after annealing treatment, as seen by the low hysteresis, near-ideal flat band voltage (−0.58 V), and a low interface state density. A positively directed flat band voltage shift is found in this figure, which corresponds to a reduction of fixed positive charges in the oxide layer. Postmetallization annealing in forming gas is effective in reducing charge levels in all films. Following postmetallization annealing, the dielectric properties of $NdAlO_x$ are superior to those of $PrAlO_x$, and MOSCs fabricated with $NdAl_xO_y$ (Nd/Al ~ 0.87) and $PrAlO_x$ (Pr/Al ~ 0.76) show leakage current densities below $7.5 \times 10^{-10}\,\mathrm{Acm}^{-2}$ ($k \sim 14$) and $1 \times 10^{-6}\,\mathrm{Acm}^{-2}$ ($k \sim 12$), respectively.

A charge trapping memory device using $Ti_{0.2}Al_{0.8}O_x$ film as charge trapping layer and amorphous Al_2O_3 as the tunneling and blocking layers is fabricated for nonvolatile memory applications [69]. Compared with the traditional charge trapping layers, employing high-k dielectric allows a higher electric field over the tunneling layer due to electric flux density continuity and results in modified Fowler-Nordheim tunneling due to the smaller conduction band offset with a Si substrate, thus enhancing program/erase speed. Moreover, using high-k materials as blocking layer, such as Al_2O_3 film, can improve the device performance such as lower voltage and scaling ability. The C-V curves of the device with $TiAl_2O_5$ nanocrystals as the charge trapping layer at 1 MHz are presented. By examining the C-V responses according to the bias polarity applied, the programmed and erased states can be determined. $TiAl_2O_5$ nanocrystals are precipitated from the phase separation of $Ti_{0.2}Al_{0.8}O_x$ film annealed at 900°C. A memory window of 2.3 V and a stored electron density of $1 \times 10^{-13}\,\mathrm{Acm}^{-2}$ are obtained. The C-V curves show no memory window. Therefore, it can be reasonably concluded that the charge trapping effect of the device is related to the formation of $TiAl_2O_5$ nano-crystals. Good retention characteristics of the memory device at 80°C are observed due to the deep charge trapping level as identified by the valence band offsets and electron energy loss spectrum measurements.

Treatment of GaAs surface by using dimethylaluminumhydride-derived AlON passivation layer prior to HfO_2 deposition is introduced to solve the issue of Fermi level pinning [58]. AlON passivation layer effectively suppresses the oxides formation and leads to the Fermi level unpinning at the interface between GaAs and HfO_2. Excellent C-V characteristics with saturated accumulation capacitance and reduced leakage current which is shown in Figure 33 have been achieved based on analysis from MOS of Au/HfO_2/AlON/GaAs stack, which may originate from the decrease in the interface state density and the increase in the conduction band offset. One can easily observe that C-V curve stretches out along the voltage axis, which indicates high density of interface states for directly deposited HfO_2 on GaAs. Meanwhile, the increased accumulation capacitance and the reduced hysteresis in HfO_2/GaAs system with passivation may come from the reduced interfacial state density and the improved trapping behavior of the dielectric. The trend of flat band voltage shift implies that these electrical characteristics could be improved by modulating the quality of the AlON interfacial layer.

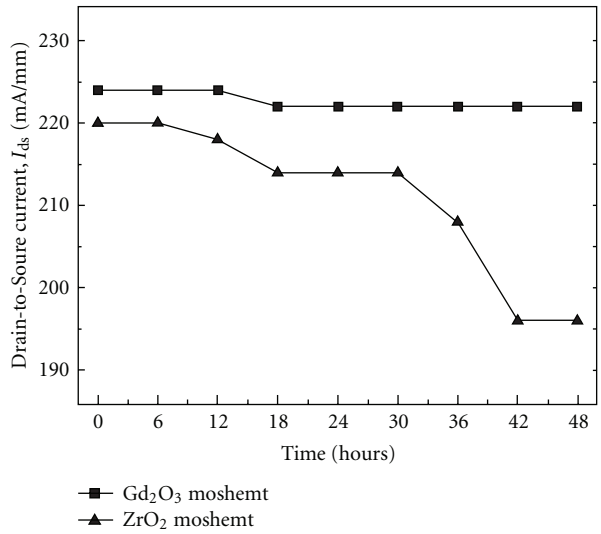

Figure 34: The reliability characteristics for both devices [59].

4.4. Rare-Earth Gate Oxide Dielectrics

4.4.1. Gadolinium Oxide. Further scaling of the SiO_2 gate layer thickness may cause problems because it may result in a large increase of the leakage current and influencing device reliability. High-k oxide layer such as Pr_2O_3, Gd_2O_3, and ZrO_2 are widely considered to replace SiO_2 as the gate dielectric film in order to suppress the gate leakage current [59]. Moreover, the thermally stable high-k GaAs MOSFETs architecture is superior to the traditional metal-semiconductor Schottky interface of GaAs MOSFETs because MOSFET can drive higher output power under a larger gate voltage swings with fewer device self-heating-induced performance degradation. To realize these potential advantages, practical GaAs-based MOSFETs require a gate insulator with a large band gap for low gate leakage current and a high-quality oxide/semiconductor interface together for efficient channel modulation ability. Based on the measurement results, Gd_2O_3 MOSFETs exhibit a better electrical characteristic with an excellent reliability. The dielectric constant of Gd_2O_3 and ZrO_2 oxide layers is estimated to be 10.6 and 7.3 by the MOS-ring capacitor method for C-V measurements. In addition, the thermal stability of the devices has been investigated and compared with the high- k materials Gd_2O_3 and ZrO_2 thin films for reliability test. The Gd_2O_3 MOSFETs achieved better thermal stable characteristic due to its similar lattice structure with GaAs native oxide layer. At high-temperature operation, the voltage degradation slope is 1.2 $\times 10^{-3}$ V/°C and the maximum current degradation slope is 1.4×10^{-2} mA/°C. Due to high-k gate insulator layer of GaAs MOSFETs have wide energy band gap; they can significantly reduce the gate leakage current at a high drain voltage operation, which will certainly be beneficial for the linearity and breakdown improvement of devices. Two devices 48-hour current stress curves are shown in Figure 34, and the Gd_2O_3 MOSFETs exhibit a better reliability characteristic within 48 hours than the ZrO_2 MOSFETs due to its higher binding energy and better interface with GaAs. Based on measurements results, the Gd_2O_3 MOSFETs exhibit the best electrical characteristics, including the lowest gate leakage current, the lowest-noise spectra density, and the high power performance. Therefore, the Gd_2O_3 MOSFETs are suitable candidate for high-power amplifier and monolithic microwave-integrated circuit applications.

Rare earth metal oxides La_2O_3 and Gd_2O_3, as promising alternative high-k gate dielectrics, cannot only control interface layer thickness but also provide a route to monolithic integration of new materials to produce high-speed microprocessor systems and to meet scaling limit [70]. Strong hysteresis and stretch-out are observed in C-V curves, the accumulation region is not flat, the EOT and the dielectric constant are estimated to be 7 nm and 6 respectively, and the fixed charge density is 8×10^{-11} Acm^{-2}. Electrical measurement indicates that the leakage current of Gd_2O_3 is high, and defect density originating from O vacancies is high. In order to improve the electrical performance of Gd-oxide layer, the O_2 partial pressure, pulse frequency, and output energy in PLD should be further optimized.

Electrical characterization of $GdScO_3$ capacitor stacks revealed a dielectric constant of 23, C-V curves with small hysteresis, and low leakage current densities [29]. The leakage current of the thicker films is close to the detection limit. A typical C-V curve of the film is obtained with a CET of 2.4 nm. It is free of humps and irregularities and exhibits a small hysteresis indicating a low number of interface states. From the slope of the linear fit a k value of 23 is derived which is comparable to HfO_2.

4.4.2. Lanthanum Oxide. A wide range of high-k materials, such as HfO_2, ZrO_2, $A1_2O_3$, Sc_2O_3, Y_2O_3, and lanthanide oxide, has been suggested as the candidates to replace SiO_2 or SiO_xN_y. However, most of them have low crystallization temperature and the relatively high oxygen diffusivity may result in a high gate leakage current and the growth of a lower permittivity interfacial layer. Rare earth oxides M_2O_3 (M = Sc, Y, La, Gd, Pr, Lu, etc.) are considered as a candidate material beyond the Hf-based materials due to their higher k values and thermodynamic stability on Si. Among rare earth oxides, La_2O_3 is attractive due to its highest dielectric constant, but it is chemically unstable, as lanthanum hydroxide and carbonate are formed with exposure to ambient atmosphere, resulting in the unwanted flat band voltage shifts. The electrical properties of amorphous $(La_2O_3)_{0.5}(SiO_2)_{0.5}$ films deposited by using pulsed deposition on Si and NH_3-nitrided Si substrates are comparatively investigated [31]. Rare earth oxides M_2O_3 (M = Sc, Y, La, Gd, Pr, Lu, etc.) are considered as a potential candidates material beyond the Hf-based materials due to their higher k values and thermodynamic stability on Si. Among rare earth oxides, La_2O_3 is attractive due to its highest dielectric constant, but it is chemically unstable, as lanthanum hydroxide and carbonate are formed with exposure to ambient atmosphere, indicating the unwanted flat band voltage shift. CET and EOT are two key metrics related to the high-k gate dielectric of the transistors. Interface layer can be effectively suppressed by effective nitrogen incorporation

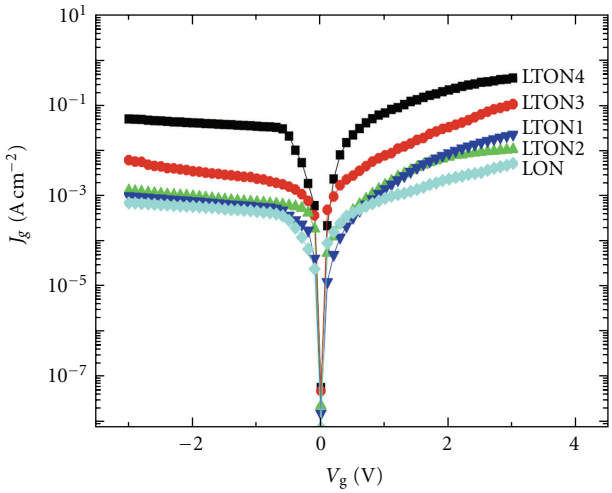

Figure 35: Gate-leakage current density (J_g) versus gate voltage (V_g) for the n-Ge MOS capacitors without or with Ti incorporation [60].

from NH_3-surface nitridation. A larger oxide charge of the as-deposited sample without surface nitridation results in a larger shift of the flat band voltage than the postannealed one. The hysteresis loop is 20 mV for the as-deposited sample with surface nitridation. Therefore, the hysteresis loop results from the chemical states of the Si-rich interface layer. The Pt/LSO/nitrided Si capacitors annealed at high temperature exhibit smaller CET and EOT, a less flat band voltage shift, a negligible hysteresis loop, a smaller equivalent dielectric charge density, and a much lower gate leakage current density as compared with those of the Pt/LSO/Si capacitors without Si surface nitridation.

La_2O_3 thin film shows many advantages, including low interface states density, very small frequency dispersion, and hysteresis due to formation of stable lanthanum germanate [60]. However, a relatively low permittivity due to Ge diffusion into the high-k dielectric prevents further decrease in equivalent oxide thickness. Ti incorporation will increase the permittivity of Hf-based oxides because of the extremely high relative permittivity of Ti-based oxides about 80. Dielectric properties could be achieved by simultaneously incorporating Ti and N into La_2O_3 thin film. Ti-incorporated samples have larger accumulation than the LON samples with larger oxide capacitance for higher Ti-target power, implying that larger k value and thus smaller capacitance equivalent thickness can be obtained for higher Ti content. The negative oxide charge indicates that these traps could be acceptor-like interface and near-interface traps due to the Ge diffusion from the substrate into the high-k layer and the reaction between Ge and Ti near the interface. So a trade-off consideration between k and interface state density is necessary when Ti is added into LaON. The gate-leakage properties of the samples are illustrated in Figure 35. The Ti-incorporated samples exhibit larger gate-leakage current than the LON sample. The higher the Ti content, the larger the gate leakage current. Results indicate that Ti addition can significantly increase the k value and decrease CET due to the extremely high permittivity of Ti-based oxides but deteriorate the dielectric/Ge interface quality, and thus gate leakage properties and device reliability due to the Ti-induced defects. Therefore, the Ti content incorporated into LaON has to be carefully chosen to achieve a good trade-off between the k value and interface state density.

Ge MOS capacitors with La_2O_3 as gate dielectric are fabricated by e-beam evaporation of La_2O_3 followed by PDA in different gases (NH_3, N_2, NO, N_2O, and O_2) [71]. The NH_3, NO, N_2O, and O_2 anneals give higher interface state and oxide charge densities, and thus larger gate leakage current, with the highest for the O_2 anneal for the growth of an unstable GeO_x interlayer. For the O_2 anneal, a thicker GeO_x interlayer is grown, causing the lowest k value and thus the largest CET, as well as deteriorating the interface properties and gate leakage properties. The NO and N_2O anneals give the best device reliability due to the formation of strong N-related bonds. Although the NH_3 anneal can higher the k value due to incorporation of N and suppression of GeO_x interlayer, it induces a large amount of H_2-related electron traps and weak hydrogen bonds, which respectively increases the gate leakage current and decreases the device reliability.

4.4.3. Others. Er_2O_3 is an attractive candidate since it has a relatively high dielectric constant, has large conduction band offset with Si (about 3.5 eV), and is chemically stable in contact with Si. In recent years, single or polycrystalline Er_2O_3 gate dielectric films have been successfully grown on Si substrates by different techniques [30]. The high-frequency (100 kHz) C-V curves of the Er_2O_3 films for different annealing temperature show that the flat band voltage shifts towards positive voltages, which suggests that the fixed charge density is reduced as the annealing temperature increases. The capacitance increases significantly for the sampler annealed at 450°C. The regrowth of the interfacial SiO_2 layer during annealing results in the monotonic decrease of the capacitance, which is due to the diffusion of oxygen atoms tunneling through the Er_2O_3 film towards the Si substrate. For the annealed samples, the leakage current densities are smaller by at least an order of magnitude than those of the as-deposited samples which is due to the improvement by annealing in O_2 ambiance to form stoichiometric films and consequent lowering of the leakage current density. As expected, the leakage current density of the samples annealed at 700°C is smaller than that of 450°C when the gate is negatively biased over 1 V.

High-k-gated MOS devices with SiGe channel and nitridation treatment using plasma immersion ion implantation (PIII) are studied [72]. Nitrogen incorporation into high-k can suppress the interdiffusion of element after high-temperature process. Plasma immersion ion implantation is becoming a favorable technique for dopant incorporation. The leakage current values for samples with PIII nitridation show slightly larger than those without PIII, which may be due to some defects generated by the ion implantation. For samples with Ge content of 10% or 20%, the EOT values and leakage current are similar. For the sample with 30% Ge content in SiGe channel and PIII nitridation, the EOT value is reduced to 9.6 A and the leakage current density

is still acceptable. By incorporating PIII nitridation, these characteristics are much improved. The value of hysteresis is all negative and clockwise and the trap states in dielectric tend to trap hole. The hysteresis values for samples with PIII nitridation are smaller than those without one. The main reason may be attributed to the suppression of Ge diffusion form SiGe channel into high-k dielectric. Stress-induced flat band voltage values for the samples with PIII nitridation are smaller than those without PIII. This result suggests that the oxide traps in high-k/Si/SiGe can be reduced by suppressing Ge diffusion with PIII. After metal gate deposited, PIII nitridation treatment is performed at an energy level of 2.5 keV for 10 minutes.

5. Dielectric Relaxation of High-k Films

High-k gate dielectric is necessary to be used to replace SiO_2. However, there are still some problems need to be considered. The MOSFET performance will be impaired due to (a) the associated losses and (b) dielectric relaxation. Keeping increasing the frequency, the high-k dielectric constant will not be constant. There are two kinds of models related to the dielectric relaxation, the physical model such as the Debye and Dissado-Hill expressions, or the mathematical model such as the Cole-Cole, Cole-Davidson, and Havriliak-Negami formulae. In this section, the model is classified based on whether it is a physical model or mathematical model.

5.1. Hafnium Oxide and Zirconium Oxide. High-k dielectrics as promising candidates to increase capacitor integration densities depend on manufacturing process and frequency because relaxation and resonance mechanisms are observed [61]. Complementary characterization protocols are implemented to analyze high-k insulator behavior from DC to microwave frequencies. The extraction of Plasma-Enhanced Atomic Layer Deposition HfO_2 and ZrO_2 complex permittivity is performed up to 5 GHz using dedicated test vehicles. The high-k films are deposited on a 60 nm thick TiN electrode by Plasma-enhanced ALD following a damascene architecture. Frequency results on Figures 36 and 37 show an excellent agreement all over the wide range of frequencies and a stable capacitance with a rise towards the very low frequencies and a decline in high frequency for the smallest thickness. HfO_2 and ZrO_2 exhibit good performance for frequencies up to 5 GHz, with a capacitance density of 10 fF/um^{-2} for the 32 nm ZrO_2 film whereas for the same thickness of HfO_2 it is only 5 fF/um^{-2}. ZrO_2 is an excellent candidate for MIM capacitors.

5.2. Doped Hafnium Oxide. Zhao et al. [25] have investigated the dielectric relaxation of $La_2Hf_2O_7$. The cause of frequency dispersion is also considered. A possible solution for increasing the HfO_2 crystallization temperature is doping with La. However, significant dielectric relaxation is associated with the high-k thin film $La_2Hf_2O_7$. The capacitance-voltage measurement is implemented for the fundamental characterization technique to extract the dielectric constant and dielectric constant loss from the strong accumulation

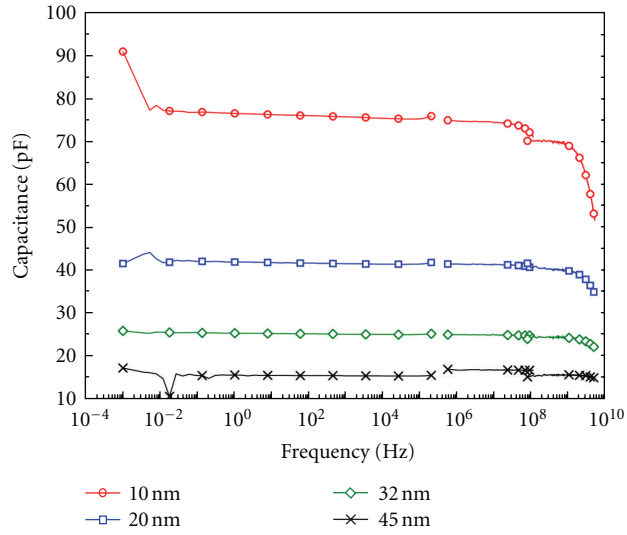

Figure 36: Extraction of the capacitance for the MIM integrating ZrO_2 [61].

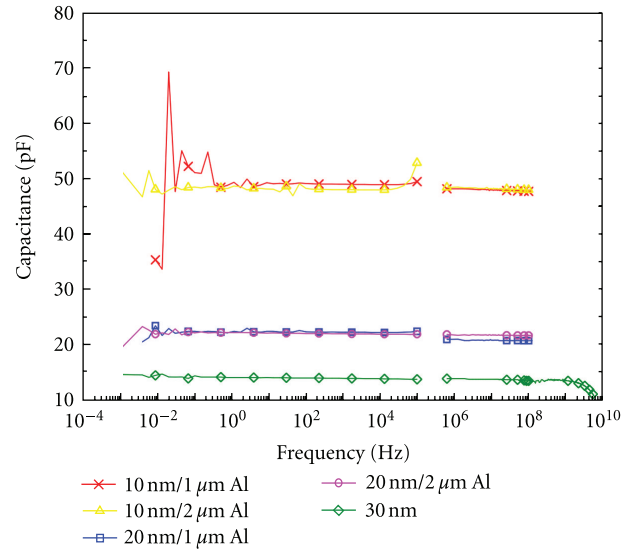

Figure 37: Extraction of the capacitance for the MIM integrating HfO_2 [61].

region in MOS capacitance. The effects of the leakage currents, series resistances, parasitic effects including back contact imperfection and cables and connections, and lossy IL have be taken into account in order to understand the original properties and permittivity of the high-k dielectric from the C-f measurements. The frequency dispersion is attributed to the effects of the lossy IL and the dependence of k value of the $La_2Hf_2O_7$ dielectric on the frequency. The high-k thin films are deposited directly on silicon wafers which have layers of native SiO_2 on their surface and a lossy IL cannot be avoided since the quality of the native SiO_2 is not good. The frequency-dependent change in the real and imaginary permittivity is shown in Figure 38. Obviously, the PDA process improved the dielectric relaxation and reduced

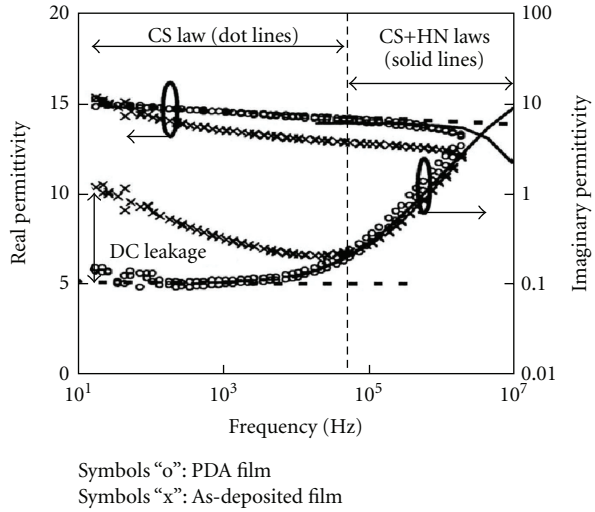

FIGURE 38: Frequency dependence of the real and imaginary permittivities of $La_2Hf_2O_7$ dielectric for the as-deposited and PDA samples [25].

the dielectric loss. The complex susceptibilities relate to the Curie-von Schweidler (CS) law and Havriliak-Negami (HN) laws, respectively. The dielectric relaxation of the PDA films is shown to be dominated mainly by the CS law, (see two dot lines in Figure 38), when the frequency is smaller than 30 MHz. However, when the frequency is over 30 MHz, the HN law plays an important role (see two solid lines in Figure 38). The dielectric loss reduces because an increase of the IL thickness caused the reduction of the dc conductivity. Two possible causes for this are proposed as: (1) ion movement of unbounded La^+ or Hf^+ ions in the metal oxide causing dielectric relaxation, and (2) the combination of unbounded metal ions with electron traps, generating dipole moments and introducing dielectric relaxation.

5.3. Doped Zirconium Oxide. Al-doping of ZrO_2 during ALD and high-temperature annealing are introduced to modify and enhance dielectric performance of MIM structures in terms of permittivity, capacitance nonlinearity, dielectric relaxation, and loss [67]. All these characteristics are a function of the amorphous/crystalline phase of the films. The crystallization temperature increases with increasing level of doping. The increased permittivity due to crystallization of the films in the tetragonal phase is associated with a significantly intensified relaxation and loss process with a cutoff frequency at about 10 kHz. The capacitance-frequency curves measured from 100 Hz to 1 MHz at a fixed voltage ranging from +1.5 down to −1.5 V for some of the samples are presented in Figure 39. A significant steeper decrease in capacitance with frequency is observed in the frequency range from 5 to 60 kHz which could be assigned to some specific crystallization-related relaxation process for the crystalline samples. The frequency dispersion of the capacitance is originated from the traps near the metal/dielectric interface which have different time constants and strongly modulate capacitor charge at a certain frequency. The capacitance dispersion increases with increasing bias especially at lower frequencies for the crystalline samples. Thus, there are additional traps at the bottom electrode interface which cause stronger dielectric relaxation at positive biases irrespectively of the amorphous/crystalline phase of the films. The increased capacitance dispersion with increasing positive biasing could be explained with different spatial location of the traps which become accessible by the electrons at a certain voltage. However, the results give also evidence that stronger Al-doping may suppress to some extent formation of this layer at high temperature. Generally, two different types of phenomena should be accounted for to explain the dielectric behavior of the structures, phenomena which are related to the crystalline state of the films and to interface-related processes which are assigned to different structural modifications and traps at the two $TiN/Zr_{1-x}Al_xO_2$ interfaces.

Lanthanum-doped zirconium oxide films, with La contents, up to 0.35, have been prepared. Films annealed at 900°C are crystallized into phases with higher k values [73]. Increasing the La content prevented the monoclinic phase and stabilized the tetragonal or cubic phase. The highest dielectric constant is achieved for a lightly doped film with a La content of 0.09, for which a constant value of 40 is obtained. C-V measurements are used to characterize the defects and obtain permittivities of the $La_xZr_{1-x}O_{2-\delta}$ thin films. There are six mechanisms which may cause the frequency dispersion: (1) series resistances, (2) parasitic effects (including back contact imperfection and cables and connections, (3) leakage currents, (4) the interlayer between $La_xZr_{1-x}O_{2-\delta}$ layer and semiconductor, (5) surface roughness, and (6) value dependence on frequency of the $La_xZr_{1-x}O_{2-\delta}$ dielectric. The relationship between the k value and test frequency is demonstrated for annealed samples. The film with a La content of $x = 0.09$ has a significant increase in the k value of the dielectric and also has a large dielectric relaxation. The dielectric relaxation is most severe at concentration levels where the highest k values are achieved. The dielectric relaxation results have been modeled with the CS and/or KWW relationships (see solid lines). The fitting parameters are given in the figure. The k value of the as-deposited $Zr_{1-x}O_{2-\beta}$ dielectric layers clearly shows a power-law dependence on frequency following the CS relationship for the $x = 0.09$ La content. For the $x = 0.35$ La content, the dielectric relaxation response is best fitted by the combined KWW and CS relationships. After annealing, the single CS relaxation process tends to the combined KWW and CS mechanism for $x = 0.09$, while the KWW relaxation vanishes altogether for $x = 0.35$. This general type of dielectric relaxation can be described by the CS law or the KWW relationship:

$$\frac{dP_{\mathrm{CS}}}{dt} \propto t^{-n} \quad \text{with } 0 \le n \le 1,$$
$$P_{\mathrm{KWW}} \propto \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \quad \text{with } 0 \le \beta \le 1, \tag{2}$$

where P_{CS} is the CS polarization and the exponent n indicates the degree of dielectric relaxation. P_{KWW} is the KWW

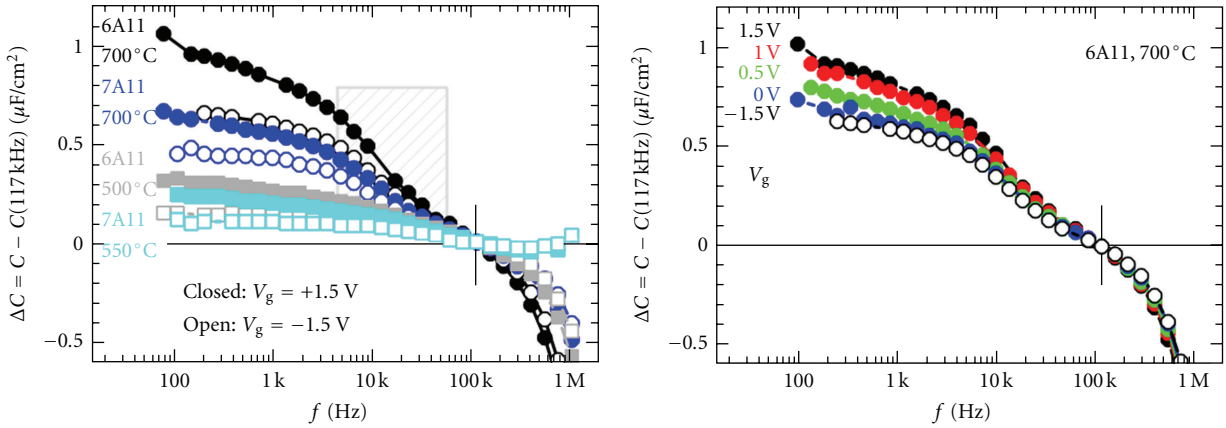

FIGURE 39: Normalized capacitance-frequency curves (a) of amorphous and crystalline at positive and negative gate polarity, and (b) of crystalline sample annealed at 700°C with gate voltage as parameter [67].

polarization, τ is the KWW relaxation time, and β is the parameter of P_{KWW}. The complex susceptibilities, χ_{CS} and χKWW, related to the CS law and KWW laws, are simply the Fourier transform of the aforementioned time domain responses:

$$\begin{aligned}
\chi_{\mathrm{CS}}(\omega) &\propto F\left(\frac{dP_{\mathrm{CS}}}{dt}\right) \propto \int_0^{\infty} t^{-n}\exp(-i\omega t)dt \propto (i\omega)^{n-1},\\
\chi_{\mathrm{KWW}}(\omega) &\propto F\left(\frac{dP_{\mathrm{KWW}}}{dt}\right)\\
&\propto \int_0^{\infty}\frac{\beta}{\tau}\left(\frac{t}{\tau}\right)^{\beta-1}\\
&\times \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\exp(-i\omega t)dt.
\end{aligned} \tag{3}$$

This was introduced by a significant dielectric relaxation, following a single CS power-law dependency with frequency, changing to a mixed CS and KWW relationships after annealing. The dielectric relaxation is most severe for lightly doped films with the highest k values. The dielectric relaxation appears to be related to the size of crystal grains formed during annealing, which is dependent on the doping level.

5.4. Lanthanum-Doped Zirconia and Cerium-Doped Hafnia. Hafnium and zirconia as leading candidates for gate insulators for DRAM exhibit a range of crystalline phases [43]. The monoclinic phase (k ~20 to 25) is thermodynamically stable at room temperature, while the tetragonal and cubic phases are metastable but have higher k-values, in theory up to 70. The tetragonal or cubic phases of HfO_2 and ZrO_2 can be stabilized by additions of rare earth elements, such as La and Ce. The permittivity enhancement due to doping has been raised to investigate the effects of the level of doping on the dielectric relaxation properties of lanthanum-doped zirconia films and cerium-doped hafnium films. The zirconia film with a La concentration of $x = 0.35$ has a relatively flat frequency response, with the dielectric constant value of 17 comparable with that of undoped ZrO_2. In contrast the lightly doped 9% sample has a substantially increased dielectric constant value but suffered from a severe dielectric relaxation. The constant value of 39 is obtained at 100 Hz, but this value was reduced with increasing frequency down to a constant value of 25 at 100 kHz, while the 10% Ce-doped hafnium film also has a dielectric constant value higher than that of undoped HfO_2. The variation in dielectric constant value with frequency is less severe than that with the La doped zirconia films with the value of 33 at 100 Hz and 26 at 100 kHz. The significant enhancement of the dielectric constant for lightly doped films is also associated with significant dielectric relaxation. The dielectric relaxation is most severe in the doping of $LaZrO_2$ film, with light doping of $CeZrO_2$ having a flatter frequency response.

6. Conclusions

A large variety of high-k oxides have been proposed for replacing SiO_2 as a MOS gate dielectric. From these oxides, HfO_2 and HfO_2-based materials have been found to be the most promising candidates. This is due to their compatibility with Si technology, high dielectric permittivity. Since HfO_2 films show poor thermal stability resulting in an increase in leakage current after subsequent thermal processing, incorporation of Al into HfO_2 films helps to improve the thermal stability. Furthermore, one of the possibilities to improve an Hf-based dielectric permittivity consists in adding another metal. Recently, Ti is added into the Hf-based dielectrics to achieve a higher k value, with remarkable thermal stability, and improved electrical properties. The dielectric constant of ZrO_2 is high enough (between 22 and 25) and significantly higher than SiO_2. Unlike TiO_2, ZrO_2will not cause fringing fields from the drain through the gate dielectric. This is due to the over large dielectric constant of TiO_2 which results in poor subthreshold performance due to the associated source-to-channel potential barrier degradation. High-k oxide layer such as Pr_2O_3, Gd_2O_3, and ZrO_2 is widely considered candidates to replace SiO_2 as the

gate dielectric film in order to suppress the gate leakage current. La_2O_3 is attractive due to its high dielectric constant, but it is chemically unstable, as lanthanum hydroxide and carbonate are formed with exposure to ambient atmosphere, resulting in the unwanted flat band voltage shift.

Although many investigations have been devoted to different aspects of the preparation and properties of high-k dielectrics and their integration with conventional Si devices, there are still many obstacles that need to be conquered. In terms of the deposition aspects, the precursors and growth conditions for the high-k films should be honed and/or optimized further [19]. The thermal stability issue should be addressed with the aim to increase the crystallization temperature of the high-k oxides to prevent the crystallization of amorphous dielectric films during subsequent high-temperature processing [73]. A search for new high-k dielectric materials is now in progress. Some multicomponent oxides, such as $LaLuO_3$ and rare-earth scandates $LaScO_3$, $GdScO_3$, $DyScO_3$, and $SmScO_3$, exhibit high dielectric constants (similar to or exceeding that of HfO_2), wide bandgaps, large band offsets to both the valence and conduction bands of Si, low leakage current, and superior thermal stability of amorphous phase [74–76]. These oxides are now under intensive investigations for potential high-k applications, and, in the future, could compete with Hf-based oxides as gate dielectrics for Si-based MOSFETs. Also, Gallium arsenide (GaAs) substrates for MOS transistors are being considered for their high electron channel mobility [53, 77]. Meanwhile, Germanium has been introduced as channel material due to its high mobility for both electron and holes as compared to silicon [27, 37, 65, 78]. It is found that for suitable future scaling, a dielectric with K over 40 is preferred. Furthermore, high-carrier-mobility Ge- and SiGe-based MOSFETs with high-k gate dielectrics have been extensively studied to further scale down the size of the devices while increasing their operating speed [38, 79, 80].

Acknowledgments

This paper was funded in part from the National Natural and Science Foundation of China under the Grant no. 60976075 and from the Suzhou Science and Technology Bureau of China under the Grant SYG201007.

References

[1] The International Technology Roadmap for Semiconductors (ITRS) Roadmap, ITRS Roadmap 2007/2008, http://public.itrs.net/.

[2] L. Yan, C. M. Lopez, R. P. Shrestha, E. A. Irene, A. A. Suvorova, and M. Saunders, "Magnesium oxide as a candidate high-κ gate dielectric," *Applied Physics Letters*, vol. 88, no. 14, Article ID 142901, 2006.

[3] S. Chen, Y. Y. Zhu, R. Xu et al., "Superior electrical properties of crystalline Er2O3 films epitaxially grown on Si substrates," *Applied Physics Letters*, vol. 88, no. 22, Article ID 222902, 2006.

[4] A. Fissel, Z. Elassar, O. Kirfel, E. Bugiel, M. Czernohorsky, and H. J. Osten, "Interface formation during molecular beam epitaxial growth of neodymium oxide on silicon," *Journal of Applied Physics*, vol. 99, no. 7, Article ID 074105, 2006.

[5] A. A. Dakhel, "Characterisation of Nd2O3 thick gate dielectric for silicon," *Physica Status Solidi*, vol. 201, no. 4, pp. 745–755, 2004.

[6] T. Busani and R. A. B. Devine, "The importance of network structure in high-k dielectrics: LaAlO3, Pr2O3, and Ta2O5," *Journal of Applied Physics*, vol. 98, no. 4, Article ID 044102, 2005.

[7] D. P. Brunco, A. Dimoulas, N. Boukos et al., "Materials and electrical characterization of molecular beam deposited CeO2 and CeO2/HfO2 bilayers on germanium," *Journal of Applied Physics*, vol. 102, no. 2, Article ID 024104, 2007.

[8] Y. Nishikawa, N. Fukushima, N. Yasuda, K. Nakayama, and S. Ikegawa, "Electrical properties of single crystalline CeO2 high-k gate dielectrics directly grown on Si (111)," *Japanese Journal of Applied Physics*, vol. 41, no. 4, pp. 2480–2483, 2002.

[9] J. S. Suehle, E. M. Vogel, M. D. Edelstein et al., "Challenges of high-k gate dielectrics for future MOS devices," in *Proceedings of the 6th International Symposium on Plasma Process-Induced Damage*, pp. 90–93, IEEE Computer Society Press, Monterey, Calif, USA, 2001.

[10] F. C. Chiu, S. Y. Chen, C. H. Chen, H. W. Chen, H. S. Huang, and H. L. Hwang, "Interfacial and electrical characterization in metal-oxide-semiconductor field-effect transistors with CeO2 gate dielectric," *Japanese Journal of Applied Physics*, vol. 48, no. 4, Article ID 04C014, 2009.

[11] P. C. Juan, C. H. Liu, C. L. Lin et al., "Electrical characterization and dielectric properties of metal-oxide-semiconductor structures using high-K CeZrO4 ternary oxide as gate dielectric," *Japanese Journal of Applied Physics*, vol. 48, no. 2, pp. 05DA021–05DA025, 2009.

[12] A. P. Milanov, *MOCVD and ALD of rare earth containing multifunctional materials: from precursor chemistry to thin film deposition and applications*, Ph.D. thesis, Ruhr University Bochum, Germany, 2010.

[13] G. Dong and Y. Qiu, "Pentacene thin-film transistors with Ta2O5 as the gate dielectric," *Journal of the Korean Physical Society*, vol. 54, no. 1, pp. 493–497, 2009.

[14] Q. Bao, C. Chen, D. Wang, Q. Ji, and T. Lei, "Pulsed laser deposition and its current research status in preparing hydroxyapatite thin films," *Applied Surface Science*, vol. 252, no. 5, pp. 1538–1544, 2005.

[15] B. H. Lee, L. Kang, R. Nieh, W. J. Qi, and J. C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing," *Applied Physics Letters*, vol. 76, no. 14, pp. 1926–1928, 2000.

[16] X. Zhu, J. Zhu, A. Li, Z. Liu, and N. Ming, "Challenges in atomic-scale characterization of high-k dielectrics and metal gate electrodes for advanced CMOS gate stacks," *Journal of Materials Science and Technology*, vol. 25, no. 3, pp. 289–313, 2009.

[17] R. Huang, H. Wu, J. Kang et al., "Challenges of 22 nm and beyond CMOS technology," *Science in China Series F*, vol. 52, no. 9, pp. 1491–1533, 2009.

[18] H. Hasegawa, M. Akazawa, A. Domanowska, and B. Adamowicz, "Surface passivation of III-V semiconductors for future CMOS devices-Past research, present status and key issues for future," *Applied Surface Science*, vol. 256, no. 19, pp. 5698–5707, 2010.

[19] N. Izyumskaya, Y. Alivov, and H. Morkoç, "Oxides, oxides, and more oxides: high-oxides, ferroelectrics, ferromagnetics, and multiferroics," *Critical Reviews in Solid State and Materials Sciences*, vol. 34, no. 3-4, pp. 89–179, 2009.

[20] Y. H. Wong and K. Y. Cheong, "ZrO2 thin films on Si substrate," *Journal of Materials Science*, vol. 21, no. 10, pp. 980–993, 2010.

[21] Y. P. Gong, A. D. Li, X. Qian, C. Zhao, and D. Wu, "Interfacial structure and electrical properties of ultrathin HfO2 dielectric films on Si substrates by surface sol-gel method," *Journal of Physics D*, vol. 42, no. 1, Article ID 015405, 2009.

[22] D. C. Suh, Y. D. Cho, S. W. Kim et al., "Improved thermal stability of Al2O3/HfO2/Al2O3 high-k gate dielectric stack on GaAs," *Applied Physics Letters*, vol. 96, no. 14, Article ID 142112, 2010.

[23] D. Rébiscoul, S. Favier, J. P. Barnes, J. W. Maes, and F. Martin, "Characterization of the annealing impact on La2O3/HfO2 and HfO2/La2O3 stacks for MOS applications," *Microelectronic Engineering*, vol. 87, no. 3, pp. 278–281, 2010.

[24] L. Y. Huang, A. D. Li, W. Q. Zhang, H. Li, Y. D. Xia, and D. Wu, "Fabrication and characterization of La-doped HfO2 gate dielectrics by metal-organic chemical vapor deposition," *Applied Surface Science*, vol. 256, no. 8, pp. 2496–2499, 2010.

[25] C. Z. Zhao, S. Taylor, M. Werner, P. R. Chalker, J. M. Gaskell, and A. C. Jones, "Frequency dispersion and dielectric relaxation of La2 Hf2O7," *Journal of Vacuum Science and Technology B*, vol. 27, no. 1, pp. 333–337, 2009.

[26] S. Lü, J. Yin, Y. Xia, L. Gao, and Z. Liu, "Study on the thermal stability and electrical properties of the high-k dielectrics (ZrO2)x (SiO2)1-x," *Science in China Series E*, vol. 52, no. 8, pp. 2222–2226, 2009.

[27] S. Abermann, C. Henkel, O. Bethge, G. Pozzovivo, P. Klang, and E. Bertagnolli, "Stabilization of a very high-k crystalline ZrO2 phase by post deposition annealing of atomic layer deposited ZrO2/La2O3 dielectrics on germanium," *Applied Surface Science*, vol. 256, no. 16, pp. 5031–5034, 2010.

[28] X. Cheng, D. He, Z. Song, Y. Yu, and D. Shen, "Interfacial and electrical characterization of HfO2 gate dielectric film with a blocking layer of Al2O3," *Rare Metal Materials and Engineering*, vol. 38, no. 2, pp. 189–192, 2009.

[29] M. Wagner, T. Heeg, J. Schubert et al., "Gadolinium scandate thin films as an alternative gate dielectric prepared by electron beam evaporation," *Applied Physics Letters*, vol. 88, no. 17, Article ID 172901, 2006.

[30] F. Ze-Bo, Z. Yan-Yan, W. Jia-Le, and J. Zui-Min, "Annealing effects on the structure and electrical characteristics of amorphous Er2O3 films," *Chinese Physics B*, vol. 18, no. 8, pp. 3542–3546, 2009.

[31] L. G. Gao, K. B. Yin, L. Chen et al., "The effect of Si surface nitridation on the interfacial structure and electrical properties of (La2O3)0.5(SiO2)0.5 high-k gate dielectric films," *Applied Surface Science*, vol. 256, no. 1, pp. 90–95, 2009.

[32] P. Taechakumput, S. Taylor, O. Buiu, R. J. Potter, P. R. Chalker, and A. C. Jones, "Optical and electrical characterization of hafnium oxide deposited by liquid injection atomic layer deposition," *Microelectronics Reliability*, vol. 47, no. 4-5, pp. 825–829, 2007.

[33] L. Shi, Y. Zhou, J. Yin, and Z. Liu, "Characterization upon potential properties of HfO2 stabilized by Y2O3 films as cubic phase," *Journal of Applied Physics*, vol. 107, no. 1, Article ID 014104, 2010.

[34] C. Wiemer, L. Lamagna, S. Baldovino et al., "Dielectric properties of Er-doped HfO2 (Er~15%) grown by atomic layer deposition for high-κ gate stacks," *Applied Physics Letters*, vol. 96, no. 18, Article ID 182901, 2010.

[35] G. He, Z. Q. Sun, M. Liu, and L. D. Zhang, "Nitrogen dependence of band alignment and electrical properties of HfTiON gate dielectrics metal-oxide-semiconductor capacitor," *Applied Physics Letters*, vol. 97, no. 19, Article ID 192902, 2010.

[36] J. Oh, P. Majhi, R. Jammy et al., "Fully strained Si0.75Ge0.25 epitaxial films with HfSiO gate dielectrics for high mobility channel metal-oxide semiconductor devices," *Microelectronic Engineering*, vol. 85, no. 8, pp. 1804–1806, 2008.

[37] Q. Xie, D. Deduytsche, M. Schaekers et al., "Implementing TiO2 as gate dielectric for Ge-channel complementary metal-oxide-semiconductor devices by using HfO2/GeO2 interlayer," *Applied Physics Letters*, vol. 97, no. 11, Article ID 112905, 2010.

[38] H. X. Xu, J. P. Xu, C. X. Li, and P. T. Lai, "Improved electrical properties of Ge metal-oxide-semiconductor capacitors with high-k HfO2 gate dielectric by using La2O3 interlayer sputtered with/without N2 ambient," *Applied Physics Letters*, vol. 97, no. 2, Article ID 022903, 2010.

[39] C. X. Li, C. H. Leung, P. T. Lai, and J. P. Xu, "Effects of fluorine incorporation on the properties of Ge p-MOS capacitors with HfTiON dielectric," *Solid-State Electronics*, vol. 54, no. 7, pp. 675–679, 2010.

[40] K. Black, H. C. Aspinall, A. C. Jones et al., "Deposition of ZrO2 and HfO2 thin films by liquid injection MOCVD and ALD using ansa-metallocene zirconium and hafnium precursors," *Journal of Materials Chemistry*, vol. 18, no. 38, pp. 4561–4571, 2008.

[41] P. R. Chalker, M. Werner, S. Romani et al., "Permittivity enhancement of hafnium dioxide high-κ films by cerium doping," *Applied Physics Letters*, vol. 93, no. 18, Article ID 182911, 2008.

[42] J. M. Gaskell, A. C. Jones, H. C. Aspinall et al., "Deposition of lanthanum zirconium oxide high-κ films by liquid injection atomic layer deposition," *Applied Physics Letters*, vol. 91, no. 11, Article ID 112912, 2007.

[43] M. Werner, C. Z. Zhao, S. Taylor, P. R. Chalker, K. Black, and J. Gaskell, "Permittivity enhancement and dielectric relaxation of doped hafnium and zirconium oxide," in *Proceedings of the 16th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA '09)*, pp. 625–627, July 2009.

[44] H. Y. Gou, S. J. Ding, Y. Huang et al., "Nonvolatile metal-oxide-semiconductor capacitors with ru-ruox composite nanodots embedded in atomic-layer-deposited Al2O3 films," *Journal of Electronic Materials*, vol. 39, no. 8, pp. 1343–1350, 2010.

[45] X. Cheng, D. Xu, Z. Song et al., "The properties of high-k gate dielectric films deposited on HRSOI," *Microelectronic Engineering*, vol. 86, no. 12, pp. 2404–2407, 2009.

[46] J. M. Gaskell, S. Przybylak, A. C. Jones et al., "Deposition of Pr-and Nd-aluminate by liquid injection MOCVD and ALD using single-source heterometallic alkoxide precursors," *Chemistry of Materials*, vol. 19, no. 19, pp. 4796–4803, 2007.

[47] Y. C. Wu, E. Y. Chang, Y. C. Lin et al., "Study of the inversion behaviors of Al2O3/InxGa1-xAs metal-oxide-semiconductor capacitors with different In contents," *Solid-State Electronics*, vol. 54, no. 1, pp. 37–41, 2010.

[48] X. Zhang, H. Tu, X. Wang et al., "Hetero-epitaxial growth of the cubic single crystalline HfO2 film as high k materials by pulsed laser ablation," *Journal of Crystal Growth*, vol. 312, no. 20, pp. 2928–2930, 2010.

[49] W. Luo, T. Yuan, Y. Kuo, J. Lu, J. Yan, and W. Kuo, "Breakdown phenomena of zirconium-doped hafnium oxide high-k stack with an inserted interface layer," *Applied Physics Letters*, vol. 89, no. 7, Article ID 072901, 2006.

[50] M. Ji, L. Wang, Y. Xiong, and J. Du, "Electrical characteristics of MOS capacitor using amorphous Gd2O3-doped HfO2 insulator," *Journal of Rare Earths*, vol. 28, no. 3, pp. 396–398, 2010.

[51] S. Toyoda, H. Kamada, T. Tanimura et al., "Annealing effects of in-depth profile and band discontinuity in TiN/LaO/HfSiO/SiO2/Si gate stack structure studied by angle-resolved photoemission spectroscopy from backside," *Applied Physics Letters*, vol. 96, no. 4, Article ID 042905, 2010.

[52] R. Gassilloud, F. Martin, C. Leroux et al., "MOCVD fluorine free WSix metal gate electrode on high-k dielectric for NMOS technology," *Microelectronic Engineering*, vol. 86, no. 3, pp. 263–267, 2009.

[53] V. Budhraja, X. Wang, and D. Misra, "MOS capacitors with metal gate/high-k dielectrics on GaAs bulk substrate," *Journal of Materials Science*, vol. 21, no. 12, pp. 1322–1326, 2010.

[54] M. K. Bera, S. Chakraborty, S. Saha et al., "High frequency characterization and continuum modeling of ultrathin high-k (ZrO2) gate dielectrics on strained-Si," *Thin Solid Films*, vol. 504, no. 1-2, pp. 183–187, 2006.

[55] D. Tsoutsou, G. Apostolopoulos, S. F. Galata et al., "Stabilization of very high-k tetragonal phase in Ge-doped ZrO2 films grown by atomic oxygen beam deposition," *Journal of Applied Physics*, vol. 106, no. 2, Article ID 024107, 2009.

[56] D. Tsoutsou, G. Apostolopoulos, S. Galata et al., "Stabilization of a very high-k tetragonal ZrO2 phase by direct doping with germanium," *Microelectronic Engineering*, vol. 86, no. 7-9, pp. 1626–1628, 2009.

[57] M. T. Yu, S. W. Jeong, H. J. Lee, and Y. Roh, "Characteristics of high-k gate oxide prepared by oxidation of multi-layered Hf/Zr/Hf/Zr/Hf metal films," *Thin Solid Films*, vol. 516, no. 7, pp. 1563–1568, 2008.

[58] G. He, L. D. Zhang, M. Liu, and Z. Q. Sun, "HfO2-GaAs metal-oxide-semiconductor capacitor using dimethylaluminumhydride-derived aluminum oxynitride interfacial passivation layer," *Applied Physics Letters*, vol. 97, no. 6, Article ID 062908, 2010.

[59] H. C. Chiu, C. H. Chen, C. W. Yang, J. S. Fu, and C. S. Wang, "Electrical and reliability characteristics of GaAs MOSHEMTs utilizing high-k IIIB and IVB oxide layers," *Microelectronics Reliability*, vol. 50, no. 5, pp. 631–634, 2010.

[60] H. X. Xu, J. P. Xu, C. X. Li, C. L. Chan, and P. T. Lai, "Impacts of Ti on electrical properties of Ge metal-oxide-semiconductor capacitors with ultrathin high-k LaTiON gate dielectric," *Applied Physics A*, vol. 99, pp. 903–906, 2010.

[61] T. Bertaud, C. Bermond, T. Lacrevaz et al., "Wideband frequency and in situ characterization of ultra thin ZrO2 and HfO2 films for integrated MIM capacitors," *Microelectronic Engineering*, vol. 87, no. 3, pp. 301–305, 2010.

[62] J. P. Xu, X. F. Zhang, C. X. Li, C. L. Chan, and P. T. Lai, "Comparative study of HfTa-based gate-dielectric Ge metal-oxide-semiconductor capacitors with and without AlON interlayer," *Applied Physics A*, vol. 99, no. 1, pp. 177–180, 2010.

[63] J. M. Gaskell, A. C. Jones, P. R. Chalker et al., "Deposition of lanthanum zirconium oxide high-k films by liquid injection ALD and MOCVD," *Chemical Vapor Deposition*, vol. 13, no. 12, pp. 684–690, 2007.

[64] D. Han, Y. Wang, S. Zhang et al., "Fabrication and characteristics of ZnO MOS capacitors with high-K HfO2 gate dielectrics," *Science China Technological Sciences*, vol. 53, no. 9, pp. 2333–2336, 2010.

[65] L. Lamagna, C. Wiemer, S. Baldovino et al., "Thermally induced permittivity enhancement in La-doped ZrO2 grown by atomic layer deposition on Ge(100)," *Applied Physics Letters*, vol. 95, no. 12, Article ID 122902, 2009.

[66] S. Abermann, O. Bethge, C. Henkel, and E. Bertagnolli, "Atomic layer deposition of ZrO2/La2O3 high-k dielectrics on germanium reaching 0.5 nm equivalent oxide thickness," *Applied Physics Letters*, vol. 94, no. 26, Article ID 262904, 2009.

[67] A. Paskaleva, M. Lemberger, A. J. Bauer et al., "Influence of the amorphous/crystalline phase of Zr1-xAl xO2 high-k layers on the capacitance performance of metal insulator metal stacks," *Journal of Applied Physics*, vol. 106, no. 5, Article ID 054107, 2009.

[68] M. Akazawa and H. Hasegawa, "High-k Al2O3 MOS structures with Si interface control layer formed on air-exposed GaAs and InGaAs wafers," *Applied Surface Science*, vol. 256, no. 19, pp. 5708–5713, 2010.

[69] Y. Zhou, J. Yin, H. N. Xu et al., "A TiAl2O5 nanocrystal charge trap memory device," *Applied Physics Letters*, vol. 97, no. 14, Article ID 143504, 2010.

[70] X. Cheng, D. Xu, Z. Song et al., "Characterization of gadolinium oxide film by pulse laser deposition," *Applied Surface Science*, vol. 256, no. 3, pp. 921–923, 2009.

[71] H. X. Xu, J. P. Xu, C. X. Li, and P. T. Lai, "Electrical properties of Ge metal-oxide-semiconductor capacitors with La2O3 gate dielectric annealed in different ambient," *Thin Solid Films*, vol. 518, no. 23, pp. 6962–6965, 2010.

[72] C. H. Fu, K. S. Chang-Liao, L. W. Du, T. K. Wang, W. F. Tsai, and C. F. Ai, "Electrical characteristics of SiGe channel MOS devices with high-k/metal gate incorporated with nitrogen by plasma immersion ion implantation," *Solid-State Electronics*, vol. 54, no. 10, pp. 1094–1097, 2010.

[73] C. Z. Zhao, S. Taylor, M. Werner et al., "Dielectric relaxation of lanthanum doped zirconium oxide," *Journal of Applied Physics*, vol. 105, no. 4, Article ID 044102, 2009.

[74] P. Sivasubramani, T. H. Lee, M. J. Kim et al., "Thermal stability of lanthanum scandate dielectrics on Si(100)," *Applied Physics Letters*, vol. 89, no. 24, Article ID 242907, 2006.

[75] J. M. J. Lopes, U. Littmark, M. Roeckerath et al., "Effects of annealing on the electrical and interfacial properties of amorphous lanthanum scandate high-κ films prepared by molecular beam deposition," *Journal of Applied Physics*, vol. 101, no. 10, Article ID 104109, 2007.

[76] J. M. J. Lopes, M. Roeckerath, T. Heeg et al., "Amorphous lanthanum lutetium oxide thin films as an alternative high-κ gate dielectric," *Applied Physics Letters*, vol. 89, no. 22, Article ID 222902, 2006.

[77] R. Thomas, J. J. Saavedra-Arias, N. K. Karan et al., "Thin films of high-k dysprosium scandate prepared by metal organic chemical vapor deposition for metal-insulator-metal capacitor applications," *Solid State Communications*, vol. 147, no. 7-8, pp. 332–335, 2008.

[78] M. Roeckerath, J. M. J. Lopes, E. Durğun Özben et al., "Gadolinium scandate as an alternative gate dielectric in field effect transistors on conventional and strained silicon," *Applied Physics A*, vol. 94, no. 3, pp. 521–524, 2009.

[79] E. Durğun Özben, J. M. J. Lopes, M. Roeckerath et al., "SmScO3 thin films as an alternative gate dielectric," *Applied Physics Letters*, vol. 93, no. 5, Article ID 052902, 2008.

[80] P. Myllymäki, M. Roeckerath, M. Putkonen et al., "Characterization and electrical properties of high-k GdScO3 thin films grown by atomic layer deposition," *Applied Physics A*, vol. 88, no. 4, pp. 633–637, 2007.