

Research Article

Multilayer Inorganic Electrets with SiO_2 and Si_3N_4 Layers for Applications on Heated Machinery

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The physics and basic properties of electrets are discussed, namely, what happens during corona charging of dielectrics, why the surface potential and trapped charge show certain limits, where the trapped charge is stored, why and how the charge is released from traps at high temperatures. The experiments have been conducted on single-layer SiO_2 and Si_3N_4 and on multilayer combination of these materials. A strong lateral mobility of charge trapped near the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface was observed at elevated temperatures. The positively and negatively charged electrets are compared to each other. The experiments on charge retention at elevated temperatures have shown the studied electrets are suitable for devices working at temperatures of up to 200–300°C.

1. Introduction

Electrets could serve as a quasipermanent source of polarization in emerging applications like electrostatic energy harvesters [1]. This would allow autonomous devices powered by energy harvesters in applications, where temperatures of up to 200–300°C are observed and, thus, batteries cannot be used as a source of power. Electrets also used, or can be used, in other applications, for example, sensors, transducers, and electrostatic microbearings and micromotors [2, 3]. The inorganic electrets composed of at least one SiO_2 layer and one Si_3N_4 layer show superior charge retention at elevated temperatures. However, the physics of electrets is not understood well enough at this moment. For example, attempts to pattern them result in instability of trapped charge at small feature size of a pattern [3]. It is obvious that better understanding of the processes occurring during and after electret charging, influence of atmospheric ions and fringing field [4], effects of temperature [4–7], and humidity and relevant surface conduction [3, 8, 9] on charge retention is necessary. It would allow designing better microdevices with electrets suitable for the market with its requirements for the long lifetime of electrets (and therefore the devices), small feature size of photolithographic pattern, and the extended temperature range in applications.

This research is primarily targeted at development of electrostatic energy harvesters. They must be able to work for at least 10 years in applications with temperatures of 150–200°C and survive occasional short overheating to about 300°C. Therefore, organic electrets that discharge at much lower temperatures are not suitable for the application. The single-layer electrets dramatically discharge at 300°C either [4, 10]. Therefore, the only remaining option in this work was the $\text{SiO}_2/\text{Si}_3\text{N}_4$ electret. However, for studying the basic electret properties, the single layers of these materials were fabricated either.

2. Corona Charging of Single- and Double-Layer Electrets

When dealing with electrets, the first question is where the charge is trapped (near the electret surface or in the bulk) and how many traps can be charged per unit volume of an electret. Typically, electrets are charged with a tip-grid corona apparatus, and the potential in an electret is controlled by the grid potential. In case where the grid potential exceeds the breakdown voltage of the electret [6, 7], the maximum surface potential still has a certain limit. Therefore, an additional question arises, namely, what limits

the surface potential in such case, either the trap density or the breakdown field of the electret. The trap density reported for Si_3N_4 widely ranges from 10^{18} to $1.7 \times 10^{19} \text{ cm}^{-3}$ [11–14], as was obtained in studies of nonvolatile memories. It may also be extracted using the data reported in [5, 15] on the charged $\text{SiO}_2/\text{Si}_3\text{N}_4$ electret. It ranges approximately from $2.7 \times 10^{18} \text{ cm}^{-3}$ to $3.8 \times 10^{18} \text{ cm}^{-3}$, which is within the ranges reported in [11, 13], but by a factor of 2.5 to 4 less compared with the minimum trap density obtained in [12, 14]. The trap density in the bulk of SiO_2 was not reported, to the best of our belief, but it can be evaluated from the data presented in the literature for the room temperature conditions. Based on [16], it is about $1.5 \times 10^{17} \text{ cm}^{-3}$. However, using the data reported in [17] one arrives to a value of about $4.5 \times 10^{18} \text{ cm}^{-3}$ for positively charged SiO_2 and essentially higher value for the negatively charged layer, that is, by a factor of at least 30 higher than in [18].

In the works reporting on $\text{SiO}_2/\text{Si}_3\text{N}_4$ electret at room temperature, the charge was found to be located in the nitride, close to the electret surface. The mean distance of charge of about 8 to 9 nm from the nitride surface was reported in [5, 15, 18], where 150 nm of Si_3N_4 were deposited on 300 nm of SiO_2 . However, in the same work [18], a mean distance of about 72 nm from the substrate was reported for a 150 nm thick Si_3N_4 electret, that is, the layer was almost uniformly charged across its thickness. In case of SiO_2 electret, the reported results show a broad range of distances to the substrate, either. In [16], the mean charge distance from the substrate was found at 850 nm in a 1000 nm thick oxide, and thus approximately 300 nm thick layer was charged. In contrary, [17] reports the about 990 nm distance from the substrate (in the oxide of the same thickness) in the positively charged electret and even larger distance in the negatively charged one, that is, it was found that all charge is stored practically near the electret surface.

In this work, a new simple method of determination of charged trap density and mean distance of charge was developed and applied to electrets. To determine these parameters, the charge, Q , supplied by the corona to the electret is measured through measuring the corona current. The charge location, namely, the mean distance of charge from the substrate, d , is obtained from the surface potential in the electret, V_s , as

$$d = \frac{\epsilon_0 \epsilon A V_s}{Q}, \quad (1)$$

where ϵ_0 is the permittivity of vacuum, ϵ is relative permittivity, and A is the charged area. The method works if either the surface potential is less than the maximum potential that could be obtained on a particular electret, or the sample is larger than the area charged in the corona charger.

In the experiment, samples were positively charged in a corona apparatus with a tip potential of 10 kV and a grid potential of 1.5 kV. This is the so-called rapid corona charging method, where the grid potential always exceeds the target surface potential in an electret. The high grid potential allows reaching the surface potential unlimited by

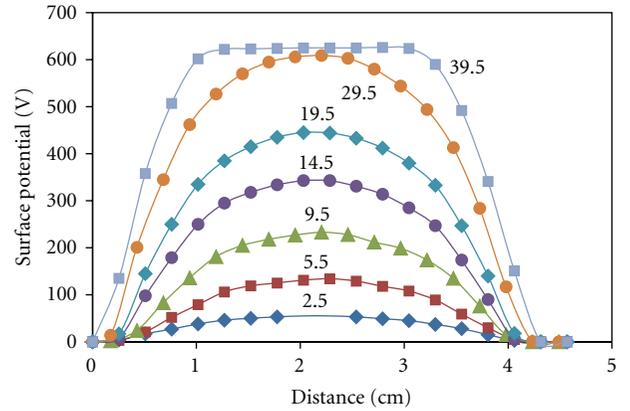


FIGURE 1: Surface potential on the charged zone of a SiO_2 sample with dimensions of $5.5 \text{ cm} \times 6 \text{ cm}$. Numbers indicate the charging time in seconds.

the former. The maximum surface potential in such case becomes limited only by the breakdown of the dielectric.

For the first experiment, a 1000 nm thick SiO_2 layer was fabricated on 6-inch wafers using thermal wet technique. A p-type Si with a resistivity of $20\text{--}30 \Omega \text{ cm}$ was used for the deposition. Two types of samples were studied, with and with no HMDS coating. There was no effect of HMDS layer on characteristics studied in this section. The sample was charged several times for a short period, with intermediate measurements of the surface potential. The sample with the size exceeding $5 \text{ cm} \times 5 \text{ cm}$ represented almost a quarter of a 6-inch wafer, while the charged area was smaller. The measurements show the current through the substrate during charging is near constant from the very beginning of charging to its end, when the surface potential increase under the tip ceases. The potential profile across the circular charged area was measured in x - and y -direction. Figure 1 shows the example of obtained surface potential over the central part of a larger sample at different charging times. In the beginning, the charging current density under the tip reaches its maximum, forming a bell-shaped charge profile. Upon reaching the maximum surface potential, a large amount of ions is deflected by the electret field to the edge of charging area. Therefore, by the end of charging, most of charge is trapped around already charged zone, in proximity to its edge. Figure 2 shows the dependence of average current density on radius from the center of charged area at different time after beginning of charging. Despite constant corona current, the trapped charge integrated over the charged area starts to deviate from the charge calculated using corona current and charging time (Figure 3). The difference represents tunneling current through the SiO_2 layer, which is expectable because the electret approaches its breakdown field.

The calculated charge trapped in the electret enables extraction of its mean distance from the substrate using (1). Figure 4 shows that the charge is trapped at a certain distance from the substrate, which varies with charging time, or, actually, with surface potential. This distance reflects the mean distance of the trapped charge. Assuming that the

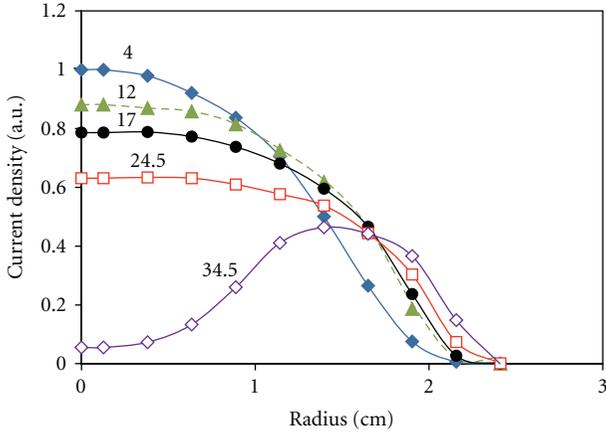


FIGURE 2: Dependence of normalized charging current density on radius from the center of charging area measured on a large-size SiO₂ sample. Numbers indicate the charging time in seconds.

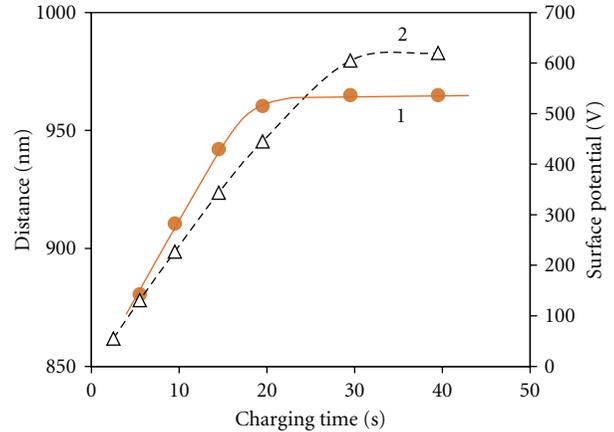


FIGURE 4: Dependence of the mean distance of trapped charge from the substrate (1) on charging time of SiO₂ electret. As in Figure 3, the surface potential (2) is shown for the reference.

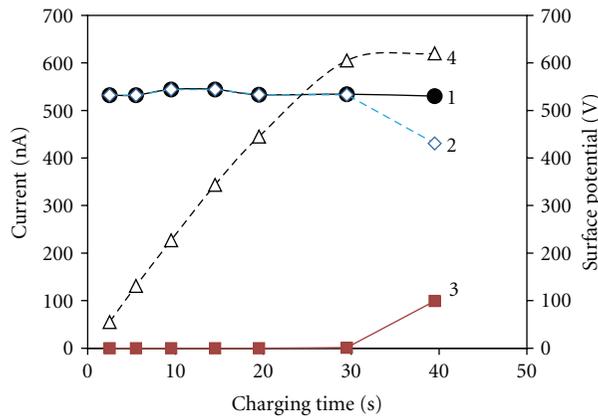


FIGURE 3: Dependence of corona current (1), the current charging traps (2), and the tunneling current through the SiO₂ electret (3) on charging time. For the reference, the surface potential (4) is shown in the middle of charged area.

charge is uniformly distributed over the charged top zone of SiO₂ layer, the thickness of the zone is 240 nm after 10 s of charging, which is close to the value reported in [16]. However, it decreases to about 70 nm when the surface potential saturates, that is, when the electret approaches the breakdown field. It seems logical that the bottom zone of the charged layer starts to discharge first in this case because it is located in higher field. The electrons tunneling through the potential barrier at the substrate—SiO₂ interface [19], must reach this zone first and neutralize the bottom traps.

The charge trap density is estimated in Figure 5 under assumed uniform distribution of charge across the charged layer. As far as one can hardly expect such a distribution, the actual density of traps in the layer close to the electret surface may actually exceed the density shown in Figure 5, while in the bottom of the layer it should decrease. The maximum trap density reaches $2 \times 10^{18} \text{ cm}^{-3}$, which is still by a factor of two less than was extracted above from the data presented in [17]. The variability of the charge distance and trap density shown in Figures 4 and 5 eliminates apparent contradiction

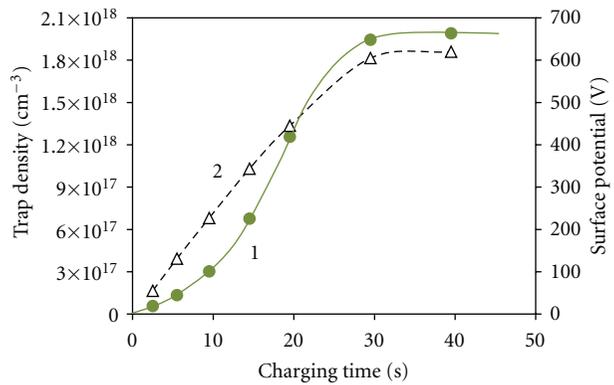


FIGURE 5: Dependence of the estimated density of charged traps (1) and the surface potential (2) on charging time of a SiO₂ electret.

between the data presented in [16, 17]. It can be explained by the difference in surface potential (which was, by the way, not reported in [16]).

The charging experiment as described above has also been conducted on the SiO₂/Si₃N₄ and Si₃N₄ electrets. The nitride was deposited using LPCVD technique. Once Si₃N₄ instead of SiO₂ forms the electret surface, one may expect the same or thinner charged layer because the reported range for trap densities extends to higher values. Indeed, the maximum trap density reached in the experiment performed in this work on 150 nm-thick Si₃N₄ electret was $4.4 \times 10^{18} \text{ cm}^{-3}$, close to the values reported in [11, 13] and those extracted above using the data reported in [5, 15]. The mean distance of charge from the substrate was about 124 nm, that is, about 50 nm out of 150 were charged near the electret surface.

The electret composed of 1060 nm SiO₂ and 150 nm Si₃N₄ showed the results quite similar to those reported in Figures 1–3. However, further analysis of the data uncovered certain difference. The obtained charge trap density by the end of charging is $4.6 \times 10^{17} \text{ cm}^{-3}$, that is, it is several times lower than in a single-layer Si₃N₄ and SiO₂. Upon reaching maximum surface potential, the mean distance of the trapped charge from the substrate was about 1060 nm,

that is, it coincided with the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface. This means that at the end of charging, the charge was approximately equally shared between two layers: the nitride and oxide. It was shown earlier [15, 20] that anneal of $\text{SiO}_2/\text{Si}_3\text{N}_4$ electret at a temperature of 400–450°C removes charges in the bulk of both layers. The remaining charge of about 70% of initial one is located near the interface. Therefore, it is believed that the interface features a kind of deep traps, both positive and negative, that are not discharged at those temperatures. The practical use of short anneal of an electret allows creation of a fine pattern of trapped charge for applications in microsystems [4, 10].

3. The Charge Trapped Near the $\text{SiO}_2/\text{Si}_3\text{N}_4$ Interface

Typically, for application in devices, a charge pattern must be formed in an electret. In [4], the charge pattern in the $\text{SiO}_2/\text{Si}_3\text{N}_4$ electret was formed in the following way. The Si_3N_4 layer was patterned using photolithography and formed lines on the oxide. The latter remained unpatterned. The electret was charged with corona, and zones with SiO_2 layer acquired a certain potential that was however lower than in the zones with $\text{SiO}_2/\text{Si}_3\text{N}_4$ [10]. The charged sample was annealed at 350°C to 450°C according to the technological process described in [21]. The annealing removed the trapped charge in the bulk of SiO_2 and Si_3N_4 . After annealing, the charge was observed only in the zones with Si_3N_4 , that is, with the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface. As was shown, the dielectric layer between charged elements of a pattern is necessary for charging narrow lines of a pattern because the presence of grounded conductive substrate results in deviation of corona ions and narrow lines could not be effectively charged in such case. Furthermore, an unpatterned oxide is needed for providing stable charge retention after fabrication [4, 10]. However, even upon optimization of the technology in [10], the charge in narrow lines was still lower than in wide lines. Therefore, in [4], the charging time on lines with a width of down to 20 μm was increased and allowed fabrication of such lines with the same potential as in mm wide lines. This variation of charging time is impossible if the charged elements with different widths are required in the same device. Therefore, in this work, the study of charge trapped near the interface has been conducted. Furthermore, in many applications, the electret charge should not degrade at elevated temperatures, such as those observed on the machinery. Therefore, attention has been paid to studying charge behavior at high temperatures.

The samples discussed in this section represent two- to four-layer unpatterned electrets with alternating oxide-nitride structure. They were fabricated on 6-inch wafers using thermal growth and TEOS (tetraethylorthosilicate) for deposition of the first and second SiO_2 layer, respectively, and LPCVD technique for Si_3N_4 and $\text{Si}_3\text{N}_{4-x}$ (silicon-rich). The samples with dimensions of 2 cm \times 4 cm have been cleaved from the wafers (Table 1).

The samples were charged to about 80–90% of the maximum potential obtainable on electrets. Then, the sample

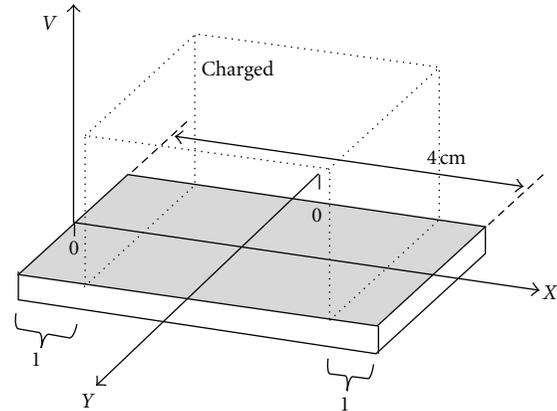


FIGURE 6: The schematics of a charged sample and location of trapped charge. The sample is discharged at its left and right edges, typically in about 6 ± 1 mm wide areas (1).

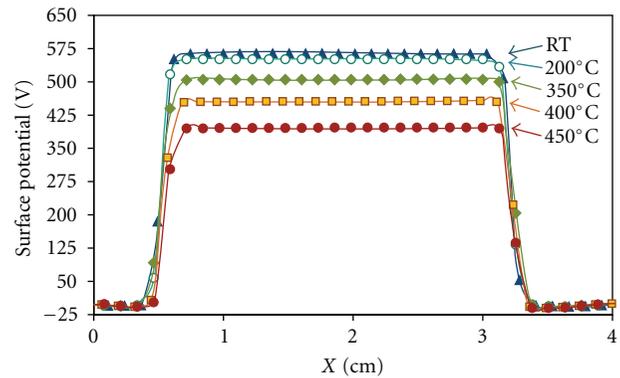


FIGURE 7: Decrease of the surface potential in the ON-2-type electret caused by a sequential anneal for 10 min at different temperatures, from room temperature (RT) to 450°C. Before the experiment, the sample was discharged in the water from left and right for 6–7 mm.

was partially deepened into a tap water for 1 min at its two ends, Figure 6. This procedure discharges electret and forms a sharp step of charge. The remaining charged zone of samples was about (2–3) cm \times 2 cm. After charging, the surface potential was measured along x - and y -axes. In the beginning of the experiment, the samples were annealed in air for 10 min at different temperatures. The charge gradually detraps with temperature (Figure 7). Upon annealing at 450°C, no charge remains in the bulk of SiO_2 and Si_3N_4 , and the remaining charge is located near their interface.

After that, the electrets were left in the oven for 110 hrs at a temperature of 450°C with periodic intermediate measurements of the potential profile. The results obtained on ON-1, ON-2, and ONON electrets were similar and showed activation of in-plane charge mobility. A typical dependence of charge decay is shown in Figure 8 for the same sample as in Figure 7.

The profile measurement along x -axis allows observation of the effect of sharp step in surface potential, while the measurement in y -direction gives an idea about the effect

TABLE 1: The electrets studied at elevated temperatures.

| Electret type | Layer sequence, material, and thickness, nm | | | |
|---------------|---|--|-----------------------------|--------------------------------------|
| | 1st | 2nd | 3rd | 4th |
| ON-1 | SiO ₂ , 450 | Si ₃ N ₄ , 150 | — | — |
| OSRN | SiO ₂ , 450 | Si ₃ N _{4-x} , 150 | — | — |
| ON-2 | SiO ₂ , 1000 | Si ₃ N ₄ , 150 | — | — |
| NO | Si ₃ N ₄ , 150 | TEOS SiO ₂ , 450 | — | — |
| ONO | SiO ₂ , 450 | Si ₃ N ₄ , 150 | TEOS SiO ₂ , 450 | — |
| ONON | SiO ₂ , 450 | Si ₃ N ₄ , 150 | TEOS SiO ₂ , 450 | Si ₃ N ₄ , 150 |

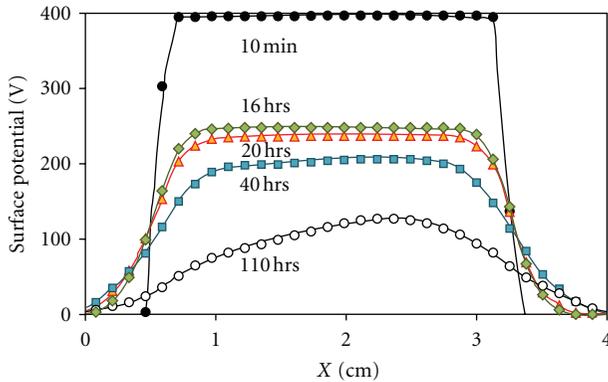


FIGURE 8: The retrapping of charge stored near the SiO₂/Si₃N₄ interface in ON-2 electret from the charged zone to uncharged side areas at different anneal time at a temperature of 450°C.

of sample edges. Figure 9 illustrates changes in the profile of potential along y -axis on the same sample ON-2.

The profile measurement along x -axis allows observation of the effect of sharp step in surface potential, while the measurement in y -direction gives an idea about the effect of sample edges. Figure 9 illustrates changes in the profile of potential along y -axis on the same sample ON-2.

As seen in Figure 9, at a temperature of 450°C the charge is lost through the sample edges. This could be attributed either to field emission from the edge of substrate [4] or to tunneling of charge carriers through the decreased potential barrier height at the sidewall surface of SiO₂. Therefore, the slope of detrapped charge shown in Figure 8 at 16 hr- to 110 hr-anneal is determined only by distance from the charged zone to the sample edge. To verify this hypothesis, a wider area of up to 10–12 mm, was discharged on some samples. Indeed, the slope always extended to the sample edge. Therefore, at a temperature of 450°C, in-plane charge retrapping in positively charged ON, ONO, and ONON electrets is huge, it is limited by the sample size.

Assuming that thermally activated trap-to-trap tunneling is the reason for such retrapping, varying the average distance between adjacent trap sites may affect the extent of this process and activation temperature. The simplest way to verify this is decreasing of trap-to-trap distance. It was done by fabricating a silicon-rich OSRN sample, where more trapping centers were created compared to stoichiometric Si₃N₄. Surprisingly, this afforded incredible change in activation temperature. Figure 10 shows that

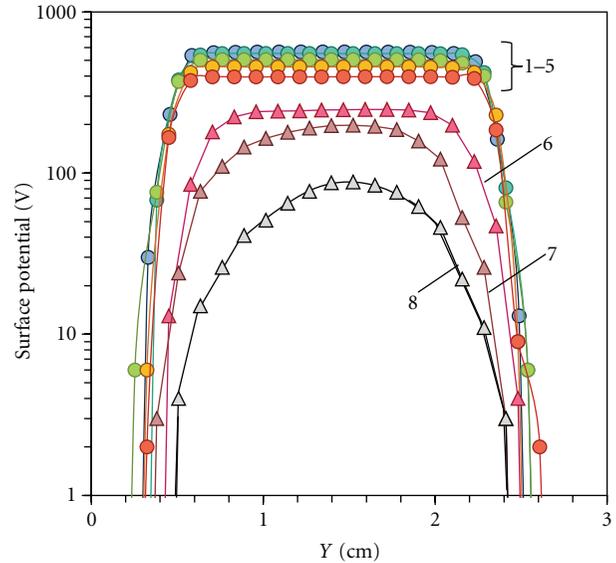


FIGURE 9: The profile of surface potential in ON-2 electret across the sample along y -axis as-fabricated (1), its decrease caused by the sequential anneal for 10 min at temperatures of 200, 350, 400, and 450°C, (2) to (5), respectively, followed by its anneal at a temperature of 450°C for 16 hrs (6), 40 hrs (7), and 110 hrs (8). The sample is 2 cm wide.

retrapping on the scale of millimeters starts already at 350°C. Unlike with stoichiometric Si₃N₄, Figures 7–9, the sample has reached the substrate-size-limited retrapping distance already after 10 min anneal at 450°C. By the next measurement procedure, after 16 hr-anneal, the sample completely lost charge through the sample edges (Figure 10). Indeed, comparison with Figure 7 shows that the dependence of potential on temperature in OSRN sample is weaker than in ON sample. The only explanation of its faster discharge is lateral mobility of charge.

To check whether the proposed method of charge step formation does not affect in-plane retrapping, another sample of OSRN electret was charged through a slit cut in aluminum foil, placed in proximity to the sample. Such way of charging does not provide sharp step of potential; therefore, the anneal time at 450°C was increased to 15 min for observation of the spatial retrapping. As seen in Figure 11, the charge mobility in such sample is the same as in the sample discharged in water.

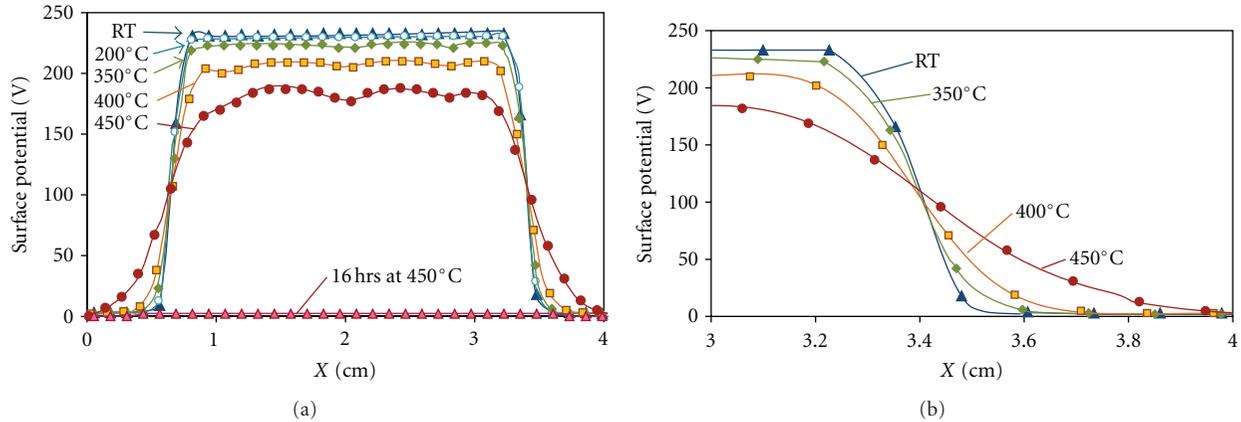


FIGURE 10: Dependence of in-plane retrapping of charge in OSRN electret. The initially trapped charge (RT) slowly decreases in the middle of the sample during 10 min anneal at different temperatures, but effectively moves in direction of sample edges. This in-plane mobility of charge located in Si_3N_4 electret close to the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface completely discharges the sample in less than 16 hrs anneal at 450°C . Shown are the surface potential over the sample (a) and the step of potential in detail (b).

The results discussed above raise the question whether the so-called “deep charge traps at the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface” exist. If the traps, indeed, deep enough, for example, having an energy of 2 eV and more, thermal energy would not be enough to activate in-plane charge retrapping between them. Therefore, the potential barrier between SiO_2 and Si_3N_4 was assumed as the reason for charge retention at 450°C . For the relevant experiment, the layer sequence was inverted in NO electret. However, neither retrapping nor any difference with single-layer SiO_2 and Si_3N_4 electrets was observed in the experiment. This confirms our guess that there are no deep charge traps at the interface. The charge in ON, OSRN, ONO, and ONON electrets is stored at high temperature in the same traps as in single-layer films. However, the potential barrier between the oxide and nitride is a serious obstacle for charges to overcome. The charges in any single-layer inorganic electret film mobilize at least above $200\text{--}300^\circ\text{C}$. Such electrets discharge in direction of field, so no in-plane mobility of trapped charges happens on the scale of centimeters (except low-temperature surface conductivity related to water molecules or silanol groups at the electret surface). Once the potential barrier is placed on their way to the substrate, they gradually move to the sample edges directed by fringing field. Therefore, the discharge through sample edges becomes more effective way of electret discharging as compared with tunneling (direct or Fowler-Nordheim one) through the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface.

The experiments described in this section were also performed on negatively charged electrets. There are some differences in charge trapping and detrapping. A slightly higher negative surface potential can always be obtained on the same sample type as compared with positively charged samples. However, after a 10 min anneal, negatively charged samples loose essentially more charge in the middle of charged zone, that is, the discharge through the potential barrier at the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface goes easier. This is in line with the observation that there are no deep charge traps near the interface. The difference is then explained just by different barrier height for electrons and holes. At a

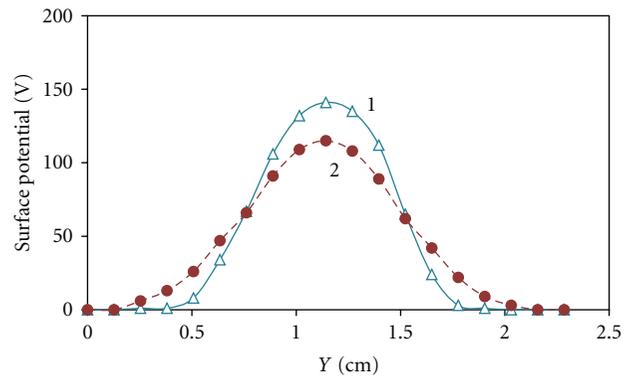


FIGURE 11: The profile of surface potential across the OSRN sample with a central zone charged through the slit in metal foil as-fabricated (1) and after anneal for 15 min at a temperature of 450°C (2).

temperature of 450°C , no retrapping in negatively charged electrets was observed. Instead, the samples were discharged from their edges, Figure 12 (to compare with Figure 9).

This result can be explained by Poole-Frenkel emission: detrapped electrons move freely in the conduction band in presence of fringing field. Therefore, at elevated temperatures, negatively charged electrets discharge faster near the sample edges than those positively charged.

4. Charge Retention at Elevated Temperatures

Three experiments were conducted in this work to characterize charge retention at elevated temperatures. Taking into account the results reported above, the NO-type electret was not studied. It was also found that the three-layer electret, ONO, shows no difference with ON-1 electret. The preliminary measurements have demonstrated deep mean charge location in ONO sample upon charging. Furthermore, after a 10 min anneal at 450°C , the remaining charge is collected near the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface that is located at the same

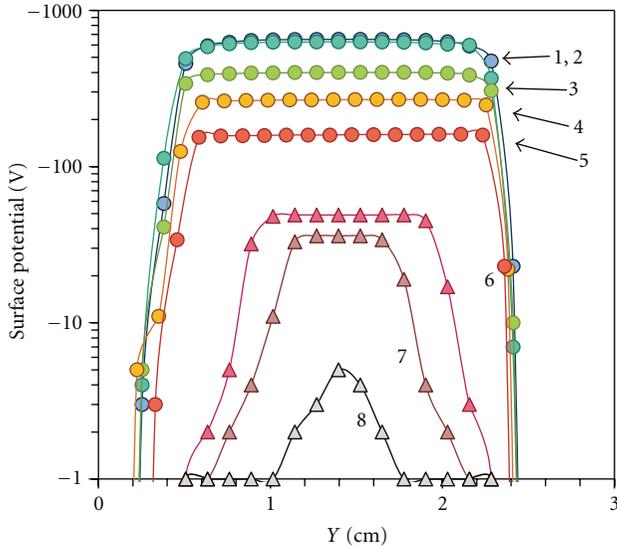


FIGURE 12: The untrapping of negative charge stored near the SiO₂/Si₃N₄ interface in ON-2 electret near the sample edges. The fabricated sample was charged (1), and sequentially annealed for 10 min at temperatures of 200, 350, 400, and 450°C, (2) to (5), respectively, followed by its anneal at a temperature of 450°C for 16 hrs (6), 40 hrs (7), and 110 hrs (8). The sample is 2 cm wide.

distance of 450 nm from the substrate as in ON-1 electret. Therefore, ONO was not studied further either.

The dependence of surface potential on temperature was measured using sequential anneal of samples for 10 min. The comparative results for positively and negatively charged electrets are shown in Figure 13. The negative charge is higher after charging, but the positive charge is more stable above 200°C.

In the second experiment performed at 450°C, the samples were stored in the oven for 110 hrs with intermediate measurements of surface potential. The comparative results for positively and negatively charged electrets are shown in Figure 14. The positive charge is more stable at this temperature. If negatively charged samples were much larger, for example, a whole wafer was charged, the charge retention in the middle of such sample would be about the same (but at lower surface potential) as in positively charged samples. However, especially in microsystems, such sample size is impossible. Therefore, negatively charged electrets are good or even more preferable for applications at room temperature, but positively charged electrets are certainly better for both applications at temperatures of 200–300°C and in patterned structures in microsystems.

The last experiment has been performed at a constant temperature of 200°C. After anneal at 450°C for discharging of shallow traps, the samples have been stored in the oven for 11 days. Initial surface potential in the positively and negatively charged samples was different, which is caused by different charge retention at 450°C. The experiment revealed no change in surface potential. The only one sample, ON-2, has demonstrated 1 V loss. This loss corresponds to a lifetime of about 12 years. The minimum detectable change

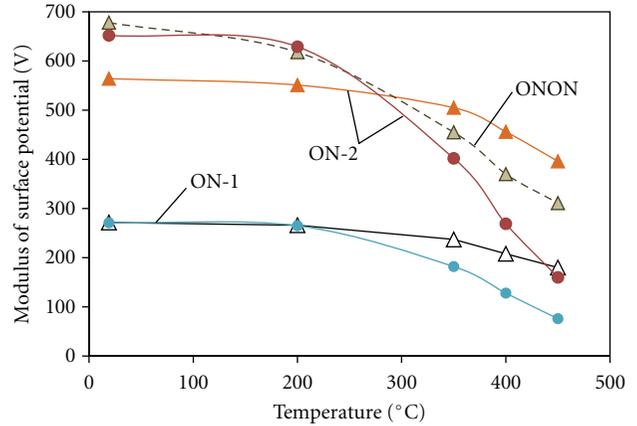


FIGURE 13: Comparative discharging of positively (triangles) and negatively (circles) charged electrets caused by a 10 min anneal at different temperatures.

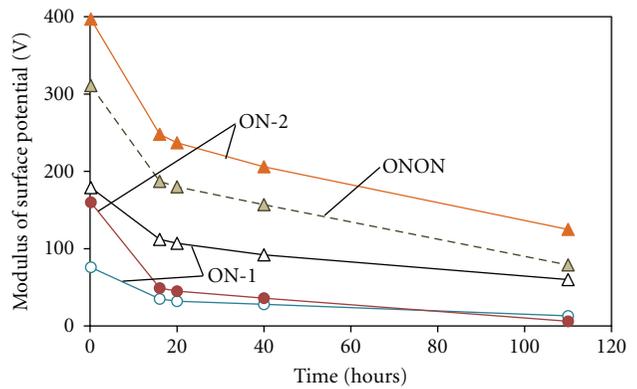


FIGURE 14: Comparative discharging of positively (triangles) and negatively (circles) charged electrets at a temperature of 450°C.

in potential in the experiment was 0.5 V. Assuming that an undetectable potential loss of 0.4 V has happened, that is, in the worst-case scenario, the estimated lifetime of charge in the studied electrets is of the order of or more than about 10 years. In patterned structures, the thermally stimulated in-plane retrapping (in positive electrets) or detrapping (in negative ones) could be much more profound, and further study is required.

5. Conclusion

The study of inorganic electrets performed in this work shows that most of charge is trapped within the certain distance from its surface. However, the thickness of charged layer depends on material and available trap density. In a 3-layer electret ONO, the charge is located very deep, which can decrease electret vulnerability to surface conduction. However, it is not better than 2- or 4-layer electrets of the same thickness in high-temperature applications. In 4-layer electret ONON, the charge seems to be almost equally shared between two SiO₂/Si₃N₄ interfaces (counted from the substrate side). This results in a larger decrease of potential at elevated temperatures. The maximum surface potential

is always limited by the breakdown field, and never by the amount of traps or trap density.

The thermally activated in-plane charge mobility observed in ON, ONO, and ONON electrets is a strong argument that the so-called “deep charge traps at the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface” do not exist. It is believed at this moment that presence of a potential barrier at the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface is the only reason for charge retention in multilayer electrets at high temperatures, that is, when both materials, SiO_2 and Si_3N_4 , completely discharge. Additional confirmation was obtained with NO electret, where the layer sequence was inverted, that is, Si_3N_4 was deposited first. This electret, despite the same interface, has shown no deep interface traps.

The studied charge retention at elevated temperatures brings optimism concerning feasibility of electret-based microdevices working at high temperatures of up to about 400°C . Typically, a pattern of charge is required in such devices. The room temperature stability in patterned electret lines with a width of $20\ \mu\text{m}$ was demonstrated recently [4, 10]. Preliminary tests performed in this work have demonstrated that much smaller structures can successfully be charged either. In particular, the patterned and charged lines with a width of down to $1\ \mu\text{m}$ were formed in ON-1 electret using the processes reported in [21]. This indicates feasibility of microsystems with charged electrets. The studied electrets, especially positively charged, successfully sustain relatively short high-temperature processes such as wafer stacking and encapsulation. Taking into account that in-plane charge mobility in the $\text{SiO}_2/\text{Si}_3\text{N}_4$ electret is observed only at a temperature of 450°C , they are also expected to sustain temperatures of up to $350\text{--}400^\circ\text{C}$ for a much longer time in applications. For example, a failure in a machine or bearing with corresponding rise of its temperature will not destroy the electret in a microdevice located nearby. Therefore, even if batteries appear on the market for application temperatures exceeding 130°C (i.e., their present temperature limitation), the electret-driven energy harvester will still be much more reliable source of power in devices than a battery.

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