

Research Article

System-on-Package MHMIC Millimeter-Wave Frequency Synthesizer for 60 GHz WPANs

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We present a low-cost millimeter-wave frequency synthesizer with ultralow phase noise, implemented using system-on-package (SoP) techniques for high-data-rate wireless personal area network (WPAN) systems operating in the unlicensed 60 GHz ISM band (57–64 GHz). The phase noise specification of the proposed frequency synthesizer is derived for a worst case scenario of an 802.11.3c system, which uses a 64-QAM 512-carrier-OFDM modulation, and a data rate of 5.775 Gbps. Our design approach adopts commercial-of-the-shelf (COTS) components integrated in a low-cost alumina-based miniature hybrid microwave integrated circuit (MHMIC) package. The proposed design approach reduces not only the system cost and time-to-market, but also enhances the system performance in comparison with system-on-chip (SoC) designs. The synthesizer has measured phase noise of -111.5 dBc/Hz at 1 MHz offset and integrated phase noise of 2.8° (simulated: 2.5°) measured at 57.6 GHz with output power of +1 dBm.

1. Introduction

The current demand for high-definition video streaming as well as the need for high-data-rate transmission in the range of multigigabit/s, attracts the use of the 60-GHz unlicensed ISM band (57–64 GHz). The main reason for the interest in the 60 GHz ISM band is attributed to the availability of 7 GHz of unlicensed bandwidth. Furthermore, the high oxygen absorption, and line-of-sight use, of the 60 GHz band makes this band well suited for frequency reuse which increases the system capacity; in addition, it minimizes harmful cochannel interferences, and increases the security of communication.

Although the 60-GHz band has many advantages, the design of low-cost high-performance frequency synthesizers that meet the system requirements of low-phase noise presents a design challenge, particularly, when CMOS system-on-chip (SoC) is the technology to be used (see

Table 2 for comparison). Such a challenge is due to the lossy silicon-substrate of CMOS technology. This is the main reason for using GaAs-based COTS components in our proposed design. The advantage of SoP integration is that, it enables the realization of the passive components on the same substrate of the packaging. In addition, active devices can be selected from different technologies to optimize the system performance. As an example, CMOS components can be used for high-density logic and analog circuits, SiGe and GaAs for high-speed microwave circuits, and GaN for high power.

This paper will derive synthesizer phase noise specification and present design and measurements of the synthesizer. System analysis is performed in Section 2, with calculation of best-case SNR required. In Section 3 an analysis is performed on the influence of the phase noise on SNR and synthesizer requirements are derived. Section 4 discusses the proposed

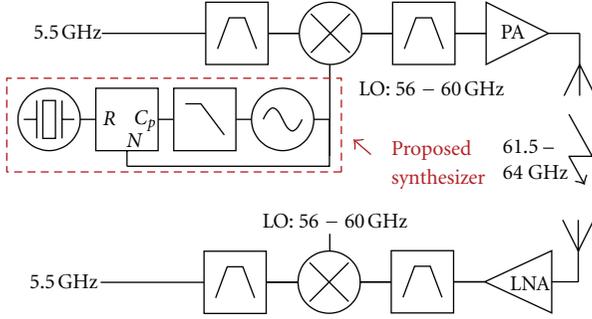


FIGURE 1: Diagram of the proposed downstream 60 GHz radio link, to be used for evaluation of 60 GHz system performance.

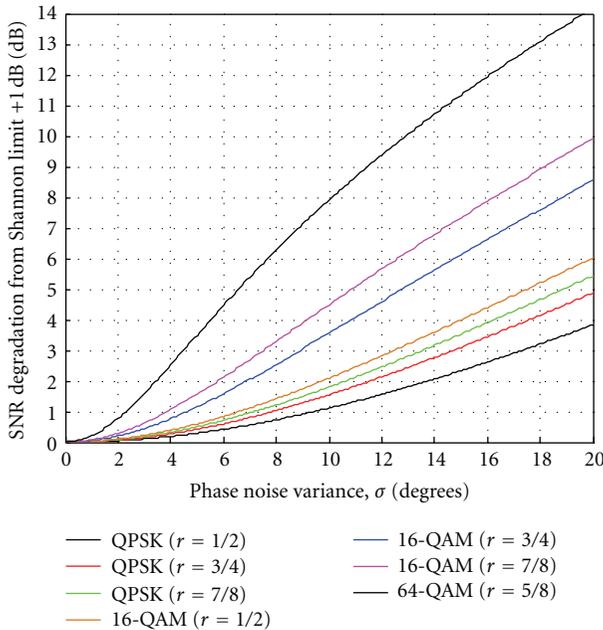


FIGURE 2: SNR degradation from phase noise for various modulation schemes and coding rates (HSI modes of 802.15.3c).

frequency synthesizer. Finally the measured data is presented in Section 5.

2. System Analysis

Before presenting the analysis and design of the synthesizer we need to understand how the synthesizer performance affects the overall system performance. The following sections will describe how the SNR of the system is derived from top level specifications and how the SNR is degraded by phase noise of the synthesizer, leading to synthesizer phase noise specification. The model presented here begins with an ideal case and builds on the nonidealities of various system components and the effect each has on the degradation of SNR. This work begins by presenting the system's link budget, followed by peak power requirement, and finally by phase noise degradation of SNR.

TABLE 1: Summary of system specifications.

Specification type	Specification value
Distance	10 m
Bit Error Rate	10^{-6}
Antenna gain	8 dBi (TX), 24 dBi (RX) [1]
Antenna parameters	Perfect copolarization. Line of sight. Beam steering is assumed to achieve desired gain.
Channel model	Rician fading channel based on [1, 2] used in Path Loss.
Transmit power	27 dBi EIRP average, 27 dBm peak [3]
Receiver noise figure (NF)	6 dB (2 dB worse than min. reported for 60 GHz applications [4])
Nominal bandwidth	1.815 GHz (data + pilot tones)
PAPR ^a coding	Worst case is assumed: with no PAPR-reducing coding

^aPeak-to-average power ratio.

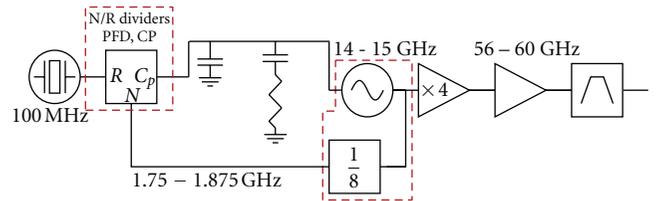


FIGURE 3: Block diagram of the proposed 60 GHz synthesizer. Highlighted blocks are individual IC's.

2.1. System Overview. The proposed synthesizer is designed to be used in an experimental setup (shown in Figure 1) to test transmission in the 60-GHz range. For simplicity, the setup would take several channels from 802.11n (5.5 GHz) signal and upconvert them to 60 GHz.

2.2. Link Budget. Following the standard specifications for 802.15.3c [5] the required system specifications is derived. The required path loss of the radio link is considered next. First we define the system specifications in Table 1.

Using the path loss equation in [1] the path loss (PL) is calculated to be 90.4 dB. From Table 1. the received signal power is 19 dBm (27 dBm EIRP-8 dBi). The maximum achievable SNR for the receiver is 36 dB.

2.3. Peak Power Requirement. An OFDM signal has a higher peak-to-average power ratio (PAPR) than a single carrier (SC) signal. The worst case PAPR as a function of number subcarriers [6] is:

$$\text{PAPR}_{\text{dB}} = 10 \cdot \log_{10}(N). \quad (1)$$

For 802.15.3c HSI mode N is 352, and PAPR is 25.5 dB. This means that average power would have to be 25.5 dB below the 27 dBm peak power specified by FCC [3]. Therefore, the average transmit power would be 1.5 dBm (27 dBm-25.5 dB) due to peak power constraint. Maximum SNR for peak power requirement would degrade to 18.5 dB.

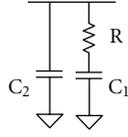
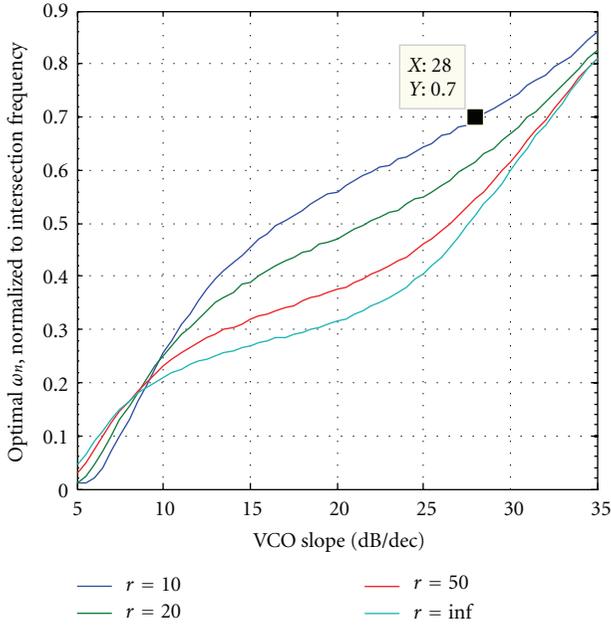
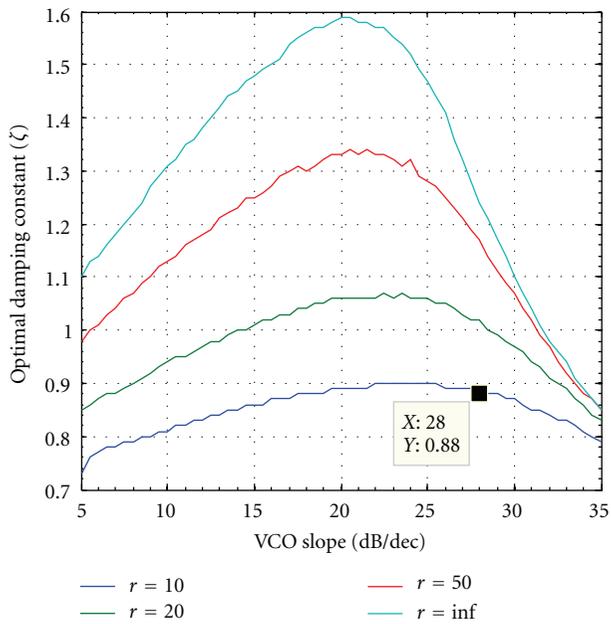


FIGURE 4: 2nd order loop filter used in PLL.



(a)



(b)

 FIGURE 5: ω_n normalized to intersection frequency (a) and damping constant ζ (b) of PLL loop filter for smallest integrated phase noise. r is the capacitance ratio of the 2nd order PLL loop filter.

TABLE 2: Loop filter parameters.

Parameter	Given values		Calculated values		
	Value	Units	Parameter	Value	Units
VCO Freq	14.4	GHz	ω_n	$0.7 \cdot \omega_x$	rad/s
K_{VCO}	$2\pi \cdot 200$	Mrad/V	ζ	0.88	
K_{LOOP}	5208		f_x	65	KHz
r	10		f_n	45.5	KHz
$\varphi_{REF-noise}$	-83	dBc/Hz	f_{3dB}	105	KHz
			C_1	65	nF
			C_2	6.5	nF
			R	100	Ω

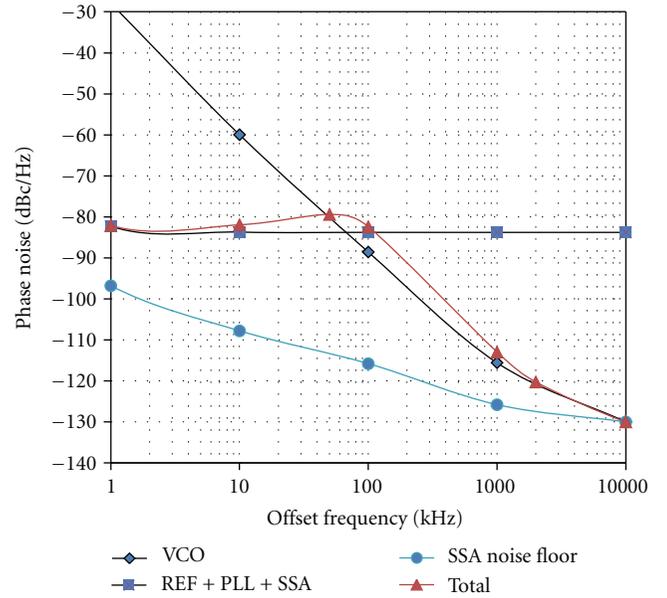


FIGURE 6: Total phase noise and open loop component phase noise (all normalized to 57.6 GHz) of VCO, reference with PLL chip and signal-source-analyzer noise floor. The intersection of VCO and reference/PLL phase noise curves is at 65 KHz.

3. Phase Noise Effect on SNR

According to [7] the SNR degradation due to phase noise in an OFDM signal can be calculated as follows:

$$\text{SNR}_{\text{with PN}} = \frac{e^{-4\sigma_\phi^2}}{1 - e^{-4\sigma_\phi^2} + 1/\text{SNR}_{\text{without PN}}}, \quad (2)$$

where σ_ϕ corresponds to the integrated phase noise in radians (also referred to as RMS jitter).

Since ECC can significantly change the required SNR, we need to look at the effect of SNR degradation due to phase noise at SNR levels required with ECC. low-density-parity-check (LDPC) coding, used in 802.15.3c, can get very close [8] to the Shannon limit. The SNR at Shannon limit is [9]:

$$\text{SNR}_{\text{min}} = 10 \cdot \log_{10}(2^{r \cdot M} - 1), \quad (3)$$

where r is code rate, M is constellation size ($M \times M$ QAM).

TABLE 3: Comparison of measured results.

Reference, publication date, SoC or SoP	Phase noise at 1 MHz offset, dBc/Hz	Integrated phase noise (RMS jitter) ^a
[10] May 2008, SoC	-91.6	5°
[11] Nov. 2010, SoC	-86.5	8°
[12] Feb. 2008, SoC	-86.8	58°
[13] Feb. 2008, SoP	-95.6	5°
This work, SoP	-111.5	2.8°

^aIntegrated from 1 KHz to 30 MHz. Based on piece-wise linear interpolation from phase noise plots, normalized to 57.6 GHz.

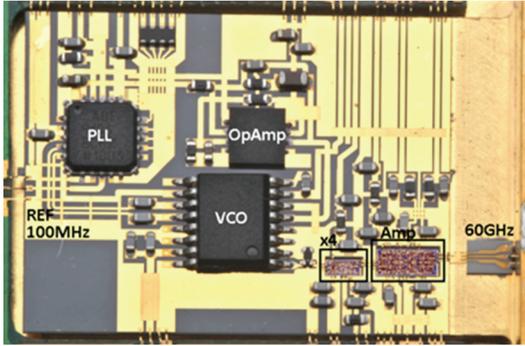


FIGURE 7: Populated MHMIC synthesizer board 1.7 cm × 2.3 cm.

LDPC coding can achieve SNR values as close as 1 dB from the Shannon limit [8]. Allowing us to see how phase noise would influence ECC-coded signal using (2) and (3). This is shown for various modulation schemes and code rates (Figure 2).

The SNR at Shannon limit for code rate 5/8 64-QAM signal is 15 dB (SNR_{min} from (3)). By adding LDPC encoding we expect it to increase to 16 dB. The SNR margin would then be 18.5 dB - 16 dB = 2.5 dB. From Figure 2 this means that the system can tolerate 4° of RMS jitter while still conforming to specifications in Table 1.

4. Synthesizer Design

4.1. PLL Design. For simplicity a standard PLL topology [14] is used as shown in Figure 3.

For better phase noise a maximum channel spacing of 3.2 GHz is chosen, based on 100 MHz PFD frequency.

The proposed synthesizer uses COTS components for reference crystal oscillator, dividers, phase-frequency detector (PFD), loop filter, 14-15 GHz VCO, ×4 multiplier, and output amplifier.

4.2. PLL Loop Filter Design. Loop filter is chosen to be a commonly used 2nd order integrator-lead RC filter [14]. Higher order filters have been simulated producing no noticeable improvement on overall phase noise. The loop filter topology in is employed as shown in Figure 4.

The loop bandwidth and loop damping constant are optimized based on the VCO slope, C_1/C_2 capacitance ratio

(r) for which a rule of thumb value of 10 is used, and the fact that the reference + PLL phase noise is nearly thermal around the loop 3 dB frequency. Using MATLAB, a sweep of loop natural frequency (ω_n) and damping constant (ξ) is performed for various VCO slopes and r 's. The ω_n and ξ values producing smallest integrated phase noise are shown in Figure 5.

Based on the plots of Figure 5, and using the fact that VCO has a slope of 28 dB/dec and with capacitance ratio of 10, the optimal ω_n/ω_x and ξ are 0.7 and 0.88, respectively, where ω_x is intersection of open loop phase noise of VCO and the reference, which is at $2\pi \cdot 65$ KHz (Figure 6). From this, loop component values that produce minimal integrated phase noise are calculated using [14]. The result is shown in Table 2.

4.3. PLL Component Selection. The PLL components are selected based on simulation of their phase noise contributions to meet the specifications:

- (i) crystek CVHD-950-100 VCXO;
- (ii) the PLL chip: ADF4106 from Analog Devices;
- (iii) hittite HMC398QS16G VCO and HMC-XDH158 ×4.

The plot in Figure 6 shows component phase noise based on open loop measurements illustrating loop bandwidth selection.

4.4. Implementation. The reference, DC supplies, and digital control signals are provided from an PCB board, which is connected to the MHMIC SoP with bond wires. The 60 GHz output signal is bond-wired from the amplifier to a coaxial V-connector. The synthesizer with populated components is shown on Figure 7.

5. Measurements

The synthesizer phase noise is measured at 57.6 GHz with a Rohde & Schwarz FSUP signal source analyzer. The plot in Figure 8 shows measured phase noise versus simulated.

Table 3 compares measured phase noise with published measurements (all normalized to 57.6 GHz).

The power consumption of VCO and ×4 multiplier is 2.1 W, which makes the applications of the proposed synthesizer suitable to large size installations such as set-top boxes, kiosks, and point-to-point radios.

6. Conclusions

A cost-effective high-performance SoP synthesizer is designed and manufactured based on the derived phase noise requirements from system analysis. Worst case 802.15.3c MCS-index-7 signal is used for derivation of SNR. The worst case SNR is derived to be 18.5 dB for 10 m link with BER of 10^{-6} . The Integrated phase noise specification is derived to be 4°. The synthesizer has been designed and manufactured in MHMIC process which exceeds this

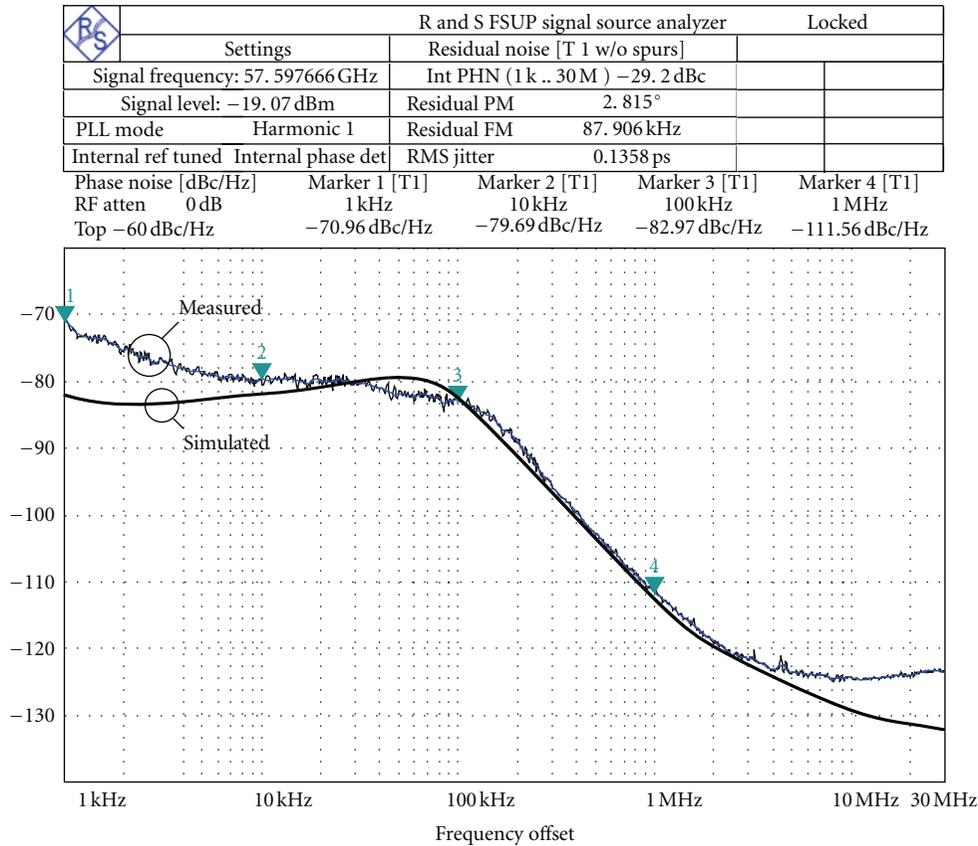


FIGURE 8: Phase noise measurement and simulation of the synthesizer at 57.6 GHz, locked to 100 MHz reference. Measured integrated phase noise is 2.8° (integrated in 1 KHz–30 MHz offset), simulated: 2.5°. Output power is +1 dBm.

specification, achieving phase noise of -111.5 dBc/Hz (1 MHz offset) and the integrated phase noise of 2.8° at 57.6 GHz, degrading SNR by only 1.8 dB. To authors' knowledge this is the best phase noise reported, at the time of writing, at frequency close to 60 GHz.

Acknowledgments

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