Hindawi Publishing Corporation
ISRN Electronics
Volume 2013, Article ID 125746, 5 pages
http://dx.doi.org/10.1155/2013/125746

Research Article

Voltage-Mode Universal Biquadratic Filter Using Single DVCC

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Received 14 January 2013; Accepted 11 February 2013

Academic Editors: M. Hopkinson and J.-Y. Sim

A voltage-mode universal biquadratic filter using a differential voltage current conveyor (DVCC), two capacitors, and two resistors is presented. The proposed circuit has four input terminals and three output terminals and can realize all the standard filter functions, which are lowpass, bandpass, highpass, notch, and allpass filters, without changing the circuit topology. Three simultaneous output filter responses can be obtained from some derived filter types. The proposed circuit employs only one DVCC that simplifies the configuration.

1. Introduction

Recently, there is a growing interest in designing current-conveyor- (CC-) or current-feedback-amplifier- (CFA-) based active filters. This is attributed to their high signal bandwidths, greater linearity, and larger dynamic range than OPAMP-based ones [1]. Note that a CFA is equivalent to a plus-type second-generation current conveyor (CCII) with a voltage follower [2].

Active filters are so widely used in electronic systems, such as telecommunications, radar, consumer electronics, instrumentation systems, and military ordnance, [1, 3]. Many voltage-mode universal biquadratic filters with multi-inputs were proposed [4–10]. From the different combinations of injection of input voltage signals, voltage-mode lowpass, bandpass, highpass, notch, and allpass filters can be obtained without changing the circuit topology. However, these circuits require at least two active components. Moreover, the universal biquadratic circuits in [4, 7–9] require one more active component for the unity-gain inverting input in the allpass realizations. In 2002, Horng et al. proposed a universal biquad with four inputs using three resistors, two capacitors, and one CFA [11]. However, it still requires one more active component for the unity-gain inverting input in the allpass realization. Two voltage-mode universal biquads each with three inputs using two resistors, two capacitors, and one CCII were presented in [12, 13]. However, each of these two circuits requires one more active component for amplifying the input signal in the notch and allpass realizations. A voltage-mode universal biquadratic filter using single plus-type CCII (CCII+), two resistors, and two capacitors was presented in [14]. However, only two standard filter types can be obtained simultaneously in the same circuit.

In this paper, a voltage-mode universal biquadratic filter circuit that has four input terminals and three output terminals is presented. It can realize all the standard filter functions, which is, lowpass, bandpass, highpass, notch, and allpass filters, without changing the circuit topology. With respect to the previous single active element universal biquad in Horng et al. [11], the proposed circuit employs less passive components does not need one more active component for the unity-gain inverting input in the allpass realization and the availability of two more simultaneous output filter responses from some derived filter types. With respect to the previous single CCII universal biquads in [12, 13], the proposed circuit does not need one more active component for amplifying the input signal in the notch and allpass realizations. With respect to the previous single CCII+ universal biquad in [14], one more simultaneous output filter response can be obtained from some derived filter types.

2. Proposed Circuit

The port relations of a CCII can be characterized by $v_x = v_y$, $i_z = \pm i_x$, and $i_y = 0$. The CCII has a disadvantage that only one of the input terminals has high-input impedance

(the y terminal). The differential difference current conveyor (DDCC) [15] and DVCC [16] are extensions of the CCII and are specially defined to handle differential input voltage signals. Using standard notation, the port relations of a DDCC can be characterized by $v_x = v_{y1} - v_{y2} + v_{y3}$, $i_{zk} = \pm i_x$, and $i_{y1} = i_{y2} = i_{y3} = 0$; the port relations of a DVCC can be characterized by $v_x = v_{y1} - v_{y2}$, $i_{zk} = \pm i_x$, and $i_{y1} = i_{y2} = 0$. Considering the proposed voltage-mode circuit in Figure 1, the output voltage functions can be expressed as

$$\begin{aligned}
V_{o1} &= \left(\left(s^2C_1C_2 + sC_2G_1 - sC_2G_2\right)V_{in3} + sC_1G_2V_{in2}\right.\\
&\quad \left. + G_1G_2V_{in1} + \left(-sC_1G_2 - G_1G_2\right)V_{in4}\right)\\
&\quad \times \left(s^2C_1C_2 + s\left(C_1G_2 + C_2G_1 - C_2G_2\right)\right.\\
&\quad \left. + G_1G_2\right)^{-1},\\
V_{o2} &= \left(-sC_2G_2V_{in3} + \left(s^2C_1C_2 + sC_1G_2\right)V_{in2}\right.\\
&\quad \left. + \left(sC_2G_1 + G_1G_2\right)V_{in1} - sC_2G_2V_{in4}\right)\\
&\quad \times \left(s^2C_1C_2 + s\left(C_1G_2 + C_2G_1 - C_2G_2\right)\right.\\
&\quad \left. + G_1G_2\right)^{-1},\\
V_{o3} &= \left(\left(-s^2C_1C_2 - sC_2G_1\right)V_{in3} + s^2C_1C_2V_{in2}\right.\\
&\quad \left. + sC_2G_1V_{in1} + \left(sC_1G_2 - sC_2G_2 + G_1G_2\right)V_{in4}\right)\\
&\quad \times \left(s^2C_1C_2 + s\left(C_1G_2 + C_2G_1 - C_2G_2\right)\right.\\
&\quad \left. + G_1G_2\right)^{-1}.
\end{aligned} \tag{1}$$

From (1), we can see that thirteen circuit types can be obtained from Figure 1.

(a) If $V_{in2} = V_{in3} = V_{in4} = 0$ (grounded), V_{in1} = input voltage signal, a lowpass filter can be obtained at V_{o1} and a bandpass filter can be obtained at V_{o3}.

(b) If $V_{in1} = V_{in3} = V_{in4} = 0$ (grounded), V_{in2} = input voltage signal, a bandpass filter can be obtained at V_{o1} and a highpass filter can be obtained at V_{o3}.

(c) If $V_{in1} = V_{in2} = V_{in4} = 0$ (grounded), V_{in3} = input voltage signal and $R_2 = R_1$, a highpass filter can be obtained at V_{o1} and a bandpass filter can be obtained at V_{o2}.

(d) If $V_{in1} = V_{in2} = V_{in3} = 0$ (grounded), V_{in4} = input voltage signal and $C_2 = C_1$, a bandpass filter can be obtained at V_{o2} and a lowpass filter can be obtained at V_{o3}.

(e) If $V_{in2} = V_{in4} = 0$ (grounded), $V_{in1} = V_{in3}$ = input voltage signal and $R_2 = R_1$, a notch filter can be obtained at V_{o1}, a lowpass filter can be obtained at V_{o2}, and a highpass filter can be obtained at V_{o3}.

(f) If $V_{in2} = V_{in4} = 0$ (grounded), $V_{in1} = V_{in3}$ = input voltage signal and $2C_2G_2 = C_1G_2 + 2C_2G_1$, an allpass filter can be obtained at V_{o1} and a highpass filter can be obtained at V_{o3}.

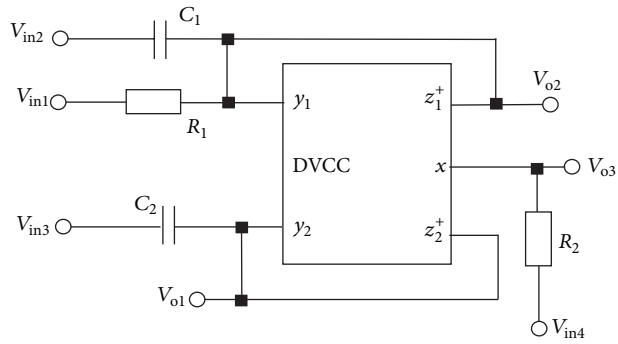

Figure 1: The proposed voltage-mode universal biquad.

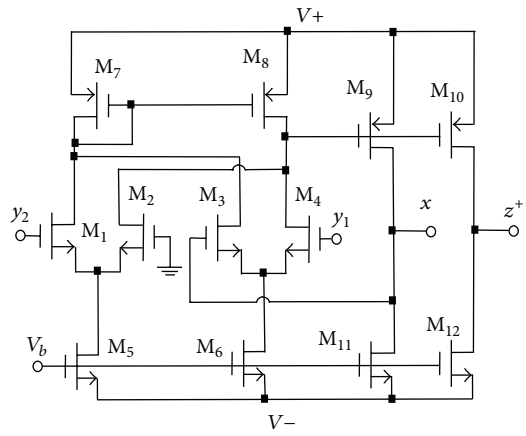

Figure 2: The CMOS DVCC implementation.

(g) If $V_{in2} = V_{in3} = 0$ (grounded), $V_{in1} = V_{in4}$ = input voltage signal and $R_2 = R_1$, a bandpass filter can be obtained at V_{o1} and a lowpass filter can be obtained at V_{o2}.

(h) If $V_{in1} = V_{in4} = 0$ (grounded), $V_{in2} = V_{in3}$ = input voltage signal and $C_2 = C_1$, a highpass filter can be obtained at V_{o2} and a bandpass filter can be obtained at V_{o3}.

(i) If $V_{in1} = V_{in3} = 0$ (grounded), $V_{in2} = V_{in4}$ = input voltage signal and $C_2 = C_1$, a lowpass filter can be obtained at V_{o1}, a highpass filter can be obtained at V_{o2} and a notch filter can be obtained at V_{o3}.

(j) If $V_{in1} = V_{in3} = 0$ (grounded), $V_{in2} = V_{in4}$ = input voltage signal and $2C_2G_2 = 2C_1G_2 + C_2G_1$, a lowpass filter can be obtained at V_{o1} and an allpass filter can be obtained at V_{o3}.

(k) If $V_{in1} = V_{in2} = 0$ (grounded), $V_{in3} = V_{in4}$ = input voltage signal, a bandpass filter can be obtained at V_{o2}.

(l) If $V_{in2} = 0$ (grounded), $V_{in1} = V_{in3} = V_{in4}$ = input voltage signal, $C_2 = C_1$, and $R_2 = 2R_1$, a highpass filter can be obtained at V_{o1} and a lowpass filter can be obtained at V_{o2}.

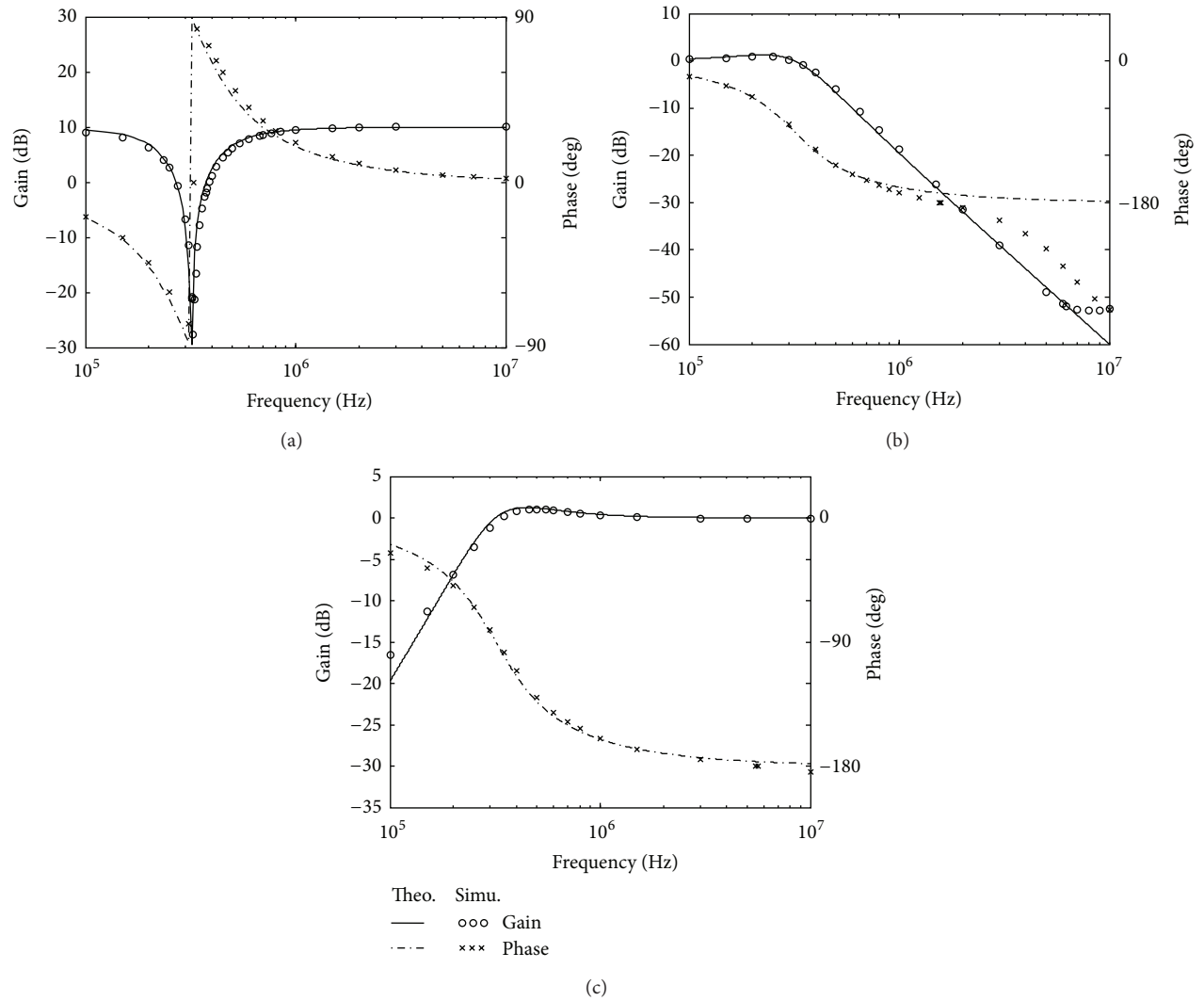

FIGURE 3: Simulated frequency responses of Figure 1 designed with $V_{in2} = V_{in4} = 0$ (grounded), $V_{in1} = V_{in3}$ = input voltage signal, $C_1 = C_2 = 50$ pF, and $R_1 = R_2 = 10$ kΩ: (a) notch filter (V_{o1}), (b) lowpass filter (V_{o2}), and (c) highpass filter (V_{o3}).

(m) If $V_{in1} = 0$ (grounded), $V_{in2} = V_{in3} = V_{in4}$ = input voltage signal, $R_2 = R_1$, and $C_2 = 0.5C_1$, a highpass filter can be obtained at V_{o2} and a lowpass filter can be obtained at V_{o3}.

Thus, the circuit is capable of realizing all voltage-mode filter functions. Note that three standard filter responses can be obtained simultaneously from the circuit types (e) and (i).

3. Nonideality Analysis of the DVCC

Taking into consideration the DVCC nonidealities, the port relations of DVCC can be expressed as

$$v_x = \alpha_1 v_{y1} - \alpha_2 v_{y2}, \qquad i_z = \pm\beta_k i_x, \tag{2}$$

where $\beta_k = 1 - \varepsilon_{ki}$ and ε_{ki} ($|\varepsilon_{ki}| \ll 1$) denotes the current tracking error from x terminal to z_k terminal of a DVCC, $\alpha_1 = 1 - \varepsilon_{v1}$ and ε_{v1} ($|\varepsilon_{v1}| \ll 1$) is the input voltage tracking error from y_1 terminal to x terminal of a DVCC, and $\alpha_2 = 1 - \varepsilon_{v2}$ and ε_{v2} ($|\varepsilon_{v2}| \ll 1$) is the input voltage tracking error from y_2 terminal to x terminal of a DVCC. The denominator of the nonideal output voltage function for Figure 1 becomes

$$D(s) = s^2 C_1 C_2 + s\left(C_1 G_2 \alpha_2 \beta_2 + C_2 G_1 - C_2 G_2 \alpha_1 \beta_1\right) + G_1 G_2 \alpha_2 \beta_2. \tag{3}$$

The resonance angular frequency and quality factor are obtained by

$$\omega_o = \sqrt{\frac{G_1 G_2 \alpha_2 \beta_2}{C_1 C_2}}, \qquad Q = \frac{\sqrt{C_1 C_2 G_1 G_2 \alpha_2 \beta_2}}{C_1 G_2 \alpha_2 \beta_2 + C_2 G_1 - C_2 G_2 \alpha_1 \beta_1}. \tag{4}$$

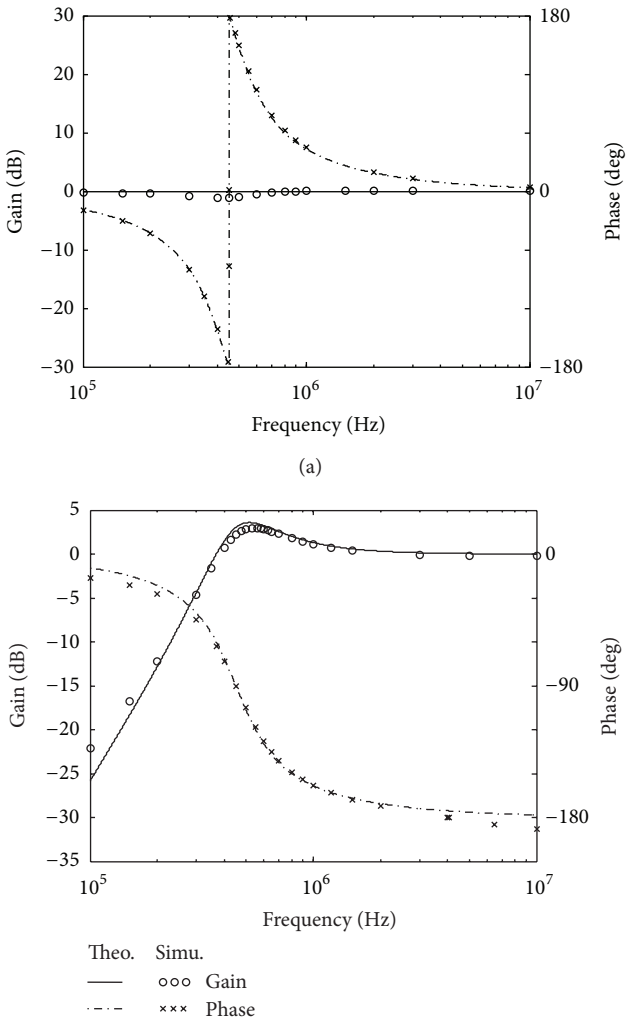

Figure 4: Simulated frequency responses of Figure 1 designed with $V_{in2} = V_{in4} = 0$ (grounded), $V_{in1} = V_{in3}$ = input voltage signal, $C_1 = C_2 = 50\,\text{pF}$, $R_1 = 10\,\text{k}\Omega$, and $R_2 = 5\,\text{k}\Omega$: (a) allpass filter (V_{o1}), and (b) highpass filter (V_{o3}).

The active and passive sensitivities are low and obtained by

$$S^{\omega_o}_{G_1,G_2,\alpha_2,\beta_2} = -S^{\omega_o}_{C_1,C_2} = \frac{1}{2},$$

$$S^{Q}_{C_1} \cong \frac{C_2G_1 - C_1G_2 - C_2G_2}{2\left(C_1G_2 + C_2G_1 - C_2G_2\right)},$$

$$S^{Q}_{C_2} \cong \frac{C_1G_2 + C_2G_2 - C_2G_1}{2\left(C_1G_2 + C_2G_1 - C_2G_2\right)},$$

$$S^{Q}_{G_1} \cong \frac{C_1G_2 - C_2G_1 - C_2G_2}{2\left(C_1G_2 + C_2G_1 - C_2G_2\right)},$$

$$S^{Q}_{G_2} \cong \frac{C_2G_1 + C_2G_2 - C_1G_2}{2\left(C_1G_2 + C_2G_1 - C_2G_2\right)},$$

$$S^{Q}_{\alpha_1,\beta_1} \cong \frac{C_2G_2}{C_1G_2 + C_2G_1 - C_2G_2},$$

$$S^{Q}_{\alpha_2,\beta_2} \cong \frac{C_2G_1 - C_1G_2 - C_2G_2}{2\left(C_1G_2 + C_2G_1 - C_2G_2\right)}. \quad (5)$$

4. Simulation Results

HSPICE simulations were carried out to demonstrate the feasibility of the proposed circuits using 0.18 μm, level 49 MOSFET from TSMC. The DVCC was realized by the CMOS implementation in Figure 2 [17] with the NMOS and PMOS transistor aspect ratios $W/L = 4.5\,\text{u}/0.9\,\text{u}$ and $W/L = 9\,\text{u}/0.9\,\text{u}$, respectively. The supply voltages are $V+ = +0.9\,\text{V}$, $V- = -0.9\,\text{V}$, and $V_b = -0.38\,\text{V}$.

Figures 3(a)–3(c) represent the simulated frequency responses for the notch (V_{o1}), lowpass (V_{o2}), and highpass (V_{o3}) filters of Figure 1, respectively, designed with $V_{in2} = V_{in4} = 0$ (grounded), $V_{in1} = V_{in3}$ = input voltage signal, $Q = 1$, and $f_o = 318.3\,\text{kHz}$: $C_1 = C_2 = 50\,\text{pF}$ and $R_1 = R_2 = 10\,\text{k}\Omega$.

Figures 4(a) and 4(b) represent the simulated frequency responses for the allpass (V_{o1}) and highpass (V_{o3}) filters of Figure 1, respectively, designed with $V_{in2} = V_{in4} = 0$ (grounded), $V_{in1} = V_{in3}$ = input voltage signal, $Q = 1.414$, and $f_o = 450.16\,\text{kHz}$: $C_1 = C_2 = 50\,\text{pF}$, $R_1 = 10\,\text{k}\Omega$, and $R_2 = 5\,\text{k}\Omega$.

5. Conclusions

In this paper, a new voltage-mode universal biquadratic filter has been presented. The new voltage-mode circuit with four input terminals and three output terminals employs two capacitors, two resistors, and one DVCC. The new circuit has the features of using only four passive components and does not need one more active component in the realizations of notch and allpass filters and the availability of three simultaneous output filter responses from some derived filter types (types (e) and (i)).

Acknowledgment

The National Science Council, China, supported this work under Grant no. NSC 101-2221-E-033-070.

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