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Research Article

FinFET Based Tunable Analog Circuit: Design and Analysis at 45 nm Technology

Ravindra Singh Kushwah[1] and Shyam Akashe[2]

[1] *ITM University, Gwalior 474001, India*
[2] *ECE Department, ITM University, Gwalior 474001, India*

Correspondence should be addressed to Ravindra Singh Kushwah; ravindrasinghkushwah@yahoo.com

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We included a designing of low power tunable analog circuits built using independently driven FinFETs devices, where the controlling of the back gate provide the output on the front gate. We show that this could be an effective solution to conveniently tune the output of bulk CMOS analog circuits particularly for Schmitt trigger and operational transconductance amplifier circuits. FinFET devices can be used to increase the performance by reducing the leakage current and power dissipation, because front and back gates both are independently controlled. FinFET device has a higher controllability, resulting relatively high I_{on}/I_{off} ratio. In this paper, we proposed a tunable analog circuit such as CMOS amplifier circuit, Schmitt trigger circuit, and operational transconductance amplifier circuit, these circuit blocks are necessary for low noise high performance ICs for analog applications. Gain, phase, group delay, and output response of analog tunable circuits have been discussed in this paper. The proposed FinFET based analog tunable circuits have been designed using Cadence Virtuoso tool at 45 nm.

1. Introduction

Scaling of the CMOS technology has moved to nanometer regime, and therefore the FinFETs have replaced the present technologies [1, 2]. FinFET has reduced short-channel effects (SCEs), higher trans-conductance, and ideal subthreshold voltage [3–5]. Whereas FinFETs are ideal for digital applications, they will also be powerful competitors for linear radio frequency (RF) applications such as wireless communication because of their capability to handle large terahertz modulation [6]. These circuits provide extra gains in terms of area, power and speed by using FinFET in independently driven mode because of its analog tunable functionality. Therefore the two gates are separated and biased as compared to symmetrically driven mode counterparts used in digital applications to maximize I_{on}/I_{off} ratio [7, 8]. Independently driven mode can be used to combine parallel FinFET transistors in noncritical paths, and therefore reduction in the power dissipation and effective switching capacitance is achieved. The tunability of the FinFETs has been predominately rejected by the analog designers because utilities of the FinFETs in RF mixing applications have been published [8–10]. In this work, we will realize various analog circuit blocks ramped up using FinFETs, where back gate will be used for the tuned circuit performance. We will show how compact low-power circuits including CMOS amplifier circuit, Schmitt trigger circuit, and operational transconductance amplifier circuit (OTA) may be built and tuned using Cadence Virtuoso tool at 45 nm complementary metal oxide semiconductor (CMOS) technology.

An overview of this paper is organized as follows. Section 2 shows a FinFET technology. Section 3 illustrates the device structure and modeling of analog tunable circuits. Section 4 describe the CMOS amplifier Circuit. Section 5 describes the Schmitt trigger circuit. Section 6 describes the operational transconductance amplifier (OTA) circuit. The final section draws the conclusions of this work.

2. FinFET Technology

Due to problems in aligning the front and back gates, as well as in building a low resistance to the back gate, DGFETs are difficult to fabricate. The FinFET has been developed to

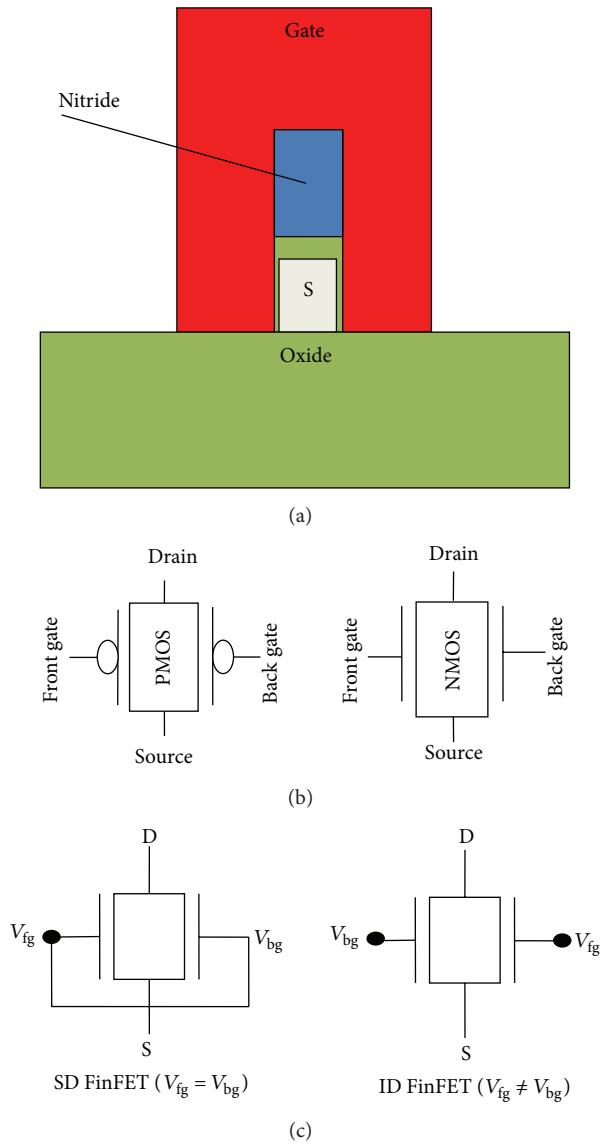


FIGURE 1: (a) Double gate FinFET, (b) shows the FinFET circuit symbols, and (c) the SD and ID refer to symmetrically and independently driven FinFET.

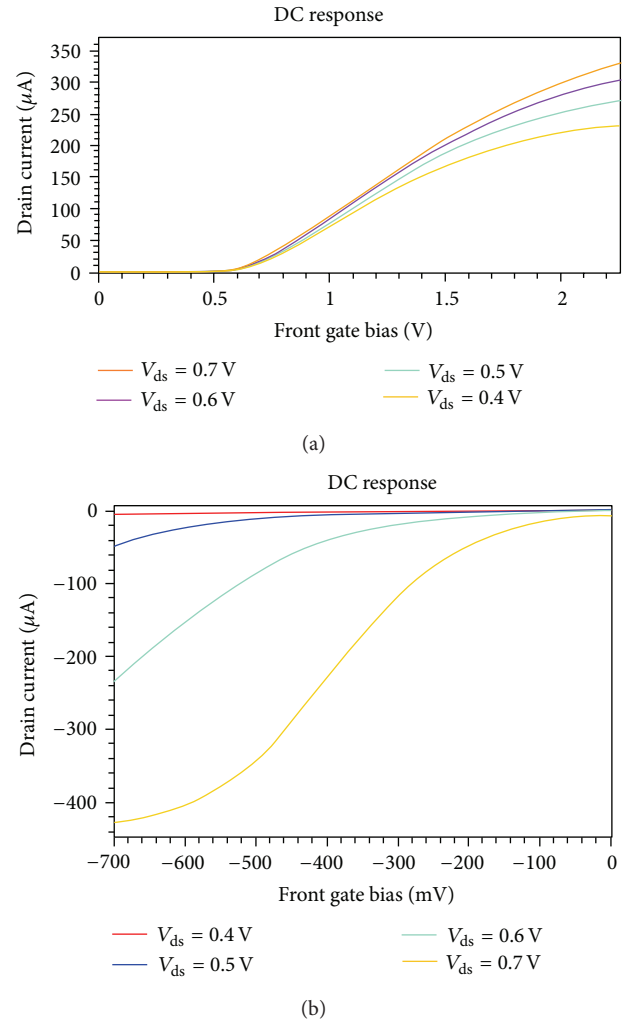
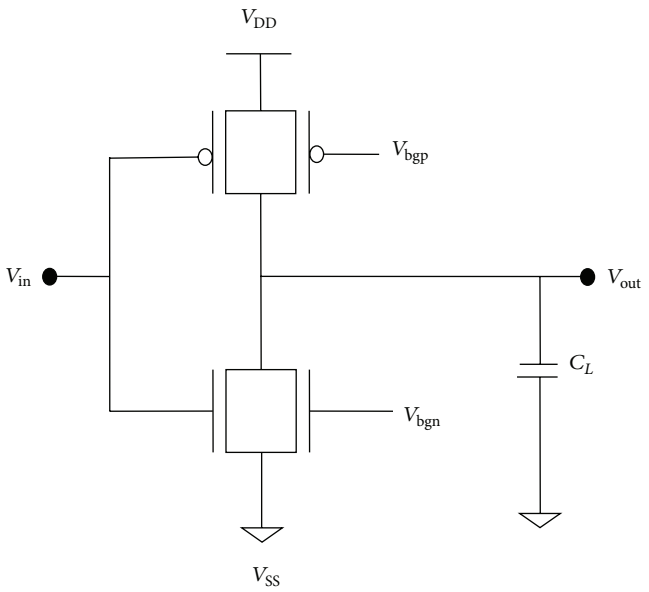


FIGURE 2: (a) The transfer characteristics of n-type FinFET with different back gate bias and (b) the transfer characteristics of p-type FinFET with different back gate bias conditions.

overcome the problems faced by DGFET. The structure of a FinFET with a cut-plane view across the fin is shown in Figure 1(a). To make a FinFET, the front oxide is made much thicker than the side oxides in order to effectively deactivate the front gate.

The FinFET is one such promising device which is considered to be a suitable successor DGFET winning over several of the hurdles mentioned over, while it is probable too to be made using a high-k gate dielectric and a metal gate. The structure of a FinFET is shown in Figure 1(a). It is called so because the thin channel region stands vertically similar to the fin of a sandwich between the source and drain regions. The gate covers around the body from three sides and therefore reduces short channel effects (SCEs). In strong inversion, conduction mainly arises along to the sidewalls, whereas in subthreshold it arises along the fin centre. A structured FinFET is actually a device in which 3D effects play a nonnegligible role (whereas reasonable mean that the fin height is higher but not considerably high than the fin width). Hence it is expected to focus on the 2D feature of the FinFET when developing a compact model. In other words, the fin height is assumed to be infinite. Thus all values derived in the model are on a per-unit-fin-height basis such as charges and currents. The device being modeled is thus deemed as a double-gate MOSFET (DGFET).

The width of a triple-gate FinFET is $W = 2H_{fin} + t_{fin}$. In many cases, t_{fin} is small in order to have suitably small SCE. Moreover, the front gate of FinFET is ineffective; therefore W is approximately $2H_{fin}$. As a result, the properties of a FinFET become higher similar to those of a DGFET. Thus, most of the invented story that discuss compact model development for DGFETs can be applied to FinFETs with a minor parameter (H_{fin}) adjustment. The long narrow portion of the fin that is not under the gate is called the extension region. This is



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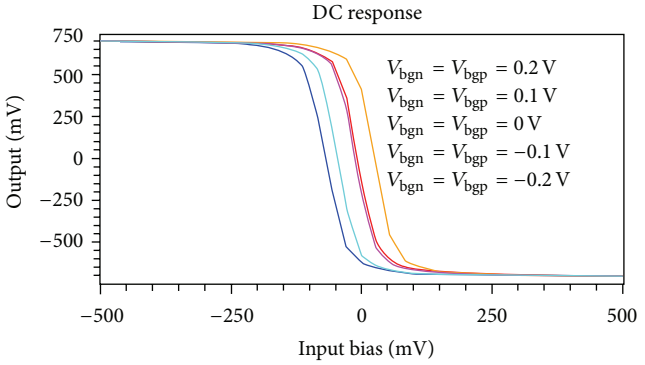

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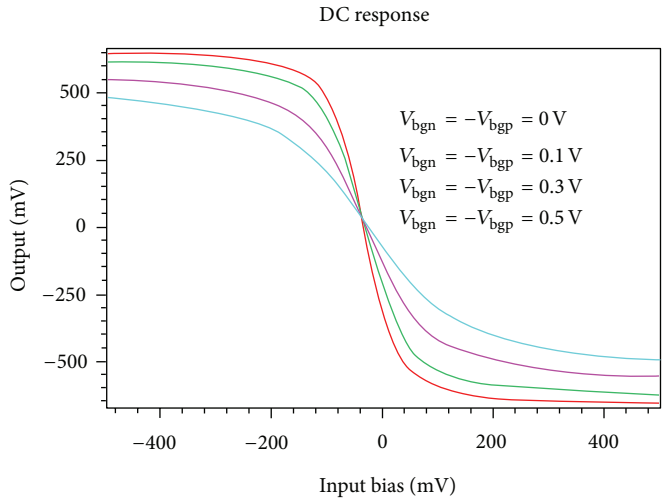

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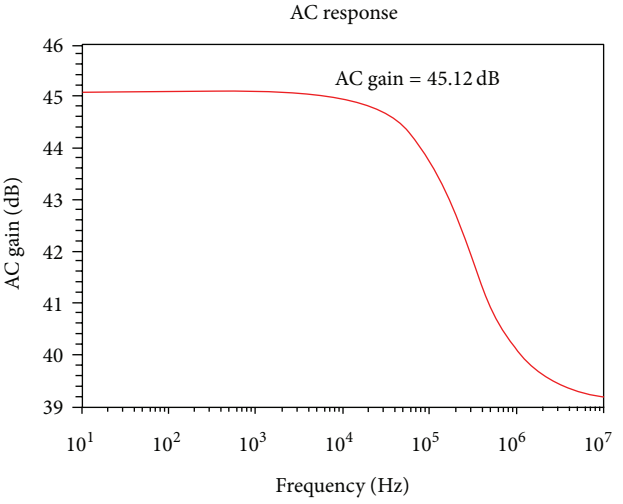

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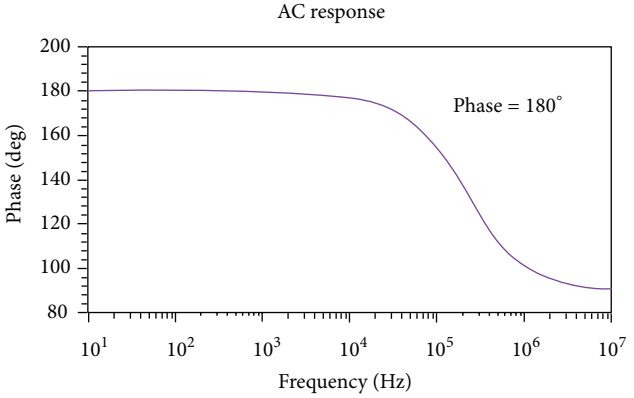

(e)

Figure 3: Continued.

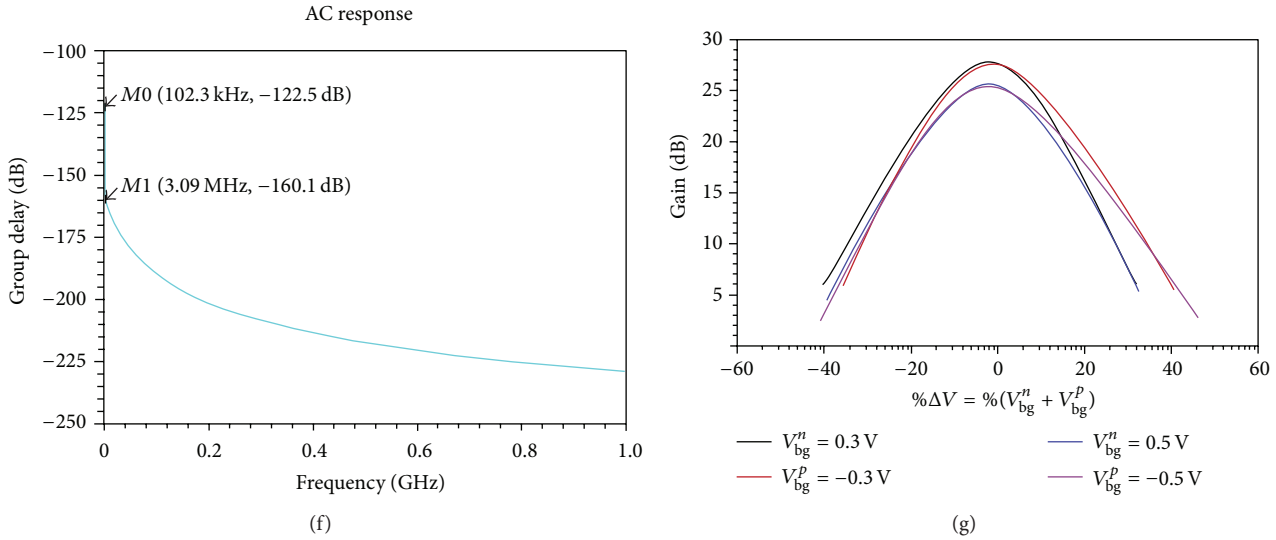

FIGURE 3: (a) A simple FinFET CMOS analog amplifier, (b) the response of a simple FinFET CMOS amplifier to setting the equal voltage on the back gates ($V_{bgn} = V_{bgp}$), (c) the response of a simple FinFET CMOS amplifier as a function of conjugate voltage on the back gate ($V_{bgn} = -V_{bgp}$), (d) the gain of a simple FinFET CMOS amplifier as a function of conjugate voltage on the back gate ($V_{bgn} = -V_{bgp}$), (e) the phase of a simple FinFET CMOS amplifier as a function of conjugate voltage on the back gate ($V_{bgn} = -V_{bgp}$), (f) the group delay of a simple FinFET CMOS amplifier as a function of conjugate voltage on the back gate ($V_{bgn} = -V_{bgp}$), and (g) the wave form of AC gain of conjugate biasing error.

a region that is technologically necessary, because it is not likely to have a vertical side doping gradient, starting from a highly doped source to drain and finishing with a lightly doped channel region. As a result, FinFETs typically have a relatively large parasitic series resistance.

3. Device Structure and Modeling of Analog Tunable Circuits

In this methodology, the FinFET is operating in two modes such as symmetrical driven and independent driven mode to design analog tunable circuits. In symmetrical driven mode, the front and back gates are connected together and in independent driven mode, separate biasing is provided to the front and back gates. FinFETs have minimum body thickness ($t_{si} \leq 8.4$ nm), oxide insulator thickness ($t_{ox} \leq 1.5$ nm), gate length ($L \leq 45$ nm), fin height ($H_{fin} \leq 65$ nm), supply voltage ($V_{DD} \leq 0.7$ V), and the maximum I_{on}/I_{off} ratio because of greater controllability to OFF state leakage current [11]. We optimized that both gates have same threshold voltage $V_{th} = \pm 0.25$ V using Cadence Virtuoso tool. Figures 1(b) and 1(c) shows the FinFET device structure and the circuit symbols for both p-type and n-type FinFET transistors. 2D simulations of this structure are achieved using Cadence Virtuoso simulation Tool.

Figures 2(a) and 2(b) show the transfer characteristics of both *n*-type and *p*-type FinFET, where controlling the back gate provide the drain current on the front gate. Therefore, the resulting independently driven devices are always inferior to symmetrical driven devices in terms of subthreshold and transconductance [12]. Due to controlling the tunability of back gate, the FinFET performance is reduced.

4. CMOS Amplifier Circuit

In present, the FinFET CMOS inverter is one of the important design blocks also for analog circuit designing. When it is biased in the transition region, it can provide as a high-gain push-pull amplifier. Depending on the sign and magnitude of the back gate biasing, the characteristics of the simple FinFET CMOS amplifier can be altered in many ways, which greatly improve various applications.

Figure 3(b) shows the response of a simple FinFET CMOS amplifier to setting some voltage on the back gates ($V_{bgn} = V_{bgp}$), thus resulting in relative changes in the voltage window for amplification. The relative changes in the voltage window can be used in analog wave-shaping circuits or in Schmitt triggers. Please note that the relative change in the voltage amplification in this circuit is determined by the intensity of the capacitive coupling through the back gate, which can be given by the choice of gate insulator thickness, dielectric constant, and body thickness in a given technology.

The alternative method for biasing the CMOS pair is conjugation, whenever the back gates are biased by separate signals of same magnitude but opposite sign ($V_{bgn} = -V_{bgp}$). In a mixed mode design using bipolar supply voltages, this biasing strategy is possible and provides the method of changing the amplifier gain that may be extremely suitable. Figure 3(c) shows gain of CMOS amplifier that is a function of the same voltage applied to both back gates with opposite

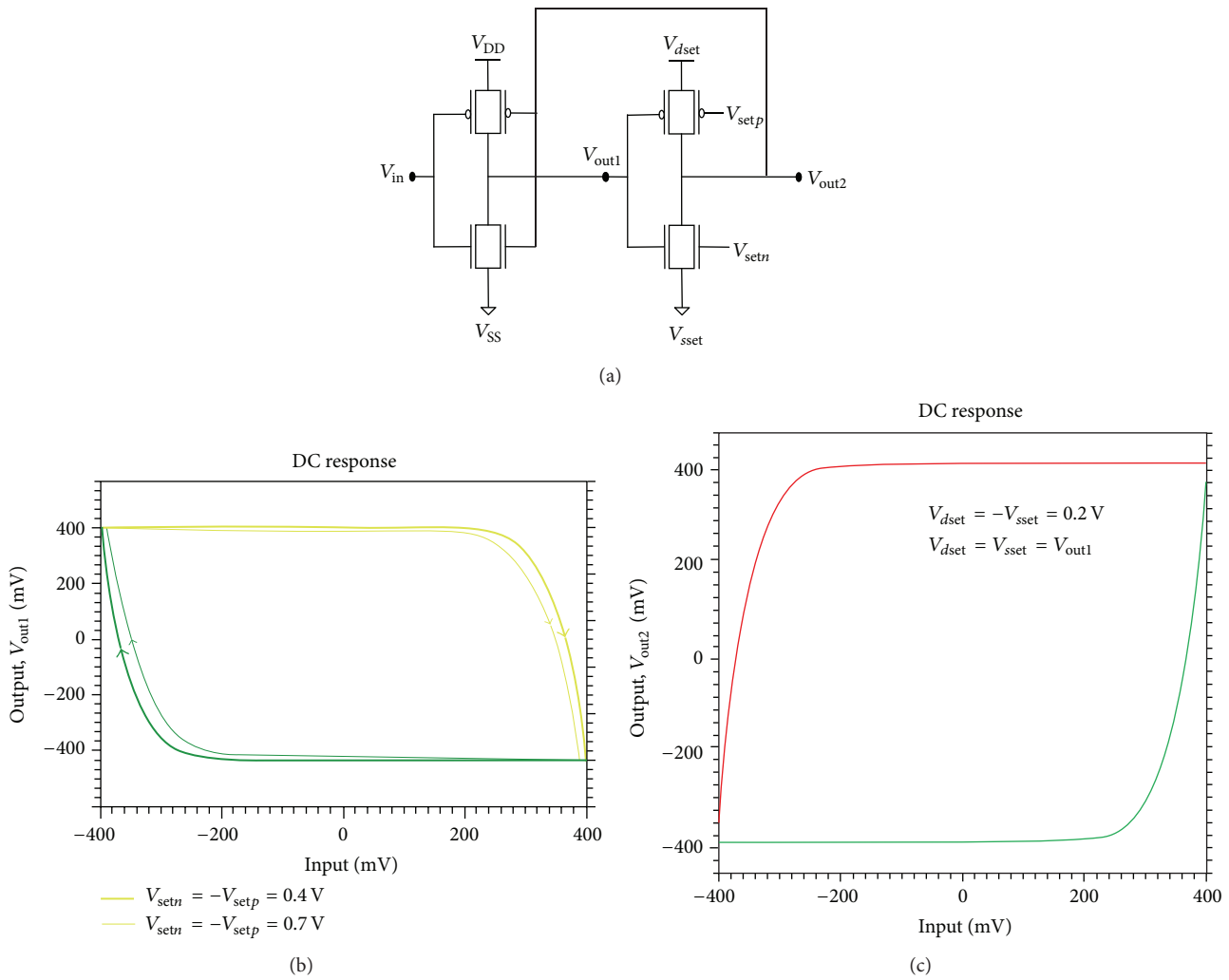

FIGURE 4: (a) A simple schmitt trigger Circuit using FinFET, (b) the simulated output of the schmitt trigger Circuit with control voltage $V_{setn} = -V_{setp} = 0.4$ V, and (c) the simulated output of the Schmitt Trigger Circuit with symmetric gate voltage $V_{setn} = V_{setp} = V_{out1}$.

polarity ($V_{bgn} = -V_{bgp}$) in the transition region, and therefore change in the output impedance dominates the intrinsic gain. In SD FinFET CMOS amplifier, the gain is larger without any bias control. The output of ID FinFET CMOS amplifier is decreased while the back gate channel is conducting whenever the top channel is off which can contribute larger leakage. The same problem occurs in self-feedback method; the output of the ID FinFET CMOS amplifier drives their back gates ($V_{bgn} = V_{bgp} = V_{out}$), which provides lower gain.

Figures 3(d), 3(e), and 3(f) show the AC analysis of ID FinFET CMOS amplifier where load capacitance of $C_L = 2$ pF is used. When the bandwidth is increased, gain and phase are linearly reduced as compared to the conjugate back gate bias. When the frequency is increased, group delay is increased. The highlinearity of FinFETs provided linear tuning response where the threshold voltage of each device is equal to 0.25 V. By using the conjugate biasing, it should provide fine tune frequency response of simple CMOS amplifier.

In practical implementation, errors are associated with conjugate biasing method as a result of limited accuracy of biasing networks and process variations. To measures this error for two examples as shown in Figure 3(g). For larger errors ($\%\Delta V > 10$), such bias imperfections can lead to considerable degradation of gain (>3.5 dB). However a more significant effect of this error is the poor linearity as a result of losses in the symmetry of gain curves in Figure 3(g). Therefore a relative change in intrinsic gain of every transistor now operates under different conditions.

5. Schmitt Trigger Circuit

Schmitt trigger circuit is a nonlinear analog circuit block; it is very useful to reduce noise in analog wave shaping circuits, control circuits, and digital circuits. In single gate (SG) MOSFET, the sizes of Schmitt Triggers are improved (to reduce the rise times and fall times of signals) due to increased layout area and power consumption of chips. FinFET Schmitt trigger has the ability to reduce layout area and power consumption and is used in static memory applications in digital circuits [13].

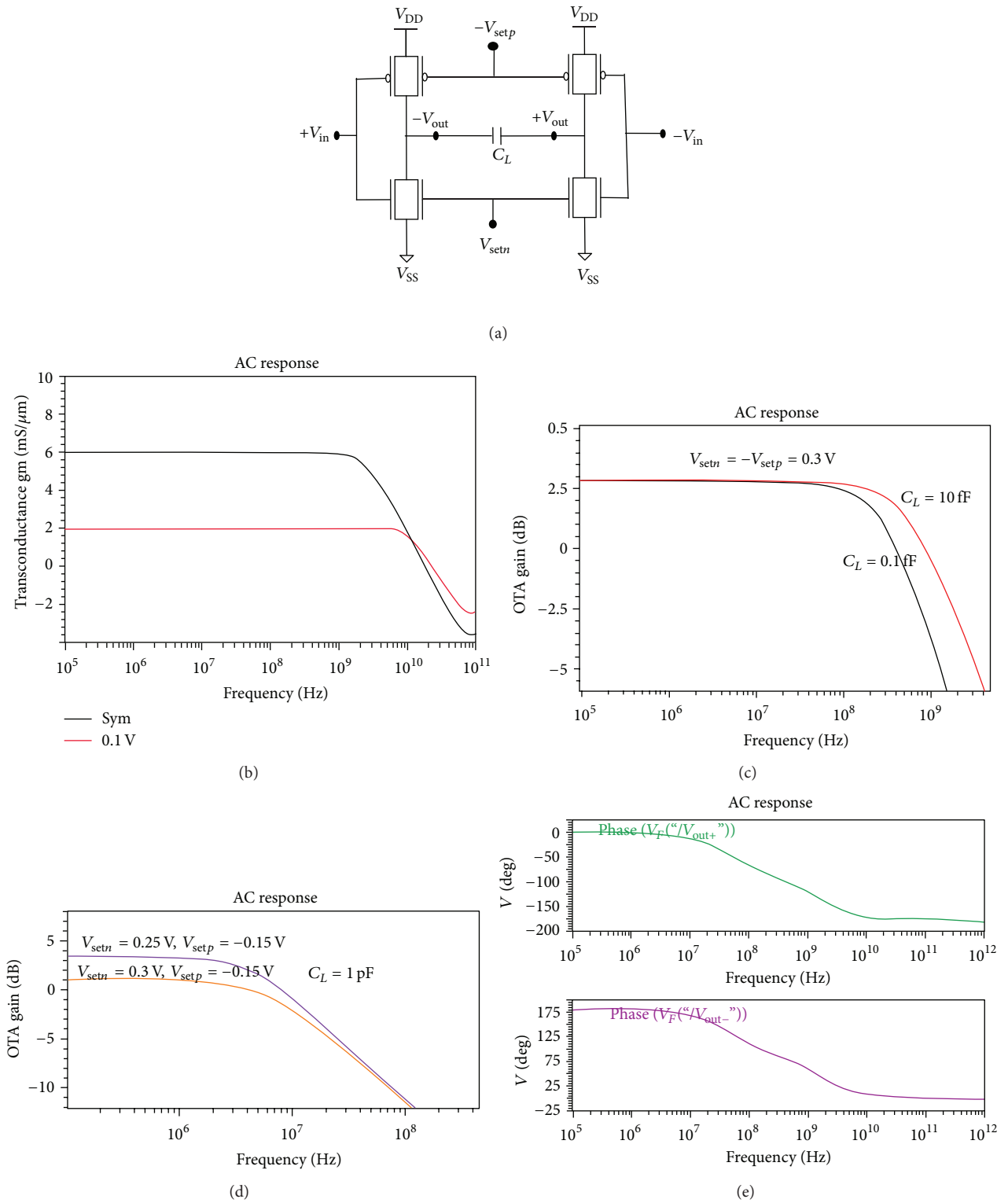

FIGURE 5: (a) A simple operational transconductance Amplifier using FinFET, (b) the transconductance of OTA circuit ($C_L = 0$), (c) the gain of simple operational transconductance amplifier as a function of conjugate bias ($V_{setn} = -V_{setp}$), (d) the gain of simple operationaltransconductance amplifier as a function of $V_{setn} \neq V_{setp}$, and (e) the phase of simple operational transconductance amplifier as a function of $V_{setn} = -V_{setp}$.

In FinFET Schmitt trigger, we use only 4 FinFETs as compared to 6 MOSFETs in traditional CMOS design [13, 14]. Figure 4(a) shows two-stage CMOS circuit where conjugate biasing of the second stage ($V_{setp} = -V_{setn}$) is used to shift the first stage's output to two opposite extremes. Figure 4(b) shows the simulated output of the Schmitt trigger circuit. At the different thresholds, the output makes transitions between sweep-up and sweep-down cases. Figure 3(b) shows the decided width of the hysteresis because of the first stage small gain compared to the second stage hence very large hysteresis width can be achieved. Large conjugate biasing is used to design of small hysteresis and limiting the output swing of the second stage.

In the nanometer technology hysteresis can be scaled by acquiring various topologies in the second stage. In this case the rail voltage nodes (V_{dset} and V_{sset}) are programmed for 0.2 V and back gates are connected to the front gates ($V_{setp} = V_{setn} = V_{out2}$), that is, the SD FinFET configuration of Figure 1(c). The simulated output of Schmitt Trigger Circuit is given in Figure 4(c) for rail voltage $V_{dset} = -V_{sset} = 0.2$ V. The feedback voltage from the output of the second stage changed then the hysteresis is scaled both horizontally and vertically because the gain of the second stage is higher.

6. Operational Transconductance Amplifier (OTA) Circuit

Operational transconductance amplifiers (OTA) produce differential output currents, when differential input voltages are applied. OTA have been popular in last two decades because of ease to design and reduction in circuit complexity compared to operational voltage amplifier. OTA can act as very efficient integrators because they often drive a capacitive load in a compact OTA-C block. Figure 5(a) show a simple OTA structure modified from traditional MOSFET, which required 6 transistors [15] as compared to 4 FinFETs used in Figure 5(a). The ease of use of the individual back gates allows the removal of the 2 extra transistors for transconductance tuning across the 2 branches of the OTA, which preserves both area and power.

There are two tuning methods available to this simple operational trans-conductance amplifier circuit such as asymmetric bias ($V_{setn} \neq V_{setp}$) to shift the frequency response or a conjugate bias ($V_{setn} = -V_{setp}$) to change the transconductance. Figure 5(b) shows where the frequency dependence of transconductance on the conjugate biasing voltage is plotted against frequency. The most significant figure of merit transconductance of OTA varies linearly with the biasing voltage and bandwidth of the OTA is constant varying transconductance, which is one of the main characteristics of OTAs. The transconductance is constant up to 90 GHz range controlled by small parasitic capacitances.

We can shift the frequency response, when an asymmetric bias is used to tune the OTA. Figure 5(c) shows gain of the OTA circuit, which serves as a low pass filter with a corner frequency 0.40 GHz at $V_{setn} = -V_{setp} = 0.30$ V and load capacitance $C_L = 10$ fF or 0.1 fF. The filter pass band extends up to 9 MHz because of applied large load ($C_L = 1$ pF) as shown in Figure 5(d). Figure 5(e) shows the phase of simple operational transconductance amplifier as a function of $V_{setn} = -V_{setp}$. Using the FinFET, OTA has a better common mode rejection, which will be explored in a future work.

7. Conclusion

The examples of low power tunable analog circuit using FinFET have been analysed. Using mixed mode Cadence Virtuoso simulations, we have shown the designing and testing of analog circuit with tunable performance metrics using back gate of an ID FinFET which is better than SD FinFET. We have used the examples of simple CMOS amplifier, a Schmitt trigger circuit, and an OTA circuit. In all cases, we can vary the back gate bias conditions to provide the figure of merit, the gain, the phase, the transconductance, and the hysteresis, respectively. A wide tuning range of performance in the figures can be identified using identical or conjugate biasing of n-type and p-type FinFETs which are preferable for most cases, and therefore, it can establish voltage tuning with good accuracy. In future work, we compare the performance in real terms with other circuits, and accuracy of the noise analysis and power consumption must be improved. We may design and analyze FinFET based ring oscillator and current mirror circuits in future work. Using the FinFET, OTA has a better common mode rejection, which will be explored in a future work.

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