

# Research Article Leakage Power Analysis of Domino XOR Gate

# A. K. Pandey, R. A. Mishra, and R. K. Nagaria

Department of Electronics and Communication, M.N.N.I.T, Allahabad 211004, India

Correspondence should be addressed to A. K. Pandey; amitkumarpandey1@gmail.com

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Two new XOR gates are proposed. First proposed circuits adopt hybrid transistor topology in the pull-down network with all transistors being low threshold voltages. A second proposed circuit adopts hybrid topology with dual threshold voltage transistors. Simulation parameters are measured at 25°C and 110°C. First proposed circuit reduces leakage power consumption up to 50% at 25°C and 58% at 110°C as compared to standard N-type domino XOR gate. It also reduces active mode power consumption up to 73% at 25°C and 90% at 110°C as compared to standard N-type domino XOR gate. It also reduces active mode power consumption up to 73% at 25°C and 90% at 110°C as compared to standard N-type domino XOR gate. It also reduces active mode power consumption by 39% as compared to standard N-type domino XOR gate.

# 1. Introduction

CMOS XOR gates are the fundamental units, it is used in many VLSI applications such as adders and microprocessors. CMOS XOR has complex pull up and pull down network, it is being characterized as high power consumption, large layout area, and low speed [1–4]. Domino XOR has small layout area, low power consumption, and improved speed as compared to CMOS XOR [5–7]. Due to its superior performance and low power consumption, domino XOR is being used in many VLSI applications. Standard domino XOR gate requires two phase input signals, one is original and the other is inverted signal. It needs additional inverters to meet the design requirements. The additional inverters not only increase the power consumption but also affect the performance of the circuit.

As technology is scaled down, supply voltages are also scaled down to keep the dynamic power at acceptable levels, and at the same time threshold voltage  $(V_t)$  is also scaled down to meet the performance requirements. However, subtreshold leakage and gate oxide leakage currents are increased exponentially with the scaling of threshold voltage and gate oxide thickness  $(T_{ox})$ , hence power consumption increases and noise immunity decreases. To solve the problem of high subthreshold leakage current, many circuit level techniques have been implemented including body bias control [8], input vector control [9], transistor stack effect [10], dual  $V_t$  CMOS [11], and sleep switch [12–14]. Dual  $V_t$  domino technique [11] is realized by using low  $V_t$  transistor in the evaluation path and high  $V_t$  transistor in the precharge path of the circuits. According to Kao, high clock and high inputs (CHIH) are preferable to reduce subthreshold leakage current in dual  $V_t$  footless domino gate.

Combination of subthreshold and gate oxide leakage current in footless domino circuit was carried out by Liu and Kursun [15–17]. Considering the major effects of gate oxide leakage current on the total leakage current, it shows that at low temperature, clock high and inputs low (CHIL) state is preferable. At high temperature CHIH state is preferable in domino footless circuit. Sleep switch methods are efficient for reducing both subthreshold and gate oxide leakage current. High  $V_t$  nMOS switch is added to the dynamic node in domino footless circuit. High clock and active sleep switch suppresses subthreshold leakage current but produces high output of domino gate that places highest gate oxide leakage current to the fan out domino gate [12]. By adding two sleep switches, one at dynamic node and other at output node, both subthtreshold and gate oxide leakage current are reduced [13, 14].

Combination of clock and inputs signal states is provided for footed domino circuits to optimize the total leakage current [18]. According to [18], subthreshold and gate oxide leakage currents are not only function of input states but also clock signal states. If subthreshold is the dominant source, then CHIH state is the best choice. Similarly, if gate oxide leakage current is the dominant source, then clock low and input low (CLIL) state is preferable. Leakage power consumption of the domino circuit is characterized as

$$P_{\text{Leakage}} = I_{\text{Leakage}} \times V_{\text{DD}},\tag{1}$$

where  $I_{\text{Leakage}}$  is the combination of subthreshold and gate oxide leakage current.

In this paper, two new domino XOR circuits are proposed. First proposed circuit has N and P type mixed transistors in the pull down network and all transistors are low threshold voltage. Second proposed circuit utilizes dual threshold voltage. Rest of the paper is organized as follows. Section 2 discusses the leakage current characteristic of single transistor. Section 3 describes the operation of the standard domino XOR circuits. In Section 4, proposed circuits are discussed in details. In Section 5, simulation results are analyzed and the conclusion is presented in Section 6.

## 2. Leakage Current Analysis of Single Transistor

The subthreshold and gate oxide leakage currents are shown in Figure 1. Subthreshold leakage current is maximum when transistor is in cut off mode and voltage difference between drain-to-source is maximum and it has reverse edge gate oxide leakage current as shown in Figure 1(a). Gate oxide leakage current has four components: gate-to-channel ( $I_{gc}$ ), gate-to-drain ( $I_{gd}$ ), gate-to-source ( $I_{gs}$ ), and gate-to-body ( $I_{gb}$ ). Igb is several orders smaller as compared to all three components and it is neglected, Igc is shared between drain and source as shown in Figure 1(b). Gate oxide leakage current is maximum, when transistor is in active mode and the voltage difference between the gate-to-source and gateto-drain are maximum. To avoid both subthreshold and gate oxide leakage currents, all terminals of a transistor must have same potential as shown in Figure 1(c).

The width and length of both an nMOS and a pMOS transistors are set to be 1  $\mu$ m and .045 um, respectively. Gate oxide leakage of an nMOS transistor is dominant over pMOS transistor because tunneling probability of electron is greater than tunneling probability of hole as shown in Figure 2. The gate oxide leakage current produced by an nMOS transistor is 9.9x to 40.1x times higher than the gate oxide leakage current of a pMOS transistor depending on the voltage difference across the gate oxide [13, 14].

Variations of subthreshold and gate oxide leakage current of an nMOS with supply voltage at two different temperatures as shown in Figure 3. At 110°C, the subthreshold leakage current is 6.7 times higher than the gate oxide leakage current at 0.8 V supply voltage [13]. Similarly, at the room temperature, the gate oxide leakage current is 2.5 times higher than subthreshold leakage current at 0.8 V.

Comparison of normalized subthreshold leakage current and gate oxide leakage current produced by low- $V_t$  transistor and high- $V_t$  transistor in dual  $V_t$  CMOS technology as shown in Table 1 [14]. Here we have taken transistor width

TABLE 1: Normalized subthreshold and gate oxide leakage currents of the low- $V_t$  and high- $V_t$  transistors at two different temperatures [14].

	nN	AOS	pMOS		
	Low- $V_t$	$High-V_t$	$\text{Low-}V_t$	$High-V_t$	
I <sub>sub</sub> (110°C)	22.3	2.6	16.01	1.0	
$I_{\text{gate}}$ (110°C)	3.3	0.05	0.097	0.0003	
$I_{\rm sub}$ (25°C)	3.7	1.9	3.1	1.0	
$I_{\text{gate}} (25^{\circ}\text{C})$	9.4	0.15	0.31	0.001	

as 1  $\mu$ m, transistor length as 45 nm, low-V<sub>t</sub> for nMOS and pMOS are set at 0.22 V and -0.22 V, high-V<sub>t</sub> for a nMOS and pMOS are set 0.466 V and -0.4118 V, and power supply is 0.8 V, respectively. For each temperature, the currents are normalized to the subthreshold leakage current produced by the high- $V_t$  pMOS transistor. The gate oxide leakage current of a low- $V_t$  nMOS transistor is 3.30 times and 9.4 times higher than the subthreshold leakage current of a high- $V_t$  pMOS transistor at the high and low temperatures, respectively. The gate oxide leakage current produced by a low-V<sub>t</sub> nMOS transistor is 34 times and 30 times higher than the gate oxide leakage current produced by a low- $V_t$  pMOS transistor at 110°C and 25°C. The gate oxide leakage current for pMOS device is lower as compared to an nMOS device with the same width and length with different  $T_{ox}$  and the same voltage difference across the gate insulator.

Figure 4 shows that subthreshold leakage current produced by the low- $V_t$  transistors is the highest source of leakage current in sub-45 nm technologies at high temperature (110°C). At room temperature (25°C), gate oxide leakage current produced by the low- $V_t$  nMOS is the dominant source of the leakage current. At room temperature, gate oxide leakage current is the dominant contributor and has little dependence on temperature. Subthreshold leakage current increases exponentially with temperature and it is dominant for high temperature. Relative contribution of gate oxide and subthreshold leakage currents is also dependent on fan-in, structure of the PDN, and inputs of the fan-in of domino circuits.

#### 3. Standard XOR Gate

The standard N-type domino XOR gate (DXN) as shown in Figure 5. Transistor M2 works as keeper. Here pull down network consists of all N-type transistors [5]. The dynamic node gives XNOR gate logic  $V_n = A \odot B$  and output node gives XOR gate logic  $V_{OUT} = A \oplus B$ . The clock signal divides the circuit operation into two operating phases, precharge and evaluation phase. In precharge phase, clock is low, dynamic node is charged to  $V_{DD}$  by pull-up transistor M1, M5 turned OFF so no direct DC current flows from power supply to ground. M5 avoids short circuit current in the circuit. During evaluation phase, clock is high, the pull-up transistor is cut off and footer transistor M5 is ON. Depending upon the inputs in the pull-down network, a conditional path is established between the dynamic node and ground. If A = 0, B = 0 or



FIGURE 1: (a) Maximum subthreshold leakage current state. (b) Maximum gate oxide leakage current state. (c) Condition to avoid both subthreshold and gate oxide leakage current.



FIGURE 2: Comparison of gate oxide leakage current for an nMOS and pMOS [14].

A = 1, B = 1, dynamic node is discharged to low voltage and output node is charged to high voltage. Output remains low for the rest of the input states.

The standard P-type domino XOR gate as shown in Figure 6. Here pull-up network consists of all P-type transistors [5]. Transistor M2 works as keeper. In precharge phase, clock is low, depending upon on the inputs of the pull-up network, a conditional path is established between the power supply and the dynamic node. If A = 0, B = 0 or A = 1, B = 1, dynamic node is charged to high voltage and output node is discharged to low voltage. During evaluation phase, dynamic node is discharged to low voltage.

P-type domino XOR gate has a great advantage as compared to N-type domino XOR. It effectively suppresses both subthreshold and gate oxide leakage current at the expense of speed. N-type domino circuit has higher speed and higher power consumption, and P-type domino circuit has lower speed and lower power consumption. Drawbacks of standard



FIGURE 3: Comparison of subthreshold and gate oxide leakage current of an nMOS at two different temperatures [14].



FIGURE 4: Comparison of subthreshold and gate oxide leakage current of low- $V_t$  and high- $V_t$  transistors at two different temperatures.



FIGURE 5: Standard N-type domino XOR gate (DXN) [5].



FIGURE 6: Standard P-type domino XOR gate (DXP) [5].

N-type or P-type is that the input signals must be two phases, original and its inverted signals. Extra inverters must be added in the circuit to get inverted signal of original signal.

Adding inverter increases the extra power consumption and propagation delay which extremely affects the performance

of the domino XOR gate.



FIGURE 7: Hybrid domino XOR gate with low threshold voltage transistors (DXHL).

## 4. Proposed XOR Structures

Focusing on the advantage of an N-type transistor having high speed and a P-type transistor having low power consumption. The proposed circuits utilized the advantage of both N-type and P-type transistors.

4.1. Proposed Circuit 1 (DXHL). This technique adopts N and P type hybrid transistors in the pull-down network and all the transistors are low threshold voltage (DXHL) as shown in Figure 7. In this circuit, parallel combination of P-type M6, M7 and N-type M8, M9 transistors are connected in series. Here additional inverters are not required to provide inverted input signals. During precharge phase, dynamic node  $V_n$  is charged to  $V_{\rm DD}$  and output is discharged to low voltage. During evaluation phase, if inputs A = 0, B = 1 or A = 1, B =0, dynamic node is discharged to low voltage and output node is charged to high voltage. For other combination of inputs, dynamic node is high and output node is low. Here DXHL requires single phase input signal and has small circuit area as compared to standard N-type and P-type domino XOR gate. From the circuit, it is clear that removing extra inverter reduces the power consumption. Drawback of this technique is that it has lower speed as compared to standard N-type or P-type domino XOR gate. Dynamic node gives XNOR logic

$$V_{n} = \overline{\left(\overline{A} + \overline{B}\right) \cdot (A + B)},$$

$$V_{n} = A \cdot B + \overline{A} \cdot \overline{B}.$$
(2)

Output node gives XOR logic

$$V_{\rm OUT} = A \cdot \overline{B} + \overline{A} \cdot B. \tag{3}$$



FIGURE 8: Hybrid domino XOR gate with dual threshold voltage transistors (DXHD).

4.2. Proposed Circuit 2 (DXHD). Hybrid XOR gate with dual threshold voltage domino gate (DXHD) as shown in Figure 8. Here all transistors that can be activated during precharge phase have high threshold voltage transistors and others have low threshold voltage transistors that determine the speed of this circuit. Subthreshold and gate oxide leakage current of all the high  $V_t$  transistors are lesser than low  $V_t$  transistor. In precharge mode, turning ON the high- $V_t$  pull-up transistor. When clock is high, operation of this circuit is similar to previous technique.

#### 5. Simulation Results

In this section, proposed circuits (DXHL and DXHD) and existing circuits (DXN and DXP) are simulated, respectively, based on 45 nm models [19] using HSPICE tool. 1 GHz clock frequency is applied to all the circuits with load capacitance 1 fF. Low threshold voltage for an nMOS and a pMOS transistor are set as 0.22 V and -0.22 V, respectively. High threshold voltage for an nMOS and a pMOS transistor are set as 0.466 V, -0.4118 V, and 0.8 V, respectively. To have reasonable comparison, all the circuits have similar size. Leakage power consumption is measured at 25°C and at 110°C, respectively. Active mode power consumption and A.C noise margin are measured at 110°C.

At room temperature, gate oxide leakage current is dominant over subthreshold leakage current. The leakage power consumption of proposed circuits and existing circuits in four clock input vectors with clock states at 25°C are listed in Table 2. It is shown that proposed circuits have lesser leakage power consumption as compared to the existing circuits. The reason is that DXHL adopts hybrid P and N transistors in the pull-down network, and DXHD adopts hybrid P and N transistors with dual threshold voltage. These techniques do not use extra inverters, as a result leakage power consumption is reduced. The optimal leakage power consumption states of DXN, DXP, DXHL, and DXHD are  $\{clock = 0, input = (0, 1)\}, \{clock = 0, input = (1, 0)\}, \{clock = 0, input = (1, 1)\}$  and  $\{clock = 0, input = (1, 1)\}$ , respectively. It is clear from the Table, DXHL reduces leakage power consumption by 49.7% and 45.1% as compared to DXN and DXP, respectively. Similarly, DXHD reduces leakage power consumption by 73.6%, 71.2%, and 47.5% as compared to DXN, DXP, and DXHL, respectively. Therefore, at low temperature, DXHD has minimum leakage power consumption compared to other techniques.

At high temperature, subthreshold leakage current is dominant over gate oxide leakage current. The leakage power consumption of proposed circuits and existing circuits in four clock input vectors with clock states at 110°C are listed in Table 3. It is shown that DXHL and DXHD have lesser leakage power consumption as compared to the existing circuits. The optimal leakage current states of DXN,DXP, DXHL, and DXHD are  $\{clock = 0, input = (1, 1)\}, \{clock = 1, ..., clock = 1,$ input = (1,0)}, {clock = 0, input = (0,0)}, and {clock = 1, input = (0, 0)}, respectively. DXHL reduces leakage power consumption by 58.4% and 53.7% as compared to DXN and DXP, respectively. Similarly, DXHD reduces leakage power consumption by 90.7%, 89.7%, and 77.8% as compared to DXN, DXP, and DXHL, respectively. Therefore, at high temperature, DXHD has minimum leakage power consumption compared to other techniques.

A.C noise margin is defined as the level of noise signal for which output is reduced by 10% of its maximum value. Noise signal is applied to all inputs of the circuits and to be set as 1 GHz square wave with 60% duty cycle at 110°C. A.C noise margin is calculated for the proposed circuits and existing circuits are listed in Table 4. DXHD increased A.C noise margin by 18.18%, 12.72%, and 5.45% as compared to DXN, DXP, and DXHL circuits.

Active mode power consumption is measured when a conditional path is established between the dynamic node and ground. Figure 9 shows comparison of normalized active mode power consumption and normalized leakage power consumption of optimal state of four XOR circuits at 110°C. It is seen from the figure that DXHD reduces active mode power consumption by 39.12%, 35.38%, and 29.04% as compared to DXN, DXP, and DXHL circuits. DXHD technique has lowest active power as compared to other techniques. DXHD technique better performance as compared to other techniques at the expense of the speed.

# 6. Conclusion

At room temperature, gate oxide leakage current is dominant over subthreshold leakage current. Similarly, at high temperature, subthreshold leakage current is dominant over gate oxide leakage current. In a 45 nm CMOS technology, both subthreshold and gate oxide leakage current are needed to be suppressed. In this paper, two new XOR circuits are proposed to reduce leakage power consumption and active mode power consumption as compared to standard XOR circuits. First proposed circuit utilizes hybrid N- and P-type transistors in the pull-down network with all transistors are low threshold

Inputs	DXN		DXP		DX	DXHL		DXHD	
	CLK = 0	CLK = 1							
A = 0, B = 0	2.06	3.50	1.93	1.91	1.14	1.88	0.67	0.88	
A = 0, B = 1	2.01	3.08	1.92	2.57	1.42	4.26	0.95	1.37	
A = 1, B = 0	2.46	3.08	1.84	2.05	1.42	4.26	0.95	1.37	
A = 1, B = 1	2.43	3.13	2.57	2.55	1.01	2.37	0.53	1.92	

TABLE 2: Leakage power consumption ( $\mu$ W) of four XOR circuits in different Input States and Clock States at 25°C.

TABLE 3: Leakage power consumption ( $\mu$ W) of four XOR circuits in different Input States and Clock States at 110°C.

Inputs	DXN		DXP		DXHL		DXHD	
	CLK = 0	CLK = 1						
A = 0, B = 0	14.87	21.22	16.81	14.72	6.05	13.04	5.55	1.34
A = 0, B = 1	19.07	17.78	16.94	14.41	8.30	15.66	7.85	1.88
A = 1, B = 0	16.11	17.58	16.46	13.08	8.30	15.66	7.85	1.68
A = 1, B = 1	14.55	21.37	18.02	15.93	9.04	10.63	8.57	10.22

TABLE 4: A.C noise margin of four XOR circuits at 110°C.



FIGURE 9: Comparision of normalized active mode power consumption and optimal leakage power consumption at 110°C.

voltage. Second proposed circuit utilizes hybrid N and P type transistors in the pull-down network with dual threshold voltage transistors. Circuits are simulated in HSPICE tool based on 45 nm technology.

At room temperature, first proposed circuit reduces leakage power consumption by 49.7% and 45.1% as compared to N-type domino XOR and P-type domino XOR respectively. Second proposed circuit reduces leakage power consumption by 73.6%, 71.2%, and 47.5% as compared to standard N-type domino XOR, P-type XOR, and proposed circuit reduces leakage power consumption by 58.4% and 53.7% as compared to N-type domino XOR and P-type domino XOR respectively. Second proposed circuit reduces leakage power consumption by 58.4% and 53.7% as compared to N-type domino XOR and P-type domino XOR respectively. Second proposed circuit reduces leakage power consumption by 90.7%, 89.7%, and 77.8% as compared to standard N-type domino XOR, P-type XOR, and

proposed circuit1, respectively. Proposed circuit 2 reduces active mode power consumption by 39.12%, 35.38%, and 29.04% as compared to standard N-type domino XOR, P-type domino XOR, and proposed circuit 1. Proposed circuit 2 increases A.C noise margin by 18.18%, 12.72% and 5.45% as compared to standard N-type domino XOR, P-type domino XOR, and proposed circuit 1.

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