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*Research Article*

# A 0.6-V to 1-V Audio ΔΣ Modulator in 65 nm CMOS with 90.2 dB SNDR at 0.6-V

**Liyuan Liu,[1,2] Dongmei Li,[1] and Zhihua Wang[1]**

[1] *Tsinghua University, Beijing 100084, China*
[2] *Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China*

Correspondence should be addressed to Liyuan Liu; liuly@semi.ac.cn

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This paper presents a discrete time, single loop, third order ΔΣ modulator. The input feed forward technique combined with 5-bit quantizer is adopted to suppress swings of integrators. Harmonic distortions as well as the noise mixture due to the nonlinear amplifier gain are prevented. The design of amplifiers is hence relaxed. To reduce the area and power cost of the 5-bit quantizer, the successive approximation quantizer with only a single comparator instead of traditional flash quantizer is employed. Fabricated in 65 nm CMOS, the modulator achieves 95 dB peak SNDR at 1-V supply with 24 kHz. Thanks to low swing circuit techniques and low threshold voltages of devices, the peak SNDR maintains 90.2 dB under 0.6-V low supply. The total power dissipation is 371 $\mu$W at 1-V and drops to only 133 $\mu$W at 0.6-V.

## 1. Introduction

CMOS technology has progressed into sub-100 nm era. Advanced technology offers speed power and area benefits for digital circuits design. However the sub 1-V low supply voltage, reduction of intrinsic gain, deteriorated device matching, and dramatic increase of flicker noise have brought difficulties to precision analog designs [1]. The ΔΣ modulator is a popular building block which is strongly demanded in high accurate analog signal conditioning such as digital audio. Several designs have been reported with sub-100 nm technology. Although large dynamic range has been achieved, the SNDR performance is lower than 80 dB due to large flicker noise and high harmonic distortion [2–5].

In [4, 5], continuous time ΔΣ modulator (CT-DSM) is adopted for low power implementation. Although the bandwidth requirement of the amplifier is relaxed in CT-DSM than that in discrete-time ΔΣ modulator (DT-DSM), CT-DSMs suffer from problems such as sensitivity to clock jitter, performance degradation due to excessive loop delay, and needing tuning circuits to deal with RC time constant variations.

In this work, we propose a high performance DT-DSM. The feedforward path together with multibit quantizer leads to very small swings at integrators' outputs. Both gain and bandwidth requirements of amplifiers are relaxed. To overcome large area and power dissipation problems associated with traditional flash multibit quantizer and conventional analog summing, in this work we propose a self-timing successive approximation (SAR) quantizer with embedded analog summing circuitry. The prototype modulator is fabricated in 65 nm CMOS. Measurement shows that peak signal to noise and distortion ratio (SNDR) of 95 dB is achieved across 24 kHz under 1-V with 371 $\mu$W. Under 0.6-V supply, the peak SNDR is still 90.2 dB. The power consumption reduces to only 133 $\mu$W.

In Section 2, the architecture of the modulator is described. Section 3 discusses detail circuits' implementations. Section 4 shows the measurement results and Section 5 concludes the paper.

## 2. Low Voltage Modulator Architecture

*2.1. Design Considerations of the Modulator.* A major challenge in low voltage design is that circuits must operate in limited voltage headroom conditions. Modulator topology with low swing is thus necessary. Shown in Figure 1 is

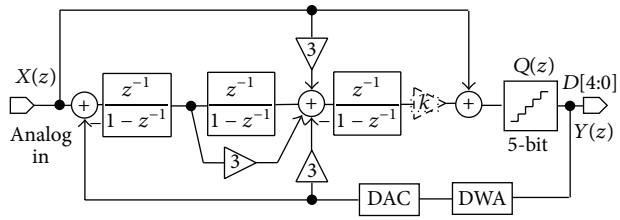



Figure 1: The 3rd order CIFB modulator with 5-bit quantizer.

the modulator architecture. It is a 3rd order CIFB modulator reported in [6, 7]. By introducing a directly input feedforward path, signal components are removed from outputs of integrators. Swings of integrators are independent of input signal's amplitude and are only determined by quantization error. By employing a 5-bit quantizer, the quantization step is fine and signal swings are even smaller.

The modulator coefficients are chosen as shown in Figure 1. Ideally the noise transfer function (NTF) is $(1-z^{-1})^3$. Such kind of NTF is aggressive and modulator stability must be considered. Although a 5-bit quantizer can guarantee that the modulator is stable with an overload level of 0.9, the gain variation of the last integrator may do harmful to the modulator stability. Such variation is caused by nonideality of the analog summation which will be described later.

Suppose a gain factor of $k$ is introduced as depicted in Figure 1. The transfer function of the modulator can be derived as (1) with the quantizer replaced by its linear model,

$$Y(z) = X(z) + \underbrace{\frac{(z-1)^3}{(z-1)^3 + 3k(z-1)^2 + 3k(z-1) + k}}_{\text{NTF}} Q(z). \tag{1}$$

Poles of the NTF can be found in

$$\begin{aligned} p_1 &= -\sqrt[3]{k(k-1)^2} - \sqrt[3]{k^2(k-1)} - (k-1), \\ p_2 &= \frac{\sqrt[3]{k(k-1)^2}}{2} + \frac{\sqrt[3]{k^2(k-1)}}{2} + (1-k) \\ &\quad + \frac{\sqrt{3}j}{2}\left(\sqrt[3]{k^2(k-1)} - \sqrt[3]{k(k-1)^2}\right), \\ p_3 &= \frac{\sqrt[3]{k(k-1)^2}}{2} + \frac{\sqrt[3]{k^2(k-1)}}{2} - (1-k) \\ &\quad + \frac{\sqrt{3}j}{2}\left(\sqrt[3]{k^2(k-1)} - \sqrt[3]{k(k-1)^2}\right). \end{aligned} \tag{2}$$

Figure 2 shows the location of poles with $k$ varying from 0.7 to 1.2. If $k$ is slightly larger than its critical value 1.14, one pole of the NTF will move out of the unit circle which means that the modulator is unstable regardless of the input signal amplitude. To prevent such a problem, in circuits' implementations the gain factor of last integrator is shrunk deliberately to compensate $k$.

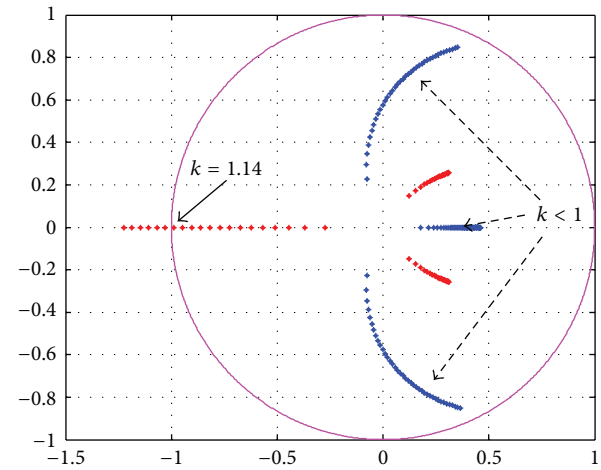



Figure 2: Poles location of the NTFs considering gain factor of $k$.

The gain factor of the directly input feedforward path must be strictly set to unity so that signal components inside the loop filter are forced to be zero. Otherwise, there is signal leakage in the loop filter and the swings of integrators increase. Furthermore, because of nonlinear gain of OTAs, harmonic distortions will be observed in the output spectrum. This problem will be discussed in the design of the quantizer.

*2.2. Multibit Quantizer.* Employing multibit quantizer is popular in high performance modulator design. One benefit is that adoption of multibit can greatly enlarge the overload level (OL). Another advantage is the fine step in quantization which leads to low quantization noise power. This feature is helpful for alleviating the quantization noise mixture effect due to nonlinear OTA gain.

Although with advantages mentioned above, there are also drawbacks in traditional multibit quantizer design. Usually flash quantizer is preferred because of its low latency which is important for the stability of the modulator. Such implementation suffers from problems such as large area and power consumption cost, because there is an exponential dependence of the hardware and power budget on the bits of the quantizer. Several methods have been proposed to overcome these drawbacks. The first method is employing interpolated multilevel quantizer reported in [8]. The key idea is that comparison procedure is separated into coarse and fine steps. However such a method only achieves 50% reduction of the number of comparators. In [8] fifteen comparators are used to implement a 5-bit quantizer which traditionally requires 31 comparators. The second solution is called tracking ADC in [3] which only needs 3 comparators to realize a 4-bit quantizer. In [9] a technique is proposed to reduce the number of comparators to only one. Although reducing the amount of comparators to the minimum, the tracking quantizer suffers from problems such as needing properly defined initial operation point and sensitivity to high-frequency signal leakage. The third way is replacing flash quantizer with successive approximation (SAR) type

[10]. This quantizer also has only a single comparator, but it is free from the problem encountering in tracking quantizer. The problem with SAR quantizer is that serial operation needs fast clock. In this work, a SAR based 5-bit quantizer is adopted to reduce the area and power cost. To mitigate the requirement of fast clock generation, asynchronous control logic is used.

Ahead of the quantizer, an analog summer is needed. Classic capacitive charge sharing based summation is popular, but signal is attenuated by a factor equal to the number of capacitors. For a single bit modulator such attenuation is not important because the quantizer only needs to determine the sign of its input. For a multibit quantizer, this attenuation must be compensated by amplification or deliberated reference voltages scaling. Otherwise the transfer function of the modulator will be changed. In this work by introducing additional switches and clock phase, analog summation can be embedded before normal operation of the SAR quantizer without significant signal attenuation.

## 3. Circuits Design

Figure 3 illustrates the switched capacitor scheme of the ΔΣ modulator. Compared to Figure 1, the gain factor from output of the 1st integrator to the last integrator output is scaled down to 31/12, the factor from output of the 2nd integrator to the last integrator output is scaled down to 10/12, and gain of the last integrator is now set to 10/12. Such modification of coefficients is important to ensure the stability of the modulator as discussed in Section 2.1. The overall circuits contain three switched capacitor integrators and a 5-bit SAR quantizer. The input sampling capacitor is divided into 31 units to implement the 5-bit feedback DAC. Each unit has a value of 527 fF and the total sampling capacitance is 16.3 pF for low thermal noise. The unit capacitor for the 2nd and 3rd stages is 54 fF because of much less noise contribution. The first and last integrators share the switch network which reduces amount of switches. The directly feedforward input signal and the output of the last integrator are summed and quantized into 5-bit digital codes by SAR quantizer. The digital output is decoded to thermometer codes and feedback through a 5-bit DAC. To alleviate distortion due to mismatch among unit capacitor in the DAC, dynamic element matching (DEM) employing data weighted averaging (DWA) is adopted. Integrators are controlled by double phase nonoverlapping clock. The first stage OTA is chopped to remove the flicker noise out of the signal band. Chopping operation happens in the middle of sampling phase $\Phi_1$ to prevent interference [11]. The control clocks of the input and output chopper circuits are also nonoverlapped. The SAR quantizer gives out binary codes which are firstly converted into thermometer code and are then used as switches control signals in the DAC.

*3.1. OTA.* Figure 4 depicts the current mirror OTA for integrators in this design. Looking like a cascade stages amplifier, the first stage contributes nondominant pole and dominant pole locates at the output. The OTA functions like a single stage amplifier which is stabilized by load compensation. Comparing to a miller amplifier, output stages in such an amplifier do not demand large current for stabilization and hence power is saved.

The drawback of the current OTA is low dc gain. Two cross coupled NMOS transistors $M_{ca,b}$ are placed in parallel with the diode connected NMOS load $M_{2a,b}$ in order to enhance the gain of the amplifier to approximately 40 dB [12]. Benefit from feedforward path and 5-bit quantizer, swings of integrators are small. Simulation indicates that maximum voltages of integrators are within ±0.124 V, ±0.064 V, and ±0.218 V which are 6.2%, 3.2%, and 10.9% of full swing ($2V_{\text{pp}}$), respectively. Although the OTA gain varies nonlinearly as shown in (3), small swings make such variations less significant,

$$A_v = 94\left(-8V_o^4 - 1.3V_o^2 + 1\right). \tag{3}$$

In (3) only even order nonlinear coefficients are considered owing to the symmetric characteristic of fully differential OTA. With (3), behavior simulation shows that modulator can achieve ideal SNDR of 119 dB. Further transistor level simulation shows better than 110 dB SNDR is maintained. The OTAs in the first and the third stages have the same transistor sizes. The bias current is 25 $\mu$A for every branch. The load capacitance of the 1st amplifier is approximately the same as the sampling capacitance which is 16.3 pF, the GBW of is then 9.5 MHz which is three times larger than the sampling frequency in order that insufficient settling does not degrade the modulator performance much. For the 2nd stage, since the capacitive load is quite small, the transistors' size and bias currents of the amplifier are half of those in the 1st and 3rd stages. The input common mode voltage (VCMI) is set by the biasing circuits in Figure 4. The benefit of such biasing method is that it can track the process, supply voltage, quiescent current variation so that $M_{1a,b}$ and tail current transistor $M_t$ are always in the saturation range. In high resolution modulator design, circuit noise must be carefully treated. The first stage contributes the most part of noise and can be expressed as

$$N_T = \frac{4kT\left(1 + 2\beta\gamma/3\right)}{\text{OSR}C_S}. \tag{4}$$

In the above expression, $k$ is the Boltzmann constant ($1.38 \times 10^{-23}$ J/K) and $T$ is the absolute room temperature (300 K). The factor $\gamma$ is the noise excessive factor of OTA and is found as (5) by noise analysis,

$$\gamma = 1 + \frac{g_{m2a} + g_{mca}}{g_{m1a}} + \frac{\left(g_{m3a} + g_{m4a}\right) g_{m2a}^2}{g_{m1a} g_{m3a}^2}. \tag{5}$$

All the transistors in Figure 4 are sized to have identical overdriver voltage of 80 mV and thus $\gamma$ is calculated to be 2.4. Besides thermal noise, flicker noise should also be considered because in audio bandwidth from 20 Hz to 24 kHz the power of such noise is significant. Figure 5 shows the noise figure of the first OTA. Below 10 kHz, flicker noise dominates. Between 10 kHz and 100 kHz, contributions of thermal noise

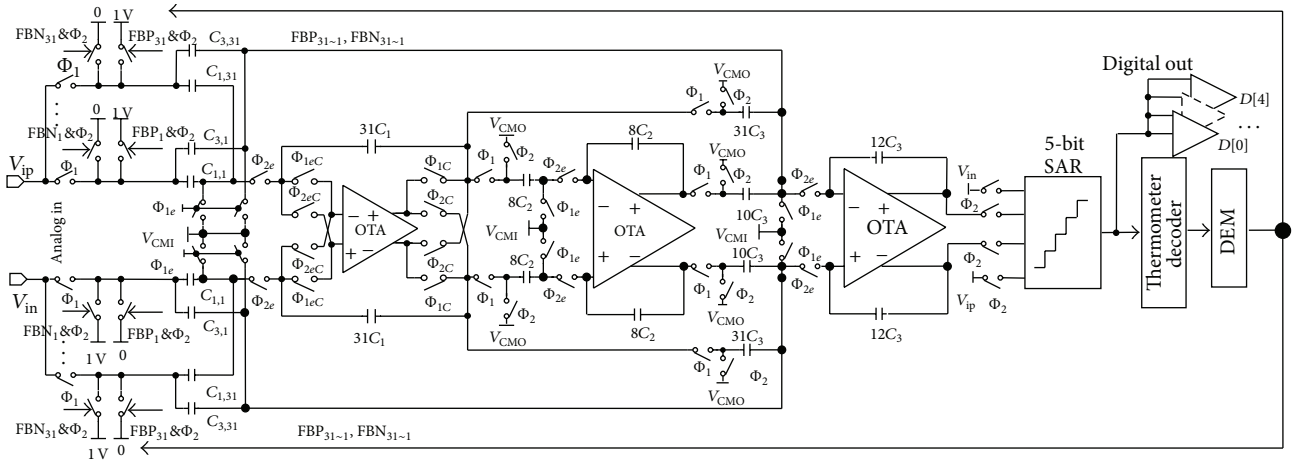
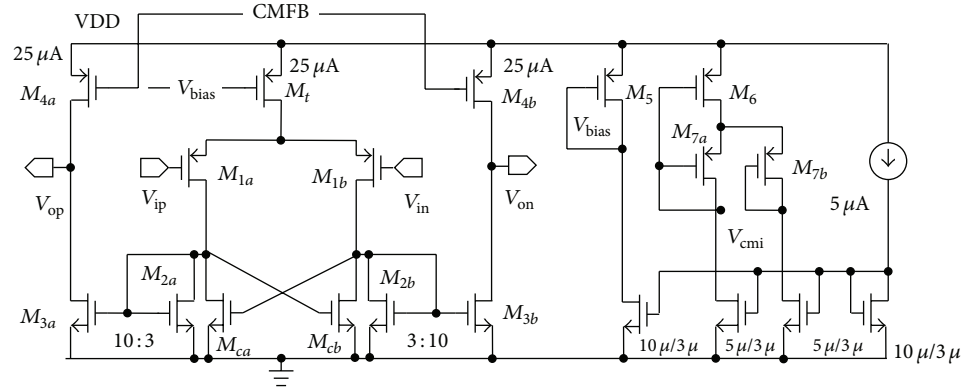



Figure 3: Switched capacitor scheme of the modulator.




| | $M_{1a,1b}$ | $M_{2a,2b}$ | $M_{3a,3b}$ | $M_{4a,4b}$ | $M_t$ | $M_{ca,cb}$ | $M_5$ | $M_6$ | $M_{7a,7b}$ |
|---|---|---|---|---|---|---|---|---|---|
| $OTA_{1,3}$ | 50 μ/1.2 μ | 4.5 μ/0.75 μ | 15 μ/0.75 μ | 45 μ/0.6 μ | 45 μ/0.6 μ | 3 μ/0.75 μ | 9 μ/0.6 μ | 2 μ/1 μ | 10 μ/1.2 μ |
| $OTA_2$ | 25 μ/1.2 μ | 3 μ/0.75 μ | 9 μ/0.75 μ | 22.5 μ/0.6 μ | 22.5 μ/0.6 μ | 1.5 μ/0.75 μ | 9 μ/0.6 μ | 2 μ/1 μ | 10 μ/1.2 μ |

Figure 4: OTAs for integrators.

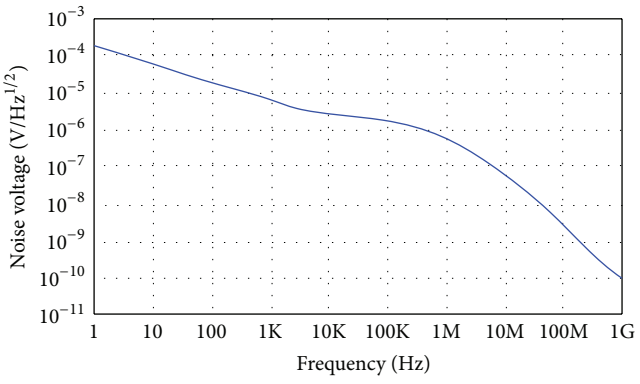



Figure 5: Noise figure of the first OTA.

gradually get larger. Above 100 kHz the noise power density drops because of OTA's frequency characteristic. According to Figure 5 a pessimistic estimation of the OTA corner frequency is around 100 kHz. To remove the flicker noise in low frequency range, the first OTA is chopped at 48 kHz. Although large portion of such noise can be moved to base and odd order harmonics of chopping frequency, there is still residue noise. This effect is modeled by factor $\beta$ in (4). According to analysis in [13], the residue noise and $\beta$ can be expressed as

$$\beta = \left(1 + 0.8525 f_k T_C\right), \tag{6}$$

in which $f_k$ is the corner frequency and $T_C$ is the chopping frequency. It is found to be 2.8 in this design. The total noise $N_T$ can now be evaluated. With 16.3 pF sampling capacitance, theoretical maximum signal-to-noise ratio is better than 100 dB which is enough for high fidelity audio applications.

*3.2. SAR Quantizer.* Figure 6 depicts the 5-bit SAR quantizer. It is composed of a charge sharing DAC, a comparator, and

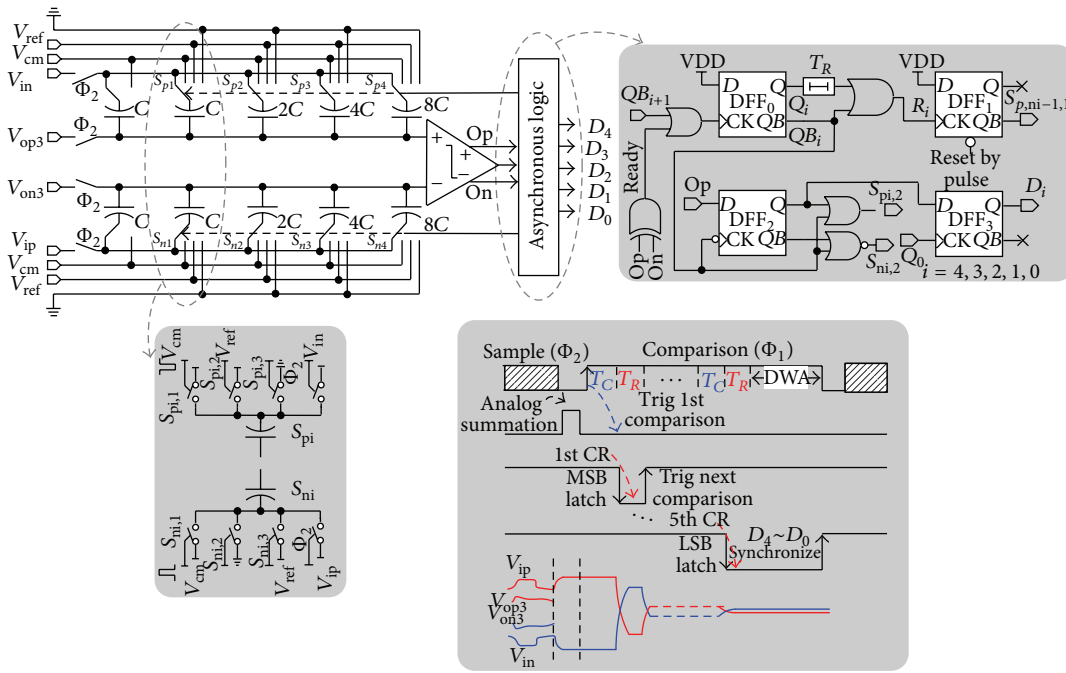



Figure 6: The self-timing 5-bit successive approximation quantizer.

asynchronous control logic. During $\Phi_2$, the top plates of capacitors are tracking the last integrator outputs. At the same time, the bottom plates are connected to input signal $V_{in}$ and $V_{ip}$, respectively. At the end of $\Phi_2$, $V_{op3}$, $V_{on3}$ and $V_{in}$, $V_{ip}$ are sampled. Charges stored on the capacitor array are $(V_{op3}-V_{in})$ $C_{total}$ and $(V_{on3} - V_{ip})$ $C_{total}$, where $C_{total} = 16\,C$. In the nonoverlapped time between the falling edge of $\Phi_2$ and rising edge of $\Phi_1$ a short pulse is generated. The bottom plates are connected to a common mode voltage ($V_{CMO}$) which is in the middle of reference voltage ($V_{ref}$) and ground. Regardless of the parasites, voltages at both terminals of the comparator become $V_{op3} - V_{in} + V_{CMO}$ and $V_{on3} - V_{ip} + V_{CMO}$, respectively. The voltage difference is hence

$$V_{diff} = \left(V_{op3} - V_{on3}\right) + \left(V_{ip} - V_{in}\right). \quad (7)$$

Parasitic capacitances at the input terminals of the comparators are composed of gate-source capacitance of input transistors, parasitic capacitance from top plates of capacitor to the substrate, and parasitic contributed by switches. Denoted as $C_P$ herein, voltage difference after analog summation is

$$V_{diff} = \left(V_{op3} - V_{on3}\right) + \frac{C_{total}}{C_{total} + C_P}\left(V_{ip} - V_{in}\right). \quad (8)$$

Clearly, the input signal is attenuated after the summation which causes signal leakage in the modulator without any compensation. However, $V_{ref}$ is also connected to the bottom plates of capacitors. In the quantization phase, the parasitic also brings the same attenuation to $V_{ref}$. Scaling down of $V_{ref}$ implies that an equivalent gain of $(C_{total} + C_P)/C_{total}$ exists in the quantizer. As a result, direct input signal path still has a unity gain which prevents leakage problem. However an extra gain is introduced to the last integrator's output. According to the analysis in Section 2, the modulator may become unstable. Ideally, the integration capacitor of the last stage should compose 10 unit capacitors in order that the noise shaping function is $(1 - z^{-1})^3$. To mitigating instability, in the circuits design, we choose 12 unit capacitors to provide an attenuation which can compensate the equivalent gain by the quantizer.

After the analog summation, the SAR quantizer generates 5-bit digital codes serially. Asynchronous timing control logic is used. The operation is triggered by the rising edge of $\Phi_1$. The comparator is activated and makes decision of the sign of the voltage difference between its two inputs after its intrinsic delay of $T_c$.

Because both outputs of the comparator are forced to ground before activation, the XOR gate outputs "0." When the comparison is completed, XOR gate outputs "1" and this rising edge will trigger $DFF_{0,i}$, flip. All the flip-flops are reset when $\Phi_1$ is low. Hence the flipping of $DFF_{0,i}$ causes $R_i$ go low immediately which simultaneously deactivate the comparator. Because of the delay, $R_i$ will keep at low for $T_R$. During $T_R$, the charge redistribution happens. $S_{pi,2}$ and $S_{ni,2}$ are generated according to comparator's decision which makes correspondence bottom plates of capacitors connect to $V_{ref}$ or ground. The purpose of $DFF_{1,i}$ is ensuring the bottom plates of correspondence capacitors keep connecting to $V_{CMO}$ when the preceding charge redistribution is ongoing. After all operation cycles, comparison results $D_i$ ($i$ = 4, 3, 2, 1, 0) are synchronized and latched on $DFF_{3,i}$. Using the

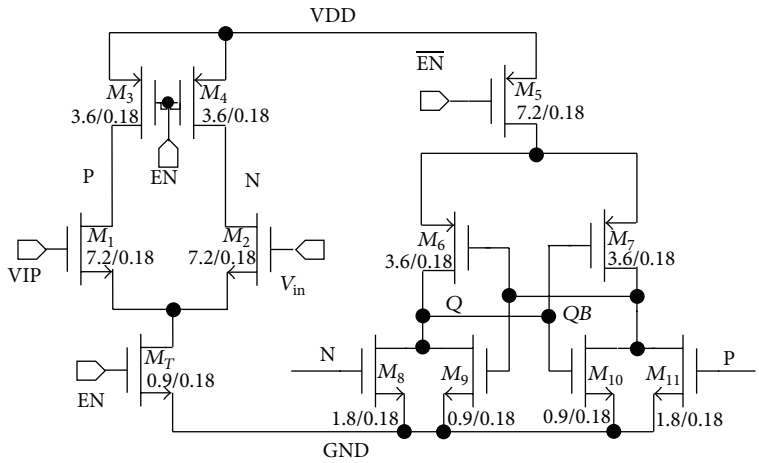



Figure 7: Comparator.

asynchronous logic, $\Phi_2$ is divided into comparison phases and charge redistribution phases automatically without fast clock generation.

The advantages of a SAR quantizer over a flash quantizer are as follows. Firstly, the number of comparator in the quantizer is reduced to only one. Hence area cost is greatly decreased. Although the comparator must work $N$ times faster than that in an $N$-bit flash quantizer, the number of comparator is reduced by $2^N$ and thus the overall power dissipation is saved. Secondly, compared to a flash quantizer, the offset of comparator in a SAR quantizer only brings an offset voltage to the output spectrum without disturbing the noise floor. For a flash quantizer, however, distribution of different offset voltages due to MOS mismatch among comparators alters the quantization step. Some steps become larger and others get smaller. Enlarging of steps causes the quantization error power to increase. With nonlinear gain as mentioned above, noise floor will increase. To prevent this, the offset of each comparator must be well controlled and preamplifier with offset cancellation is required which further increases power consumption. Although in a SAR quantizer, the mismatch among capacitors will also disturb the quantization step, such variation of step is much smaller because of excellent capacitor matching which is exactly the case under advanced technology owing to improved etching precision.

The comparator in the design is shown in Figure 7 [14]. When the comparator is reset, nodes N and P are charged to supply. The enable signal makes $M_T$ conduct. Discharging current of $M_1$ and $M_2$ will pull low the common mode voltage of N and P which makes the next stage latch functional. In a very short time zone, $M_1 \sim M_4$ are all in saturate range and the voltage difference between $V_{ip}$ and $V_{in}$ can be magnified which finally causes the latch flip and generates the decision result.

The noise of such comparator is analyzed in detail in [15] which shows that the noise power is inversely proportional to the parasitic capacitance at nodes N and P. Thanks to the 3-stage integration before the quantizer, the equivalent noise contribution of the comparator at the input of the modulator is greatly suppressed. Hence the sizes of transistors in the comparator can be quite small which saves silicon area.

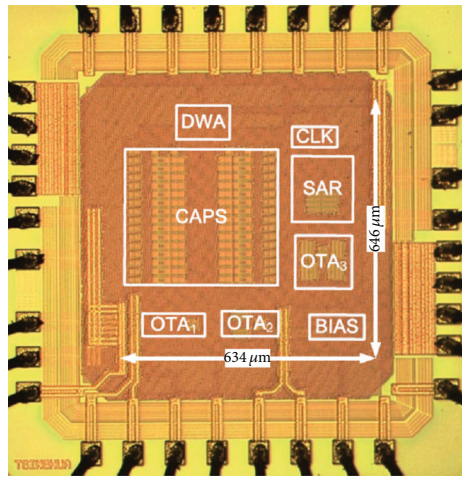



Figure 8: Chip microphotograph.

## 4. Experiment Results

The prototype modulator is fabricated in 65 nm general purpose 1P9M CMOS. Only regular threshold voltage nMOS and pMOS transistors are used. The chip micrograph is shown in Figure 8. The total die area is $1.28 \times 1.33\ \text{mm}^2$ with bonding pads and the active core only occupies $0.41\ \text{mm}^2$.

*4.1. Measurement Setup.* We designed a four-layer printed circuit board (PCB) to evaluate the performance of the chip. An integral ground plane is included. Decoupling capacitors with value of $3.3\,\mu\text{F}$ are connected between supplies and ground for voltage regularity. At all the digital pads, resistors of $50\,\Omega$ are connected so as to reduce signal ringing. Input signal is provided by DS360 which is an ultra low noise and

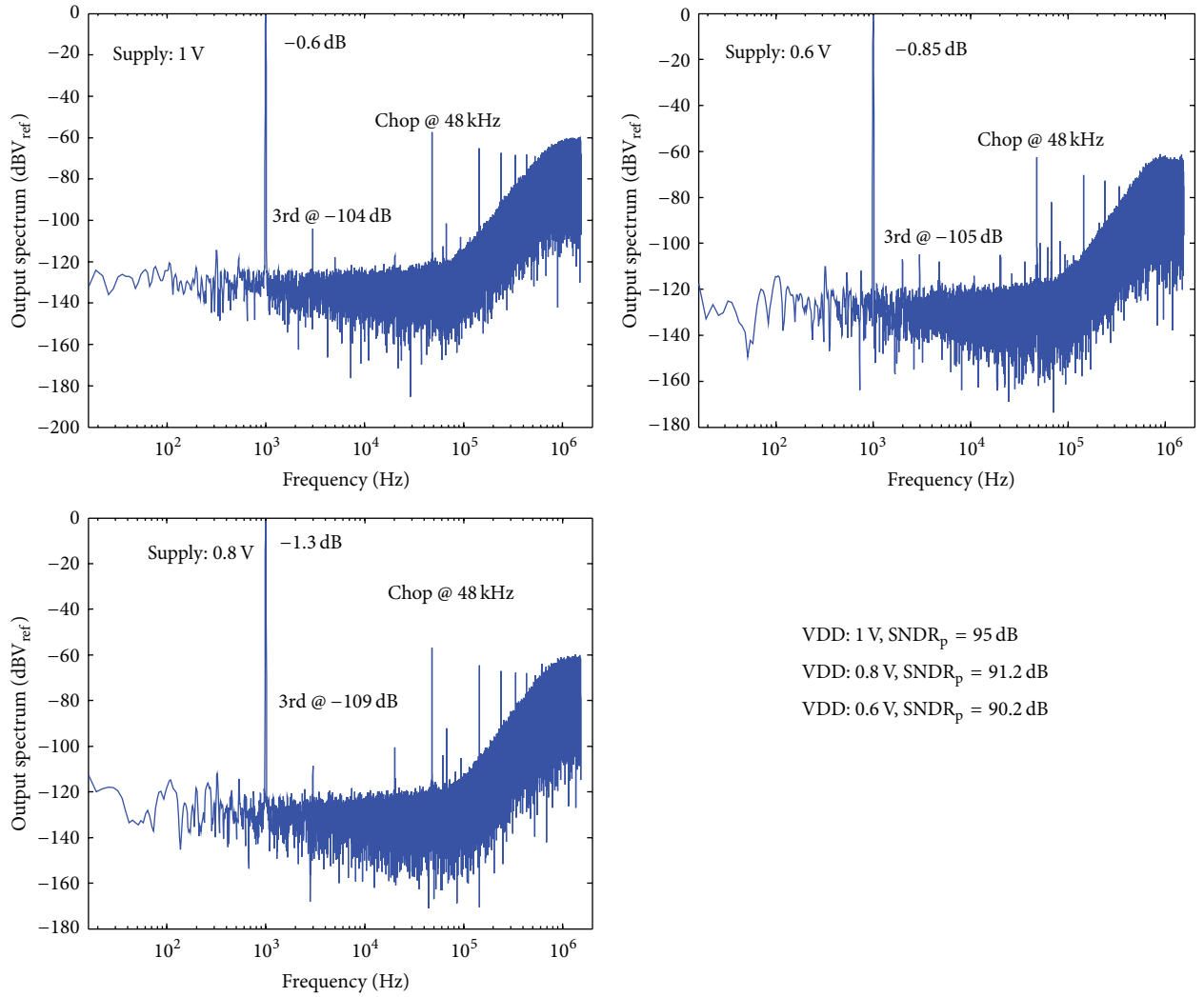



Figure 9: Measured output spectrum.

low distortion signal generator. If the output sine wave has amplitude less than 1.26 V, the noise floor of the equipment is less than 15 nV/$\sqrt{\text{Hz}}$ which leads to integrated noise of only 2.3 $\mu V_{\text{rms}}$ with 24 kHz bandwidth. The total harmonic distortion (THD) is less than −110 dBc. The five-bit digital codes are captured by logic analyzer and MATLAB program is used to do the spectrum analysis.

*4.2. Performance Measurement.* Figure 9 shows the output spectrum. The frequency of the input is chosen as 997 Hz which is a standard in audio measurement. Measurements are done under different supply voltages. The measured peak SNDR is 95 dB, 91.2 dB, and 90.2 dB corresponding to 1 V, 0.8 V, and 0.6 V supply. Our design operates well with only 0.6 V supply. The reasons are firstly input feedforward combined with 5-bit quantizer which makes the signal swing at each integrator output quite small. Although the supply is lowered down, there is still enough voltage headroom for internal amplifiers. Secondly, low device threshold voltage under 65 nm helps amplifiers maintain their proper operational range.

Tones are observed at odd times of Nyquist frequency which shows the effectiveness of chopper. Thermal noise dominates the performance. Figure 10 gives the SNDR performance versus varying input signal amplitude. The measured dynamic range of the modulator is 96.4 dB, 92.4 dB, and 91.9 dB, respectively.

The total power consumption of the modulator is measured with the help of pico-ampere instrument because the voltage drop introduced by the instrument is less than 200 $\mu$V which does not cause any disturbance to the normal operation of the circuits. Under 1 V supply, measured power dissipation of the modulator is 371 $\mu$W and it drops 133 $\mu$W under 0.6 V.

The SAR quantizer inside the loop can be measured separately. Figure 11 shows the differential nonlinearity (DNL) and integral nonlinearity (INL). According to the measurement DNL of the quantizer is less than 0.18 LSB and INL is within 0.23 LSB.

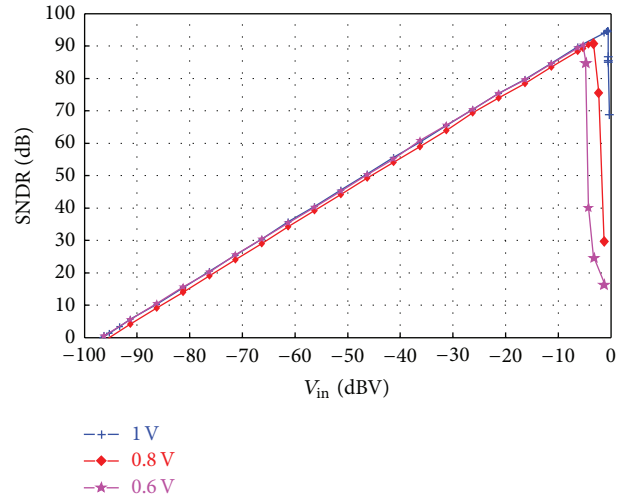



Figure 10: Measured SNDR versus input amplitude.

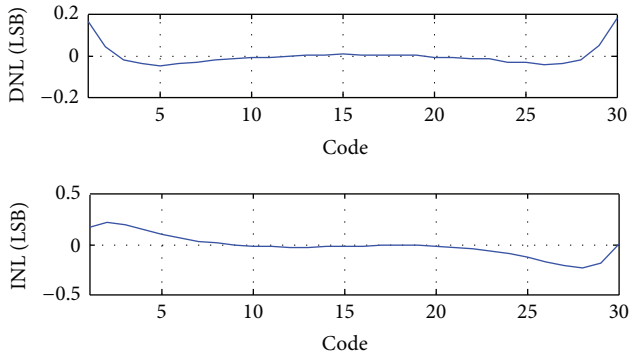



Figure 11: Measured DNL and INL performance of the asynchronous SAR.

Figure-of-merit (FOM) is popular in comparison between designs with different specifications. It is defined by

$$\text{FOM} = \frac{P}{2^{(\text{SNDR}_{\text{peak}}-1.76)/6.02} f_N}, \quad (9)$$

where $P$ denotes the total power dissipation and $f_N$ is the Nyquist frequency which is twice the signal bandwidth. Our design achieves 0.17 pJ/converstion step under 1 V. This value improves to 0.10 pJ/converstion step under 0.6 V. The performance is summarized and compared with published works in Table 1.

## 5. Conclusion

In this paper, design, implementation, and measurement of a high performance audio ΔΣ modulator under 65 nm standard CMOS technology are presented. Low voltage and low power modulator architecture is employed which greatly relaxes the design requirement of the amplifier and comparator. The prototype modulator achieves 95 dB peak SNDR with 24 kHz under 1 V supply while only consumes 371 $\mu$W. With the help of low threshold voltage of devices under 65 nm, the modulator works well under voltage of only 0.6 V. FOM is used in comparisons which show that our design has an overwhelming low power performance.

Table 1: Performance summary and comparison.

| | [3] | [4] | [9] | This work | | |
|---|---|---|---|---|---|---|
| Process (nm) | 65LP | 45LP | 180 | 65GP | | |
| Supply (V) | 1.2 | 1.1 | 0.7 | 1.0 | 0.8 | 0.6 |
| $f_s$ (MHz) | 12 | 12 | 5 | 3.072 | | |
| OSR | 300 | 300 | 100 | 64 | | |
| SNDR (dB) | 74 | 76.5 | 95 | 95 | 91.2 | 90.2 |
| DR (dB) | 95 | 91.7 | 100 | 96.4 | 92.4 | 91.9 |
| Power ($\mu$W) | 2200 | 1200 | 870 | 371 | 224 | 133 |
| FOM (pJ/step) | 11.2 | 4.57 | 0.37 | 0.17 | 0.16 | 0.10 |

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## References

[1] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog circuit design in nanoscale CMOS technologies," *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1687–1714, 2009.

[2] L. Yao, M. S. J. Steyaert, and W. Sansen, "A 1-V 140-$\mu$W 88-dB audio sigma-delta modulator in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 1809–1818, 2004.

[3] L. Dörrer, F. Kuttner, A. Santner et al., "A 2.2 mW, continuous-time sigma-delta ADC for voice coding with 95 dB dynamic range in a 65 nm CMOS process," in *Proceedings of the 32nd European Solid-State Circuits Conference (ESSCIRC '06)*, pp. 195–198, September 2006.

[4] L. Dorrer, F. Kuttner, A. Santner et al., "A continuous time DS ADC for voice coding with 92 dB DR in 45 nm CMOS," in *Proceedings of the Solid-State Circuits Conference IEEE ISSCC Digest of Technical Papers*, pp. 502–503, 2008.

[5] J. Zhang, Y. Lian, L. Yao, and B. Shi, "A 0.6-V 82-dB 28.6-mW continuous-time audio delta-sigma modulator," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2326–2335, 2011.

[6] P. Benabes, A. Gauthier, and D. Billet, "New wideband sigma-delta convertor," *IET Electronics Letters*, vol. 29, no. 17, pp. 1575–1577, 1993.

[7] K. Lee and G. C. Temes, "Improved low-distortion ΔΣ DS ADC topology," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '09)*, pp. 1341–1344, May 2009.

[8] Y. Yang, T. Sculley, and J. Abraham, "A single-die 124 dB stereo audio delta-sigma ADC with 111 dB THD," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1657–1665, 2008.

[9] H. Park, K. Nam, D. K. Su, K. Vleugels, and B. A. Wooley, "A 0.7-V 870-$\mu$W digital-audio CMOS sigma-delta modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1078–1088, 2009.

[10] L. Samid and Y. Manoli, "A multibit continuous time sigma delta modulator with successive-approximation quantizer," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '06)*, pp. 2965–2968, May 2006.

[11] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114-dB 68-mW chopper-stabilized stereo multibit audio ADC in 5.62 $mm^2$," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2061–2068, 2003.

[12] J. Roh, S. Byun, Y. Choi, H. Roh, Y. G. Kim, and J. K. Kwon, "A 0.9-V 60-$\mu$W 1-bit fourth-order delta-sigma modulator with 83-dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 361–370, 2008.

[13] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of Op-Amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[14] D. Schinkel, E. Mensink, E. Klumperink, E. Van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *Proceedings of the 54th IEEE International Solid-State Circuits Conference (ISSCC '07)*, pp. 314–315, February 2007.

[15] M. Van Elzakker, E. Van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9 $\mu$ W at 1 MS/s ," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, 2010.