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Research Article

0.5 V Cardiac Sense Amplifier Realization Using Log-Domain Filtering

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A novel configuration of a cardiac sense amplifier for pacemakers, realized using the concept of Log-Domain filtering, is introduced in this paper. The analog part of the amplifier operates under a single 0.5 V power supply voltage. Compared to the corresponding already published configuration, the proposed scheme offers the benefits of reduced operating voltage and dc power dissipation. The performance of the intermediate stages, as well as of the whole system, has been evaluated through the utilization of the Analog Design Environment of the Cadence software and, also, the design kit provided by the AMS 0.35 μm CMOS process.

1. Introduction

A pacemaker is a closed-loop system where the intracardiac signal events are monitored and detected by a cardiac sense amplifier. The output of the amplifier is directly connected to a microcontroller which provides the appropriate signals to the stimulator in order to establish a therapy scheme for the heart. Taking into account that the biological signals are handled in the body's noisy environment, the cardiac sense amplifier should offer a relatively high signal-to-noise ratio. In addition, this device should be capable of operating in an ultralow voltage environment and, simultaneously, of drawing as small as possible power from the battery in order to achieve maximum life of operation for the pacemaker.

A promising technique for realizing circuits with high dynamic range is the Log-Domain technique. This originated from its companding nature, where the input current is converted into a compressed voltage and then is processed by the nonlinear core. The derived output compressed voltage is converted into a linear current, in order to preserve the linear operation of the whole system. In addition, the internal compressed voltages offer the capability for operation in a low-voltage environment, because of their reduced swings in comparison with those observed in the conventional linear filters. Log-Domain filters could be realized through the utilization of bipolar transistors in the forward active region or MOS transistors in the subthreshold region. The last approach offers potential for reducing the power consumption and this is very important in biomedical applications, since such devices should have a long battery life. Taking also the low-frequency range of biological signals into account, the employment of MOS transistors in the subthreshold region offers the benefit for realizing Log-Domain filters with small capacitor area, due to the large values of the realized equivalent resistors [1–9].

The concept of Log-Domain filtering has been followed in the realization of a cardiac sense amplifier in [10]. Due to the utilization of bipolar transistors in the forward active region, the topology in [10] suffers from the following drawbacks: a power supply voltage equal to 2 V is required and, also, the required power consumption (240 nW) is relatively high for biomedical applications.

In order to overcome the aforementioned drawbacks, a novel topology of a cardiac sense amplifier is presented in this paper. It is constructed from a 4th-order bandpass filter realized using the concept of Log-Domain filtering, a current absolute value circuit, an RMS-DC converter, and a current comparator circuit. The analog part of the amplifier operates in a 0.5 V environment, while the digital part (i.e., the comparator) in a 1 V environment. The power consumption

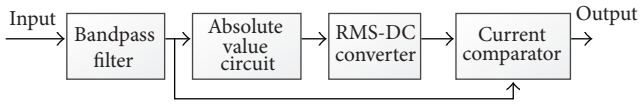

Figure 1: FBD of a cardiac sense amplifier.

of this topology is 2.92 nW. The paper is organized as follows: the 4th-order bandpass filter is presented in Section 2, while the other stages are provided in Section 3. The performance of the proposed topology is evaluated, through simulation results, in Section 4 using the Analog Design Environment of the Cadence software and the design kit provided by the AMS 0.35 μm process.

2. Log-Domain 4th-Order Bandpass Filter

The Functional Block Diagram (FBD) of a cardiac sense amplifier is depicted in Figure 1. According to this, the input signal is fed to a bandpass filter which is used for selecting the QRS complex or R-wave and minimizing the effect of the overlapping myocardial interference signals and low-frequency breathing artifacts. Immunization of the measurements from the position of electrodes is achieved through the utilization of an absolute value circuit, where its output is fed to an RMS-DC converter in order to extract information about the energy of the signal. The resulted output is then compared with the output of the bandpass filter in order to detect the presence of the specific cardiac activity.

In order to describe the operation of the proposed Log-Domain filter topology, the following set of operators will be used:

$$\widehat{v} = \mathrm{LOG}\,(i) \equiv V_{\mathrm{DC}} + nV_T \cdot \ln\left(\frac{i + I_o}{I_o}\right), \tag{1}$$

$$i = \mathrm{EXP}\,(\widehat{v}) \equiv I_o \cdot e^{(\widehat{v}-V_{\mathrm{DC}})/nV_T} - I_o. \tag{2}$$

In (1)-(2) I_o and V_{DC} are a dc current and a dc voltage, respectively; V_T is the thermal voltage, and n is the subthreshold slope factor of an MOS transistor. Variables with a circumflex represent compressed voltages [5–8].

The above operators describe the compression of the input current into a compressed voltage and the expansion of the intermediate compressed voltage into linear currents. The realization of Log-Domain circuits is performed by employing non-linear transconductors, denoted as $E+$ and $E-$ cells, which are given in Figure 2. The expression of the output current for both of them is given by the following formula:

$$i_{\mathrm{out}} = I_o \cdot e^{(\widehat{v}_{\mathrm{in}}-\widehat{v}_{\mathrm{out}})/nV_T}, \tag{3}$$

where $\widehat{v}_{\mathrm{in}}$ and $\widehat{v}_{\mathrm{out}}$ are the input and output voltages, respectively.

Using (1)–(3) the realization of LOG and EXP operators could be achieved by the topologies given in Figure 3.

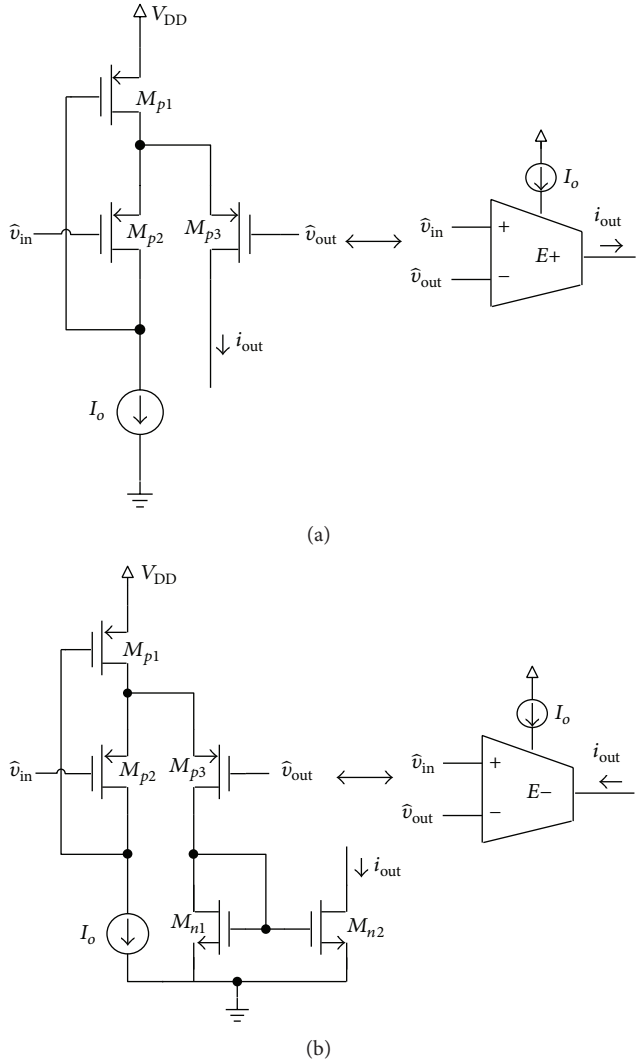

Figure 2: Realization of nonlinear transconductors (a) $E+$ cell and (b) $E-$ cell.

The topology of a Log-Domain two-input lossless integrator is presented in Figure 4. The current that flows through the capacitor $\widehat{C}$ is given by the expression as follows:

$$i_C = \widehat{C}\frac{d\widehat{v}_{\mathrm{out}}}{dt} = I_o \cdot e^{(\widehat{v}_{\mathrm{in}\,1}-\widehat{v}_{\mathrm{out}})/nV_T} - I_o \cdot e^{(\widehat{v}_{\mathrm{in}\,2}-\widehat{v}_{\mathrm{out}})/nV_T}. \tag{4}$$

Multiplying both terms in (4) with the factor $e^{(\widehat{v}_{\mathrm{out}}-V_{\mathrm{DC}})/nV_T}$ and employing the definition of the EXP operator in (3) it is derived, after some algebraic manipulation, that

$$\mathrm{EXP}\,(\widehat{v}_{\mathrm{out}}) = \frac{1}{\widehat{\tau}s}\left[\mathrm{EXP}\,(\widehat{v}_{\mathrm{in}\,1}) - \mathrm{EXP}\,(\widehat{v}_{\mathrm{in}\,2})\right], \tag{5}$$

where $\widehat{\tau} = \widehat{C}nV_T/I_o$ is the realized time constant.

Using (2) the expression in (5) could be also written as in (6):

$$i_{\mathrm{out}} = \frac{1}{\widehat{\tau}s}\left(i_{\mathrm{in}\,1} - i_{\mathrm{in}\,2}\right). \tag{6}$$

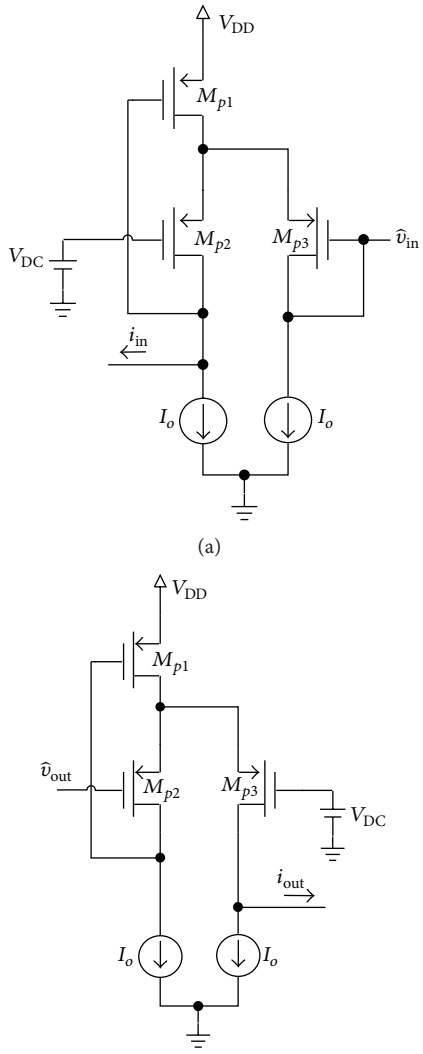

Figure 3: Realization of (a) LOG and (b) EXP operators.

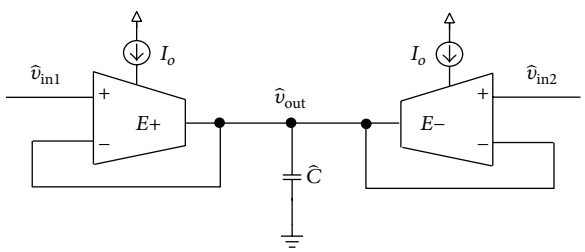

Figure 4: Two-input Log-Domain lossless integrator.

The topology of a Log-Domain two-input lossy integrator is depicted in Figure 5. Performing a similar analysis the expressions in (7) and (8) are obtained:

$$\mathrm{EXP}\left(\widehat{v}_{\mathrm{out}}\right) = \frac{1}{\widehat{\tau}s+1}\left[\mathrm{EXP}\left(\widehat{v}_{\mathrm{in}\,1}\right) - \mathrm{EXP}\left(\widehat{v}_{\mathrm{in}\,2}\right)\right] \tag{7}$$

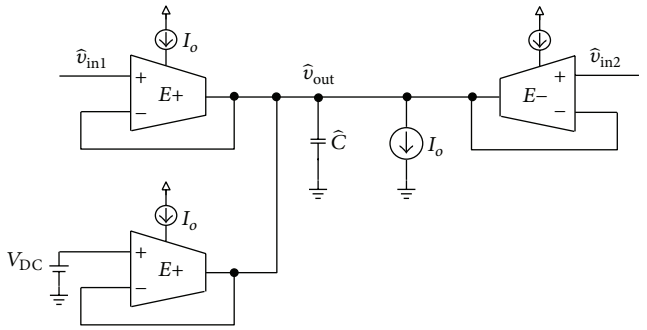

Figure 5: Two-input Log-Domain lossy integrator.

or

$$i_{\mathrm{out}} = \frac{1}{\widehat{\tau}s+1}\left(i_{\mathrm{in}\,1} - i_{\mathrm{in}\,2}\right). \tag{8}$$

The FBD of a 4th-order bandpass filter is given in Figure 6, where the transfer function is

$$\begin{aligned} H(s) = G_1 &\frac{\left(1/\widehat{\tau}_1\right)s}{s^2 + \left(1/\widehat{\tau}_1\right)s + \left(1/\widehat{\tau}_1\widehat{\tau}_2\right)} \\ &\cdot G_2 \frac{\left(1/\widehat{\tau}_3\right)s}{s^2 + \left(1/\widehat{\tau}_3\right)s + \left(1/\widehat{\tau}_3\widehat{\tau}_4\right)}. \end{aligned} \tag{9}$$

The realization of the FBD in Figure 6, using the integrators in Figures 4 and 5 and the compression and expansion blocks in Figure 3, is given in Figure 7. The required gain factors G_1 and G_2 are realized through appropriate sizing of the transistors and dc currents in the corresponding expansion blocks. Also, the realized time constants are given by the formulas: $\widehat{\tau}_1 = \widehat{C}_1 nV_T/I_o$, $\widehat{\tau}_2 = \widehat{C}_2 nV_T/I_o$, $\widehat{\tau}_3 = \widehat{C}_3 nV_T/I_o$, and $\widehat{\tau}_4 = \widehat{C}_4 nV_T/I_o$, respectively.

3. Absolute Value, RMS-DC Converter, and Comparator

A topology that performs the conversion of current into its absolute value is presented in Figure 8 [11]. The operation of this circuit is the following: in the case that the current i_{in} is entering to the topology, transistor M_{p1} is in conduction and the input current is conveyed into the output terminal through the current mirror formed by the transistors M_{n1} and M_{n2}. In the case that the current i_{in} leaves the topology, then transistors M_{p2} and M_{p3} are in conduction and the input current is again conveyed into the output terminal through the current mirror formed by transistors M_{n1} and M_{n2}. Thus, the output current has a constant direction and, simultaneously, its value is equal to that of the input current. This is mathematically described by the following:

$$i_{\mathrm{out}} = \begin{cases} i_{\mathrm{in}} & \text{if } i_{\mathrm{in}} > 0 \\ -i_{\mathrm{in}} & \text{if } i_{\mathrm{in}} < 0. \end{cases} \tag{10}$$

A topology of an RMS-DC converter is depicted in Figure 9 [12]. The dynamic translinear loop is formed by the

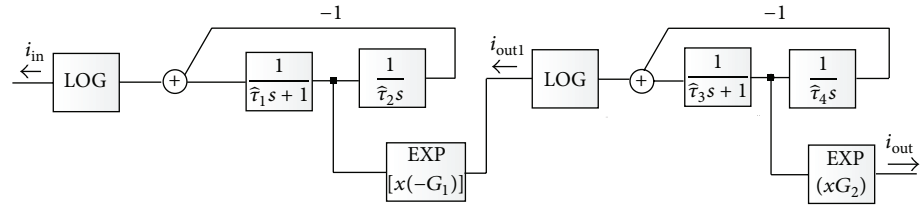

Figure 6: FBD of a 4th-order bandpass filter.

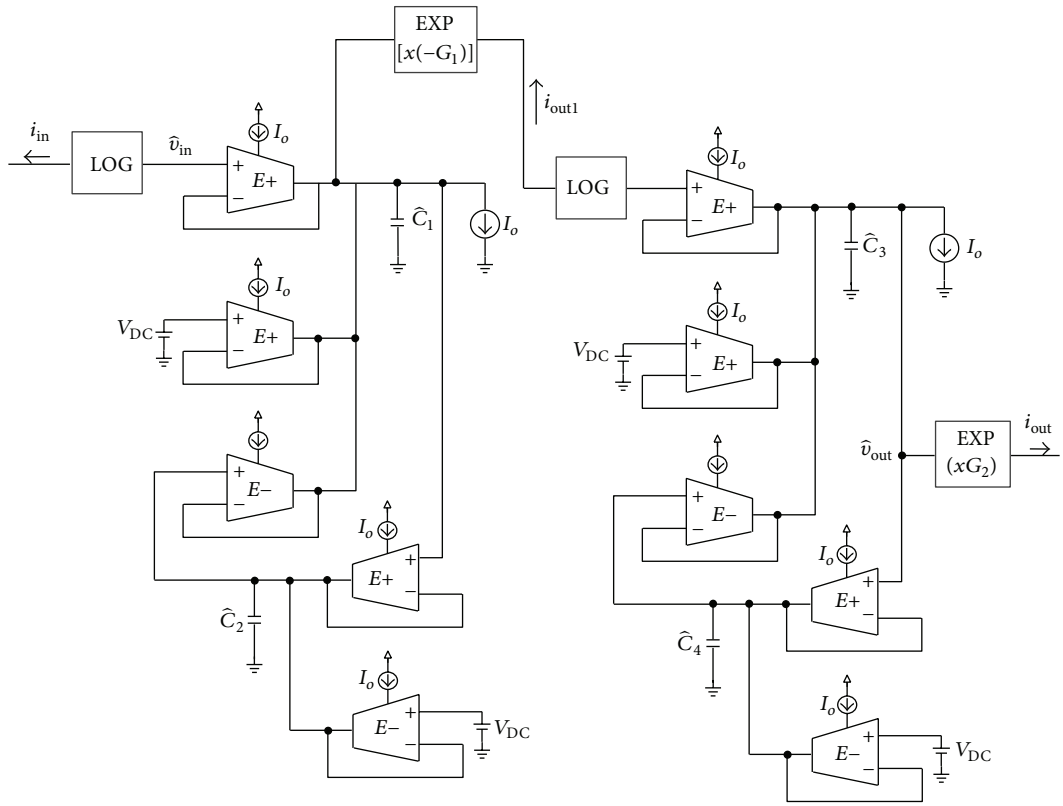

Figure 7: Log-Domain realization of the FBD in Figure 6.

transistors M_{p4}–M_{p6} and the capacitor C_{rms} implementing the following equation: $i_{CAP}i_{out} = C_{rms}nV_T\dot{i}_{out}$, while the static translinear loop formed by the transistors M_{p1}–M_{p6} implements the equation: $(i_{CAP} + I_o)i_{out}^2 = I_o i_{in}^2$. Combining both equations results in

$$C_{rms}nV_T\dot{i}_{out}i_{out} + I_o i_{out}^2 = I_o i_{in}^2. \tag{11}$$

The expression in (11) could be alternatively rewritten as

$$i_{out} = \frac{\overline{i_{in}^2}}{i_{out}}. \tag{12}$$

According to (12) the output current is equal to the rms value of the input current.

A topology of a current comparator is given in Figure 10, where the core introduced in [13] has been employed along with the addition of two inverters in order to increase the speed of operation and achieve rail-to-rail output voltages. When $i_{in} < I_{REF}$, then the output voltage will be equal to zero. In the case that $i_{in} > I_{REF}$, the output voltage will be equal to V_{DD_DIG}.

4. Simulation and Comparison Results

As a first step, the behavior of the building blocks of the cardiac sense amplifier will be evaluated through the utilization of the Analog Design Environment of the Cadence software. MOS transistor parameters provided by the AMS 0.35 μm CMOS process will be used in simulations.

Regarding the bandpass filter, the power supply voltages were chosen to be $V_{DD} = 0.5$ V and $V_{DC} = 100$ mV, while the dc current I_o was equal to 100 pA. Considering that the MOS transistors operate in the subthreshold region, the aspect ratios of M_{p1} and M_{p2}-M_{p3} of the E cells

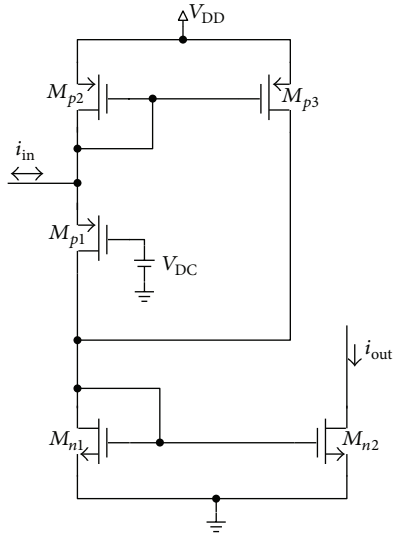

FIGURE 8: Topology of an absolute value circuit.

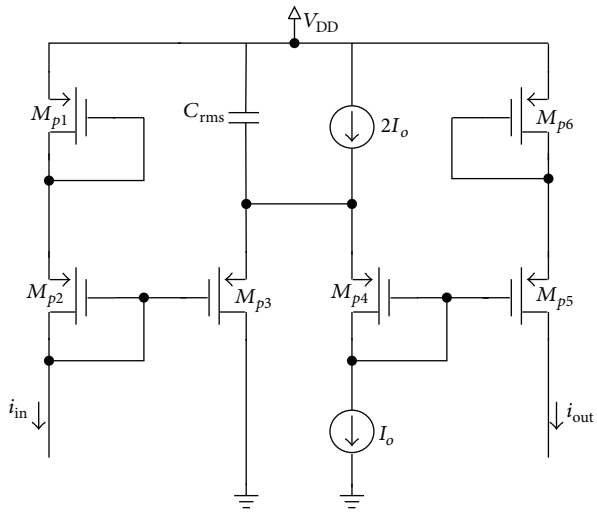

FIGURE 9: Topology of an RMS-DC converter.

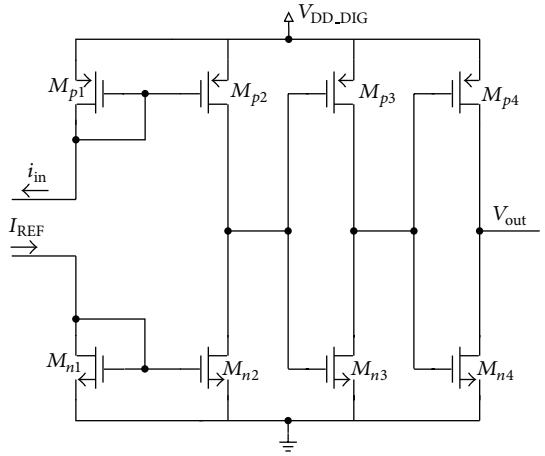

FIGURE 10: Typical current comparator.

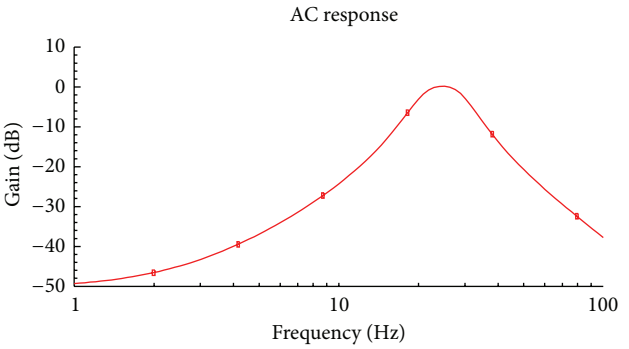

FIGURE 11: Frequency response of the bandpass filter.

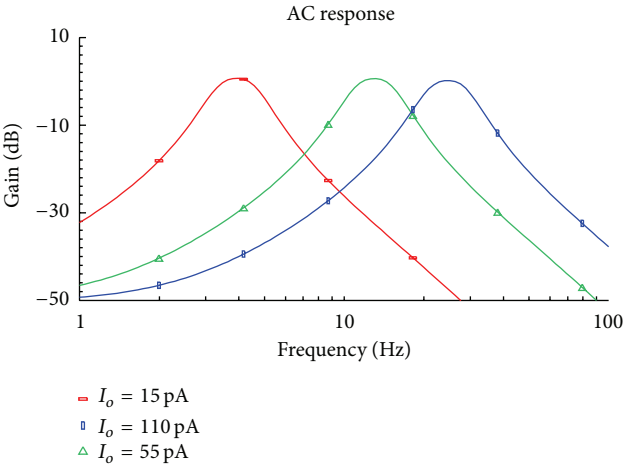

FIGURE 12: Demonstration of the electronic tunability of the filter in Figure 7.

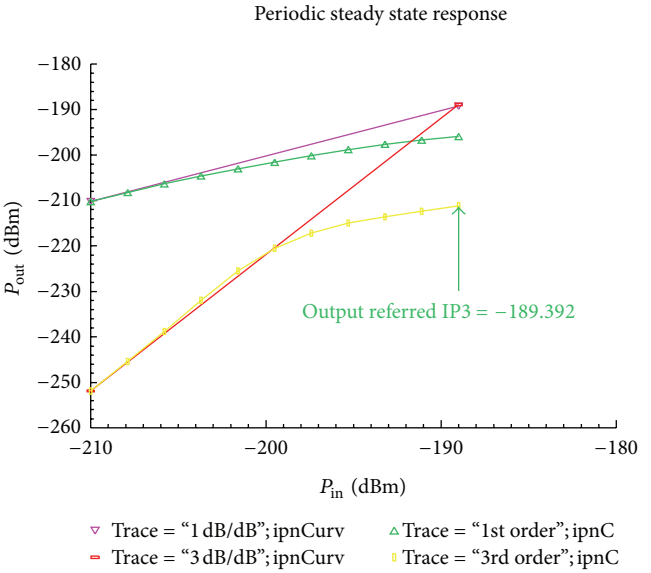

FIGURE 13: Linear performance of the filter in Figure 7.

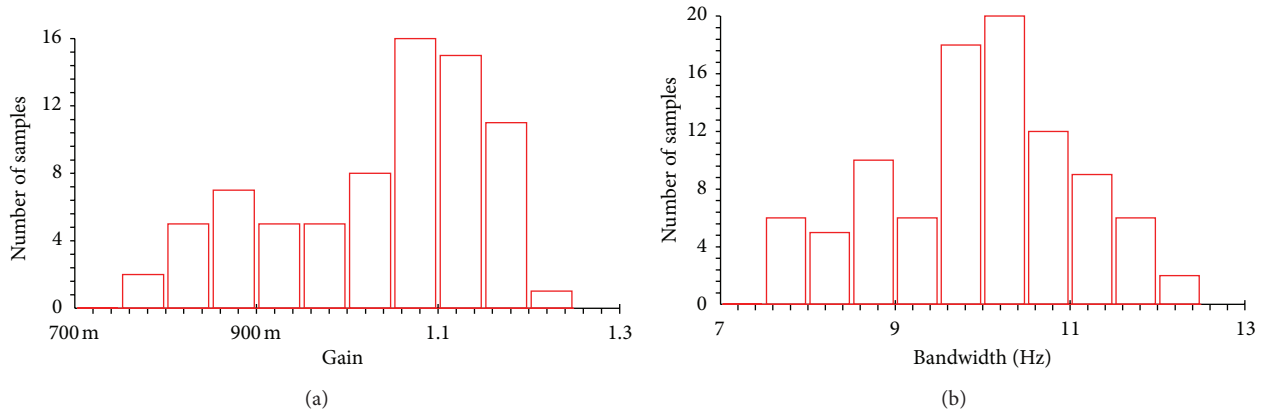

Figure 14: Monte Carlo analysis results about the (a) gain and (b) bandwidth of the filter in Figure 7.

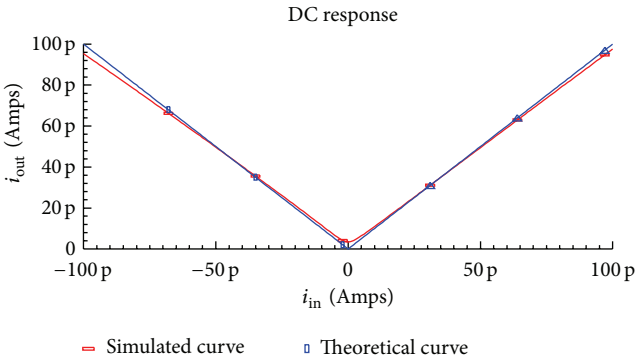

Figure 15: DC transfer characteristic of the absolute value circuit.

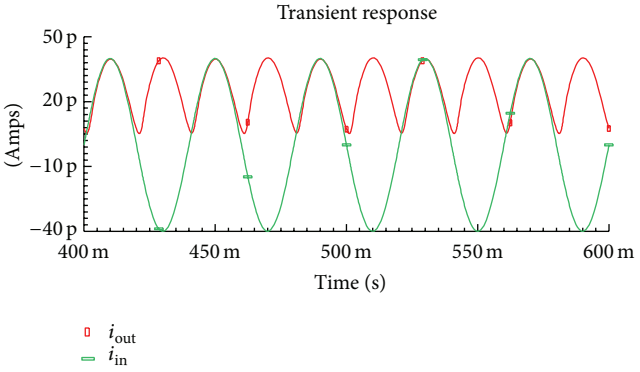

Figure 16: Time-domain behavior of the absolute value circuit.

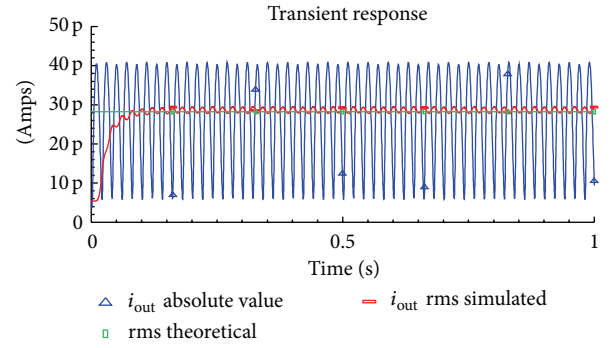

Figure 17: Time-domain behavior of the RMS-DC converter.

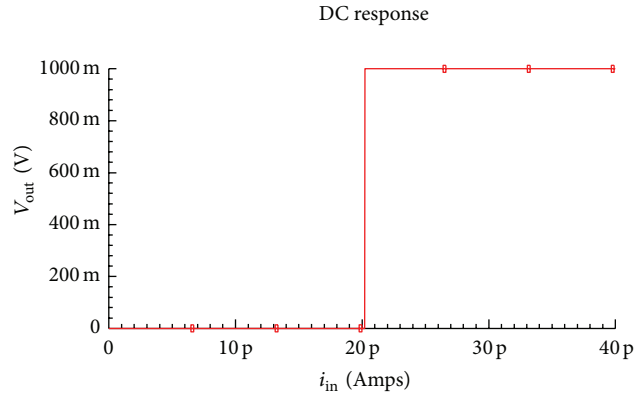

Figure 18: DC transfer characteristic of the current comparator.

in Figure 2 were 70 μm/1 μm and 60 μm/1 μm, respectively, while the aspect ratio of M_{n1}-M_{n2} of the $E-$ cell in Figure 2(b) was 8 μm/1 μm. The distribution of the bias current has been performed through the employment of pMOS and nMOS current mirrors with aspect ratios 20 μm/1 μm and 8 μm/1 μm, respectively.

Considering a bandpass filter with center frequency f_o equal to 25 Hz and a Q factor equal to 2.5, the derived transfer function is given by

$$1.24\frac{50.71\cdot s}{s^2+50.71\cdot s+3.28\cdot 10^4}\cdot 1.65\frac{38.15\cdot s}{s^2+38.15\cdot s+1.856\cdot 10^4}. \quad (13)$$

Comparing (9) and (13) it is derived that $G_1 = 1.24$, $G_2 = 1.65$ while the capacitor values will be $\widehat{C}_1 = 58.3$ pF, $\widehat{C}_2 = 4.57$ pF, $\widehat{C}_3 = 77.6$ pF, and $\widehat{C}_4 = 6.08$ pF.

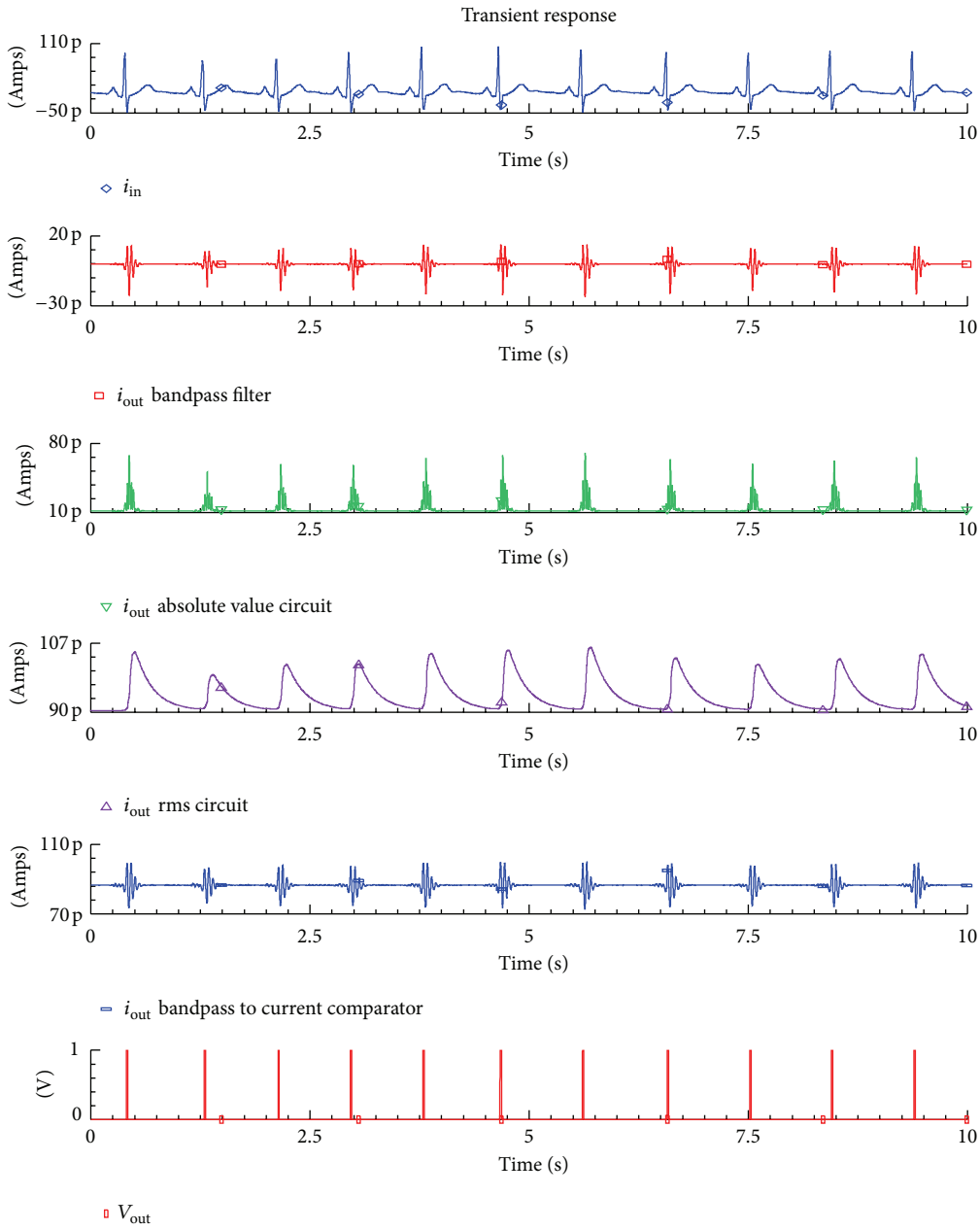

Figure 19: Waveforms for the cardiac sense amplifier.

The obtained gain response of the filter is demonstrated in Figure 11, where the dc current I_o has been adjusted to 110 pA in order to realize a center frequency equal to 25 Hz. The tunability of the filter is demonstrated in Figure 12, where the frequency responses at I_o = 15 pA, 55 pA, and 110 pA are simultaneously given. The center frequency at I_o = 15 pA was 4 Hz, while at I_o = 55 pA the corresponding frequency was 13.2 Hz.

The linear performance of the filter has been studied through the application of two closely spaced tones, located at 25 Hz and 26 Hz, at the input of the filter. The simulated 3rd order intermodulation distortion plot is given in Figure 13, where the output referred 3rd-order intersect point (IIP3) was at −189.4 dBm (76 pA rms value). The noise has been integrated within the passband of the filter, and the rms value of the output referred noise was 0.51 pA. Consequently, the predicted value of the Dynamic Range (DR) of the filter will be 43.4 dB. The dc power consumption of the filter was 2.71 nW.

The sensitivity of the filter with regards to the effects of the process parameters variations and MOS transistor parameters mismatching has been evaluated through the employment of the Monte Carlo analysis offered by the Analog Design Environment. The derived statistical plots are given in Figure 14, where the standard deviation of the gain was 0.12, while the corresponding value for the bandwidth

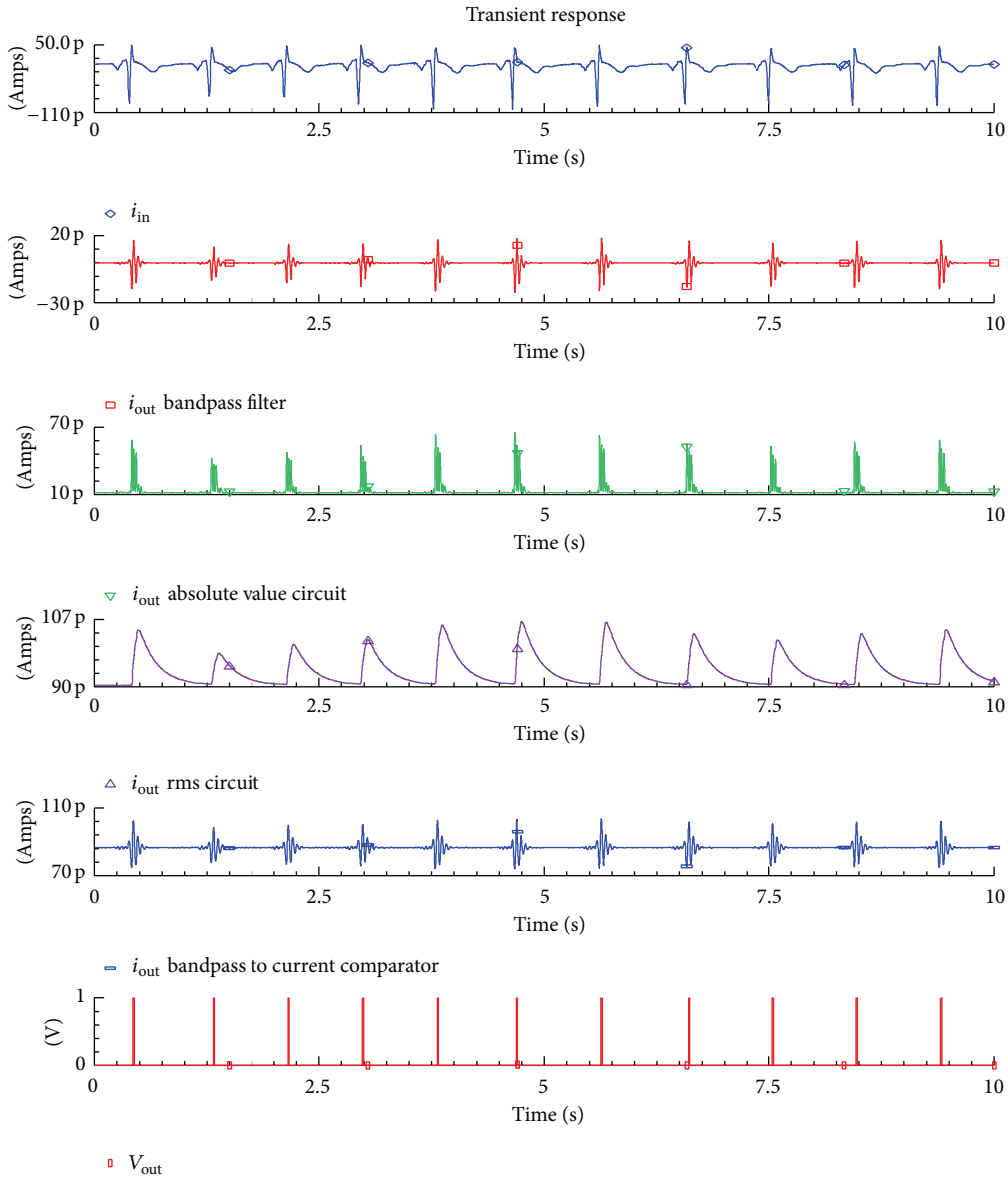

Figure 20: Waveforms for the cardiac sense amplifier with opposite orientation of electrodes.

was 1.1 Hz. Therefore, the filter has reasonable sensitivity characteristics.

The behavior of the absolute value circuit has been evaluated by employing a power supply voltage scheme as $V_{DD} = 0.5$ V and $V_{DC} = 100$ mV. The aspect ratios of M_{p1}, M_{p2}-M_{p3}, and M_{n1}-M_{n2} of the topology in Figure 8 were 16 μm/0.4 μm, 4 μm/0.4 μm, and 20 μm/1 μm, respectively. The dc transfer characteristic of the topology is demonstrated in Figure 15. It is worth mentioning at this point that the input current has a range of variation between −100 pA and +100 pA, which is the possible range of variation for the output current of the bandpass filter. The behavior of the topology in the time domain is given in Figure 16, where the output waveform is plotted for an input current with an amplitude equal to 40 pA.

The performance of the RMS-DC converter circuit has been evaluated by employing the following bias scheme: $V_{DD} = 0.5$ V, $V_{DC} = 100$ mV, and $I_o = 5$ pA. Moreover, the capacitor value was 11 pF. The aspect ratio of M_{p1}–M_{p6} of the topology in Figure 9 was 500 μm/0.35 μm. The distribution of the bias current has been performed using pMOS and nMOS current mirrors with aspect ratios 200 μm/1 μm and 35 μm/4 μm, respectively. The obtained output current waveform for an input signal equal to that obtained from the output of the absolute value circuit (Figure 16) is given in Figure 17. Although there is a variation presented at the output current this is not a problem in the detection of an intracardiac signal, as it was confirmed through exhaustive simulations. This choice has been performed in order to avoid the significantly large capacitor value required for

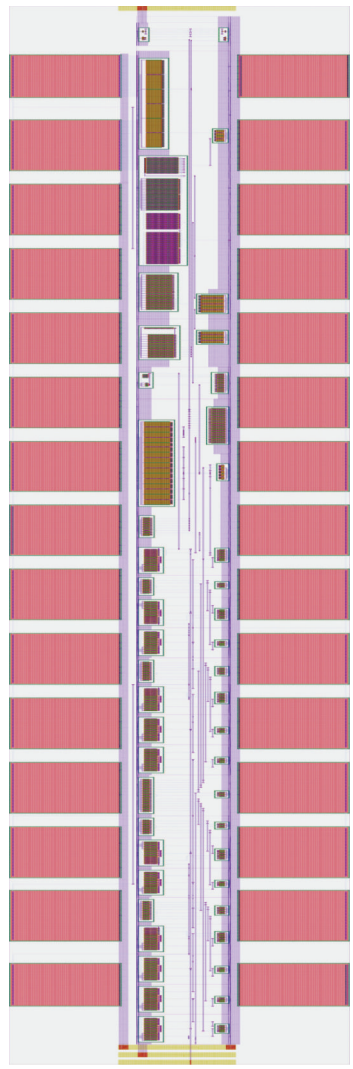

Figure 21: Layout design of the cardiac sense amplifier.

the accurate operation of the RMS-DC converter, which is impractical from the fabrication point of view.

The comparator given in Figure 10 has been biased at $V_{DD\_DIG} = 1\,V$. The aspect ratios were $1\,\mu m/1.5\,\mu m$ for M_{p1}-M_{p2}, $0.5\,\mu m/2\,\mu m$ for M_{n1}-M_{n2}, $1\,\mu m/0.35\,\mu m$ for M_{p3}-M_{p4}, and $0.5\,\mu m/0.35\,\mu m$ for M_{n3}-M_{n4}. The obtained dc transfer characteristic of the comparator for a reference current equal to 20 pA is given in Figure 18, where it is easily concluded that the topology behaves correctly.

The whole system of the cardiac sense amplifier has been simulated using the following conditions: $V_{DD} = 0.5\,V$, $V_{DC} = 100\,mV$, and $V_{DD\_DIG} = 1\,V$. In addition the bias currents for the bandpass filter and the rms converter were 110 pA and 5 pA, respectively. The reference dc current for the comparator was equal to 44 pA. The capacitor values were $\widehat{C}_1 = 58.3\,pF$, $\widehat{C}_2 = 4.57\,pF$, $\widehat{C}_3 = 77.6\,pF$, and $\widehat{C}_4 = 6.08\,pF$ for the bandpass filter and 11 pF for the RMS-DC converter. The MOS transistors aspect ratios were the same as those chosen in the simulations performed for the intermediate stages of the amplifier. Considering cardiac signals which are available from [14], the derived waveforms from the intermediate stages and the output of the amplifier are simultaneously given in Figure 19. Also, in Figure 20 the corresponding waveforms obtained from a reversed position of electrodes are given and the conclusion is that the operation of the amplifier is independent from the position of electrodes. The total power dissipation of the amplifier was 2.92 nW, instead of 240 nW of the topology in [10]. Taking also into account that the analog part of the amplifier operates in a 0.5 V environment and only the comparator requires a 1 V power supply voltage, while the employed bias in the topology in [10] was 2 V, it is concluded that the proposed topology simultaneously offers the benefits of reduced power supply voltage requirement and dc power consumption.

The layout of the whole amplifier is demonstrated in Figure 21; its dimensions were $1818.2\,\mu m \times 267.4\,\mu m$. Performing post layout simulations, the derived input and output

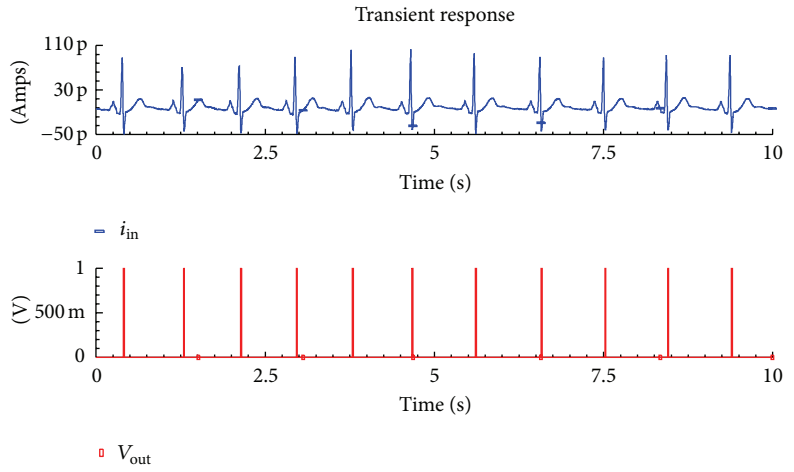

Figure 22: Postlayout simulation results of the cardiac sense amplifier.

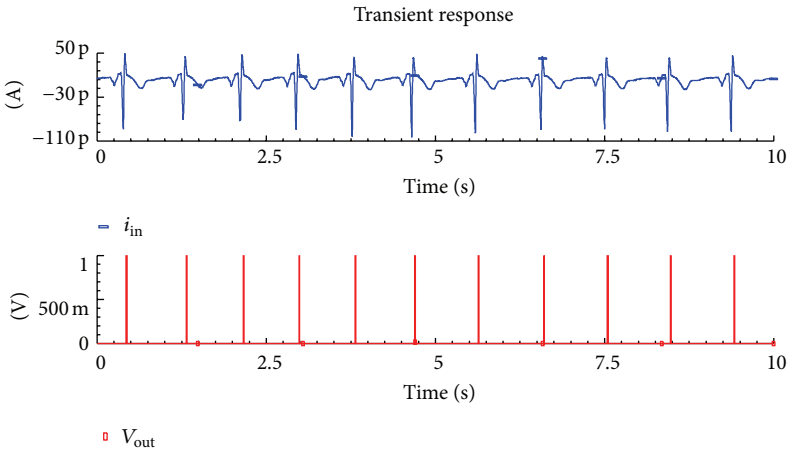

Figure 23: Postlayout simulation results of the cardiac sense amplifier with opposite orientation of electrodes.

waveforms for both possible orientations of electrodes are given in Figures 22 and 23, where it is readily obtained that the proposed topology behaves as it was expected.

5. Conclusion

The proposed cardiac sense amplifier, realized by employing MOS transistors in the subthreshold region and the concept of the Log-Domain filtering, offers the benefits of the capability of operation in an ultralow voltage environment and the reduced dc power consumption. The postlayout simulation results confirmed its correct behavior, and, thus, it could be an attractive candidate for realizing high performance modern biomedical signal processing systems.

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