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Research Article

Reduced Precision Redundancy for Satellite Telecommand Receiver Module on FPGA

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A novel and highly efficient design of a software defined radiation tolerant baseband module for a LEO satellite telecommand receiver using FPGA is presented. FPGAs in space are subject to single event upsets (SEUs) due to high radiation environment. Traditionally, triple modular redundancy (TMR) is used for mitigating Single Event Upsets (SEUs). The drawback of using TMR is that it consumes a lot of hardware resources and requires more power. Reduced precision redundancy (RPR) can be a viable alternative of TMR in digital systems for arithmetic operations. This paper uses the combination of RPR and TMR for mitigating SEUs. The designed module consumes less resources on FPGA and has bit error rate (BER) identical to theoretical results, apart from degradation due to implementation losses. An improved Costas loop and timing recovery algorithm are implemented for achieving carrier recovery and bit synchronization. The hybrid approach mitigates SEUs while consuming 26% less resources than a customary TMR protected receiver.

1. Introduction

Reconfigurability and adaptability are one of the most desirable features of modern space technology. FPGA provides this flexibility along with good performance. They have become an integral part of satellite systems for over a decade. Their high computational capacity combined with small size and light weight makes them a preferable choice over other digital systems. The ability to reconfigure FPGA with an updated functionality reduces the hardware requirement in space craft [1].

However, FPGAs face some severe problems in the space environment. The high energy particles in space may interact with memory cells within an integrated circuit and can change their logic state [2]. This alteration may disrupt the operation of a digital system defined by memory cells. FPGAs contain large array of memory cells which makes them more susceptible to single event upsets (SEUs).

In order to operate properly in space, some mitigation techniques need to be applied in FPGAs. Traditionally, triple modular redundancy (TMR) has been used for this purpose. The drawback of using TMR is that it consumes a lot of hardware resources and requires more power [3]. Thus, there has been a constant effort to find an alternative to the TMR technique. Shim and Shanbhag [4] introduced reduced precision redundancy (RPR) as part of a power-reduction technique for ASIC-based systems; Snodgrass [5] demonstrated variation of RPR on FPGA to limit high magnitude errors of arithmetic operations in high radiation environment. Pratt et al. [6] have presented the hybrid approach using RPR and TMR for FPGA-based communication systems.

This paper presents a highly efficient design of a software defined radiation tolerant module for a LEO satellite telecommand receiver. The proposed module uses the combination of RPR and TMR for SEU mitigation. To the best of the authors knowledge, this hybrid approach is not being implemented to a satellite telecommand receiver module using binary phase shift keying (BPSK) modulation. During the literature review, it was found that the BPSK receiver of Maya et al. [7] and our design have same technical specifications. So it was taken as a benchmark for fair resource utilization. The designed module consumes less resources, and its bit error rate (BER)

is approaching 10^{-6}. This paper evaluates the effect of SEUs on the BER performance of a telecommand receiver.

The paper is organized as follows. Section 2 explains the impact of high radiation environment of space on FPGA and introduces the concept of RPR. In Section 3, the detailed implementation of our proposed telecommand receiver and SEU mitigation technique using RPR is described. Section 4 shows the hardware cosimulation results. Section 5 presents the conclusions drawn from the results.

2. FPGA in Space Environment

2.1. Single Event Upsets. In SRAM-based FPGAs, a large area is composed of memory cells. These memory cells contain both user data and circuit configuration data that defines the functionality of a system. When high energy charged particles such as neutrons and alpha particles present in the space environment interact with SRAM cells, they occasionally invert thir logic state. This phenomenon is called SEU [2]. The inverted logic state can be both of user data or configuration data and can cause unpredictability in systems behavior. The SEU directly affects the bit error rate performance of a communication receiver. Four general classes of SEUs are identified according to their effect on BER [6].

(1) In class 1 SEUs, lower order bits of arithmetic operations (such as output of accumulator or coefficient of a filter) are affected. They are 30%–77% of the total SEUs.

(2) In class 2 SEUs, middle order bits of arithmetic operations are affected. They are 17%–64% of the total SEUs.

(3) In class 3 SEUs, higher order bits of arithmetic operations are affected. They cause severe degradation in circuit performance and are unacceptable. They constitute 3%-4% of the total SEUs.

(4) In class 4 SEU, clock distribution, global reset signals, MSB of filter, or threshold comparator is affected. They are termed "catastrophic" and reduced BER to 1âĄĎ2. They constitute 2%–4% of the total SEUs.

So classes 3 and 4 SEUs are more critical and need to be mitigated proficiently. Various techniques have been used in the past to mitigate classes 3 and 4 SEUs, the most popular being the TMR technique [6]. In TMR, three replicas of the same circuit are made, and they are connected to a voter block which selects the correct output among them. TMR, however, consumes a lot of resources and power. On the other hand, a resource efficient alternative to TMR for arithmetic operations is "RPR." In this paper, we have presented the application of RPR to the arithmetic operations involved in the design of a telecommand receiver.

2.2. Reduced Precision Redundancy. In RPR, the full precision (FP) module to be protected is replicated twice with reduced precision (RP) as shown in Figure 1. The decision block uses the output of RP modules to determine the error in FP module as follows:

$$\begin{aligned} &\text{if } \left(\left(\left|\mathrm{FP}_{\mathrm{out}} - \mathrm{RP1}_{\mathrm{out}}\right| > T_h\right), \left(\mathrm{RP1}_{\mathrm{out}} = \mathrm{RP2}_{\mathrm{out}}\right)\right) \\ &\qquad \text{output} = \mathrm{RP2}_{\mathrm{out}} \\ &\text{else} \\ &\qquad \text{output} = \mathrm{FP}_{\mathrm{out}}. \end{aligned} \tag{1}$$

Threshold (T_h) value is a very critical parameter in RPR. If T_h is very small, false error detection will occur, and if T_h value is high, error will not be detected. In order to avoid this problem, the T_h value is set equal to the difference between the FP and RP modules' outputs as shown in (2) when there is no error:

$$T_h = \left|\mathrm{FP}_{\mathrm{out}} - \mathrm{RP}_{\mathrm{out}}\right|. \tag{2}$$

The reduced precision redundancy factor (k) is a tradeoff between mitigation cost and SEU performance [6]. Therefore, the size of RP modules and decision block must be chosen in such a way that they consume less resource than TMR while mitigating SEUs. RPR can be applied to arithmetic operations of any size and complexity, whether it is a simple FIR filter or a complex receiver.

Unlike TMR, RPR is not suited for every application. It is only applicable to those arithmetic operations that can be approximated with a reduced precision.

3. Implementation of Telecommand Receiver and SEU Mitigation

3.1. Telecommand Receiver. This paper focuses on the implementation of a baseband processing module on FPGA and its SEU mitigation. The data rate of the designed system is set to be 1 Mbps, and baseband carrier frequency is 4 MHz. BPSK modulation is used in telecommand link due to its strong anti-interference, good spectral performance, fast transfer rates, and good BER [8].

The algorithms and concepts used in the receiver system are validated using high level design tools (i.e., MATLAB/SIMULINK) providing the flexibility to simulate, debug, and analyze the functionality of each working block. Moreover, they accelerate the design process and assist in verifying the accuracy of the algorithms. The designed receiver is realized on FPGA using Xilinx System Generator, a system level design tool for FPGA.

Coherent demodulation approach is adopted due to its good BER and high SNR performance as compared to the noncoherent one [8]. The designed system as shown in Figure 2 contains the following submodules: carrier recovery, integration, bit synchronization, and decision block.

The Costas loop is used for achieving the carrier recovery of BPSK modulated signal as shown in Figure 3. Carrier recovery is performed for extracting the RF carrier from a received modulated signal which is then used to recover the data from it [9]. The incoming baseband signal is first downsampled by a factor of two which reduces the

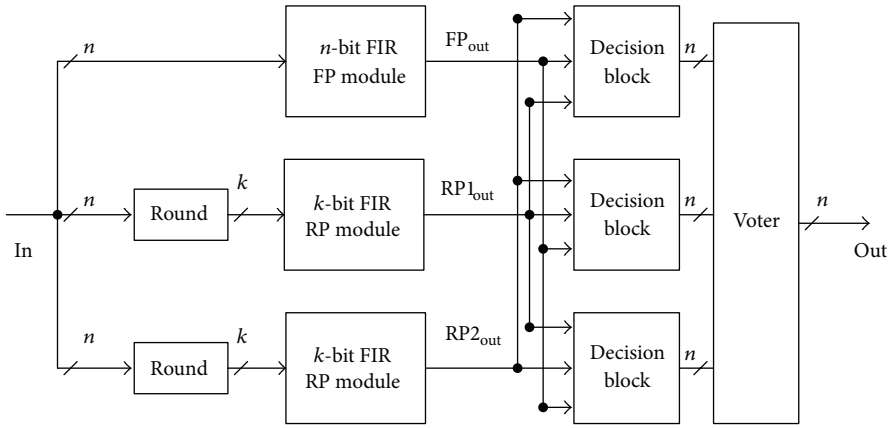

Figure 1: Block diagram of an n-bit FIR filter protected with k-bit RP modules.

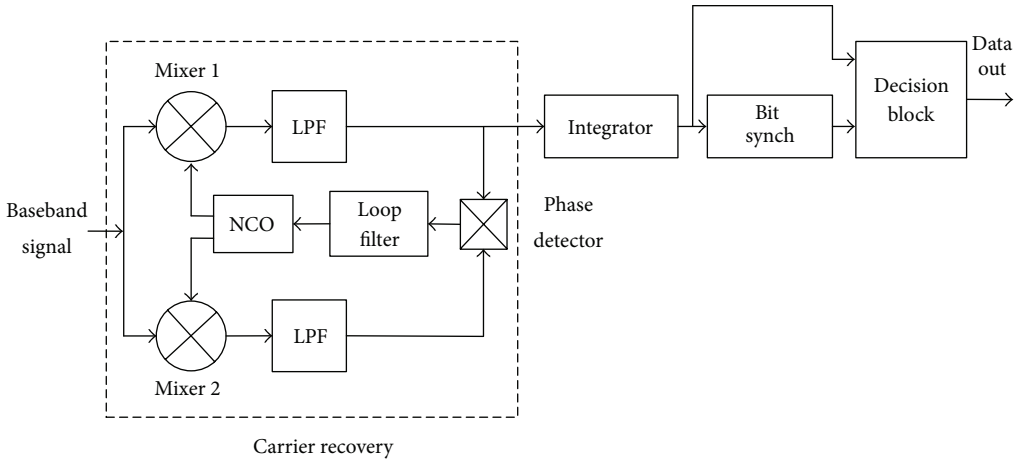

Figure 2: Telecommand receiver.

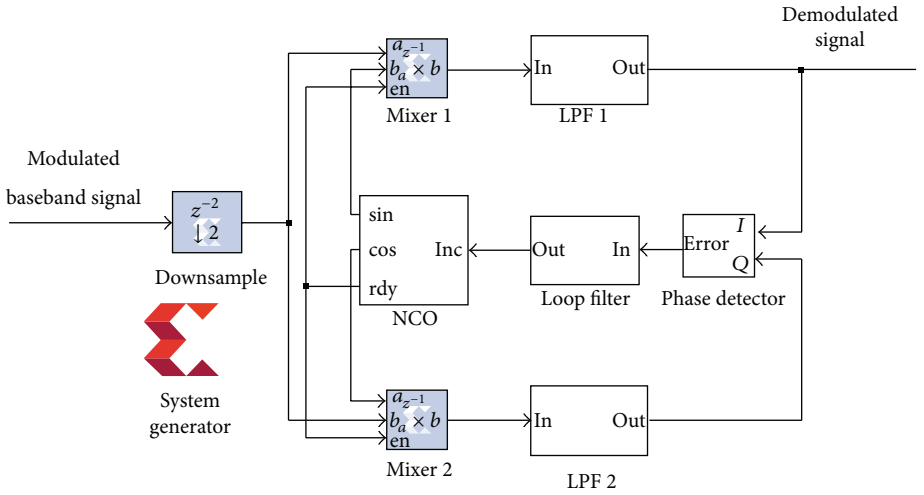

Figure 3: Implementation of Costas loop.

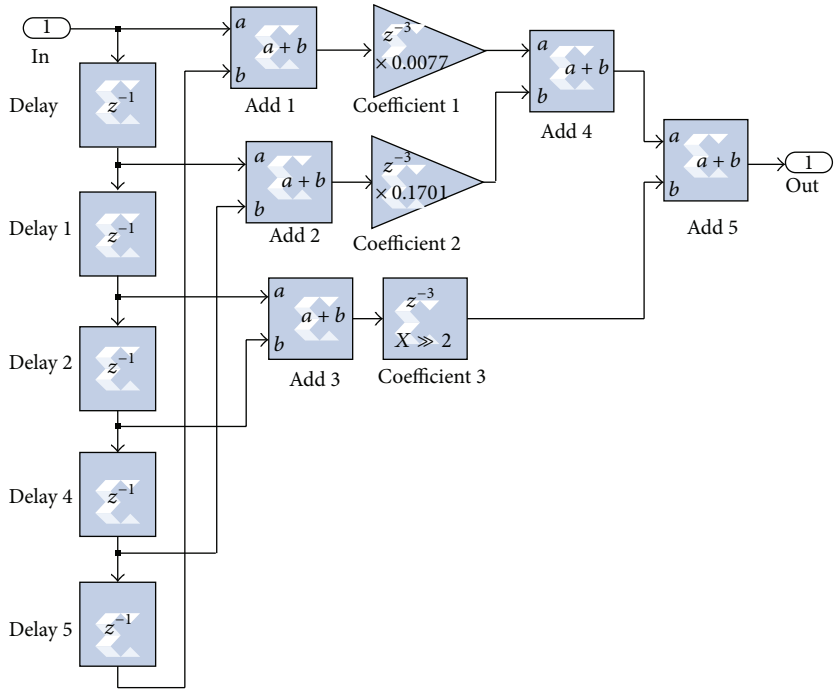

Figure 4: Implementation of Low pass Filter.

sampling frequency to half for the rest of the system. This downconverted signal is mixed by the 14 × 14 bits multiplier of in-phase channel (I-channel) and quadrature channel (Q-channel) with sine and cosine signals, respectively. These orthogonal sinusoids are generated through numerical controlled oscillator (NCO). The NCO is implemented by using Direct Digital Synthesizer compiler 4.0 (DDS 4.0) in FPGA with 96 dBc spurious-free dynamic range (SFDR). The accumulator size of DDS is 18 bits with the output signal width set to 14 bits. These values ensure the least resource utilization along with desired performance. The I and Q channel multiplier outputs are passed through a fifth order low pass FIR filter to remove high frequency components. Our designed filters are realized using direct form symmetric architecture as shown in Figure 4. This architecture uses the symmetry in the coefficients of filter and requires half the multiplier and adders compared to other architectures and thus consumes less resources on FPGA. Moreover, one of the filters coefficients is implemented through binary shift operation which further reduces resource consumption. The low pass filters in each channel are designed wide enough to pass the data modulation without distortion [10].

The filtered I and Q channel signals are passed on to phase detector (PD) block. It extracts the phase difference between I and Q signals. It is implemented by using small angle approximation [11]. Loop filter removes the high frequency leakages of the phase detector. It provides a smooth and stable 18-bit control word to the NCO for modifying its output frequency and phase with respect to input signal. When the NCO's generated carrier frequency and phase are synchronized with the incoming signals frequency and phase, the demodulated signal is produced at the I channel. The designing of loop filter is a very sensitive task as it determines the bandwidth of the loop and controls NCO's output. The loop filter is a first order Butterworth IIR filter and is entirely implemented by binary shift registers without using embedded multipliers. The designed Costas loop can demodulate input signal with Doppler shifts up to 10 percent of the carrier frequency.

The demodulated signal is applied to the integrator module. It accumulates the signal over one bit duration before resetting itself which produces triangular wave at the output. The resetting of integrator is the core of timing synchronization and is performed exactly after one bit duration. The design of integrator module is accomplished by using an accumulator block with the timing control module. Integrator's output is processed by the bit synchronization unit which uses an improved form of early late gate sampling algorithm as shown in Figure 5. The algorithm is implemented by using relational operators rather than arithmetic operators in order to avoid any floating-point arithmetic. It uses three samples (i.e., early (E), present (P), and late (L)) and a threshold value (T_h) to detect the peak of the signal which determines the sampling instant for the bit. The algorithm used is as follows:

$$\text{if } \left(\left(|E| < |P|\right), \left(|L| < |P|\right), \left(|P| \geq T_h\right)\right) \\ \text{Peak detect} = 1. \tag{3}$$

The peak detect signal is sent to the data sampler and preamble match modules. Data sampler consists of a counter along with relational operators to sample the signal. The preamble match module is composed of a Block RAM to

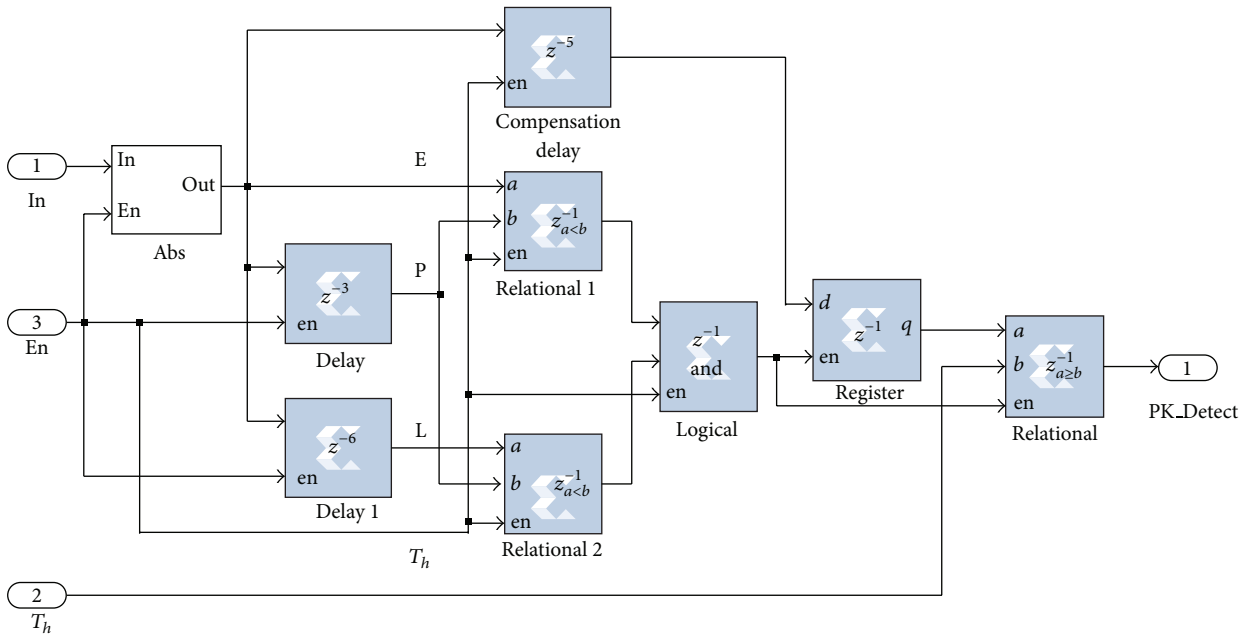

Figure 5: Early-late gate sampling block.

store the preamble bits and relational operators for comparing the preamble with sampled bits. When the peak detect signal is asserted, the preamble module compares the sampled bits from data sampler with the prestored preamble bits. After successful matching of the preamble, the decision block starts sampling the integrator module output, and thus data bits are recovered at the output port. The complete receiver implementation is pipelined to maximize the timing performance. It has been observed during simulations that the data sampling at integrator's output produces good BER than sampling of demodulated output from Costas loop.

3.2. SEU Mitigation. As mentioned earlier, RPR is not suited to all types of applications and designs. For applications comprising arithmetic and nonarithmetic operations, combination of both RPR and TMR is the best approach for mitigating SEUs [6]. The baseband processing module of a telecommand receiver is composed of arithmetic and nonarithmetic operations.

The designed system was analysed to identify the potential areas where RPR application would cause significant reduction in resource consumption for the complete system. It was observed that the low pass filters and mixers of I and Q channel consist of bulk of arithmetic operations. In fact they constitute more than half of the total design resources. This makes them ideal contenders for RPR. Phase detector comprises multiplication operation, which is better suited for RPR than TMR [12]. Loop filter is composed of binary shift registers which makes RPR ineffective. The decision block contains no arithmetic operation, so it cannot be protected using RPR. Experimentally, it was determined that, due to the high cost of RPR decision blocks, it is more efficient to apply TMR to NCO, integrator, and the bit synchronization module. The diagram of a telecommand receiver module is shown in Figure 6 with annotations indicating the type of mitigation technique applied to each system block.

The suitable value of RPR factor ($k = 7$) is determined which reduces the size of RPR module while ensuring good SEU mitigation. The threshold value (T_h) is set to be the maximum difference between FP and RP modules.

4. Results

The proposed design of the telecommand receiver module is implemented on Xilinx System Generator. The module was hardware cosimulated using Spartan 3E XCS3E500E-4FG320 FPGA as shown in Figure 7. Hardware cosimulation incorporates FPGA hardware into the simulation and automates the data exchange process between hardware and software. The data is processed in FPGA, and the results are displayed in system generator.

Results from graphs shown in Figure 8 confirm that the Sync_lock signal (a) and received data bits (b) from Xilinx System Generator simulation are identical to the Sync_lock signal (d) and data received bits (e) results from hardware cosimulation. BER analysis of the receiver module is performed using "BERtool" provided in MATLAB. The BER performance of the overall designed system is calculated using Monte Carlo simulation. Figure 9 presents a comparison between the BER of the proposed system and the ideal BPSK receiver in AWGN channel. It can be seen that the proposed systems BER is almost identical to the BER of the ideal receiver. The slight degradation in BER graph of the designed module is due to the implementation losses.

The proposed module's logic utilization on FPGA and its comparison with Maya et al. [7] are presented in Table 1. It can be seen that the designed system consumes 50% less multipliers, 1% less slices, and 5% less 4-input LUTS as

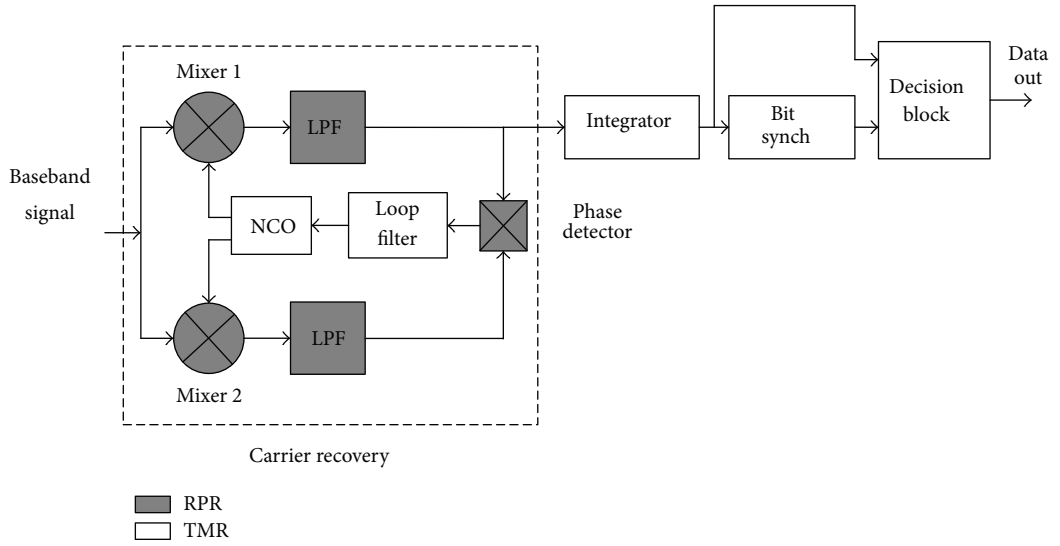

Figure 6: Telecommand receiver annotated for RPR + TMR mitigation.

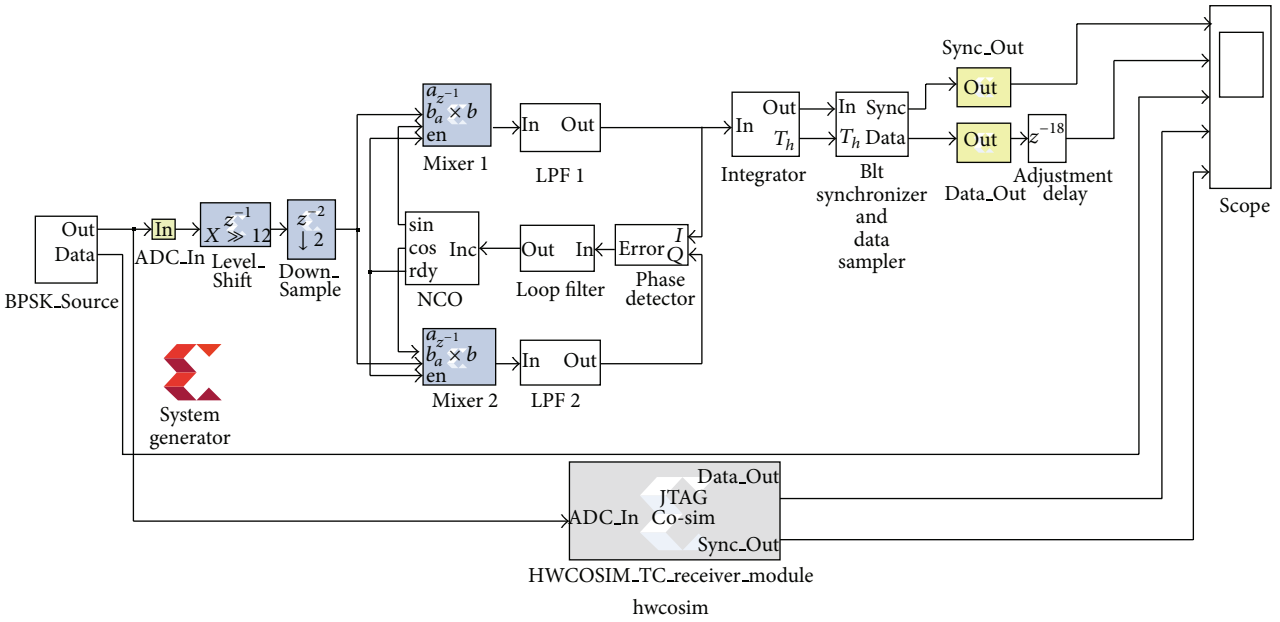

Figure 7: Telecommand Receiver Model.

Table 1: Resource comparison of the proposed receiver module and Maya et al. [7] on Spartan 3E.

Logic utilization	Carrier recovery Used		Timing recovery Used		Total avail.	Utilization Percentage %	
	This work	[7]	This work	[7]		This work	[7]
Slice	553	607	155	387	4,656	15	16
Slice flip flops	759	732	158	651	9,312	9	13
4-input LUTS	677	973	136	503	9,312	8	13
RAMB16s	1	2	1	0	20	10	10
MULT18 × 18s	3	2	0	4	20	15	30
BUFGMUXs	1	1	1	1	24	4	8

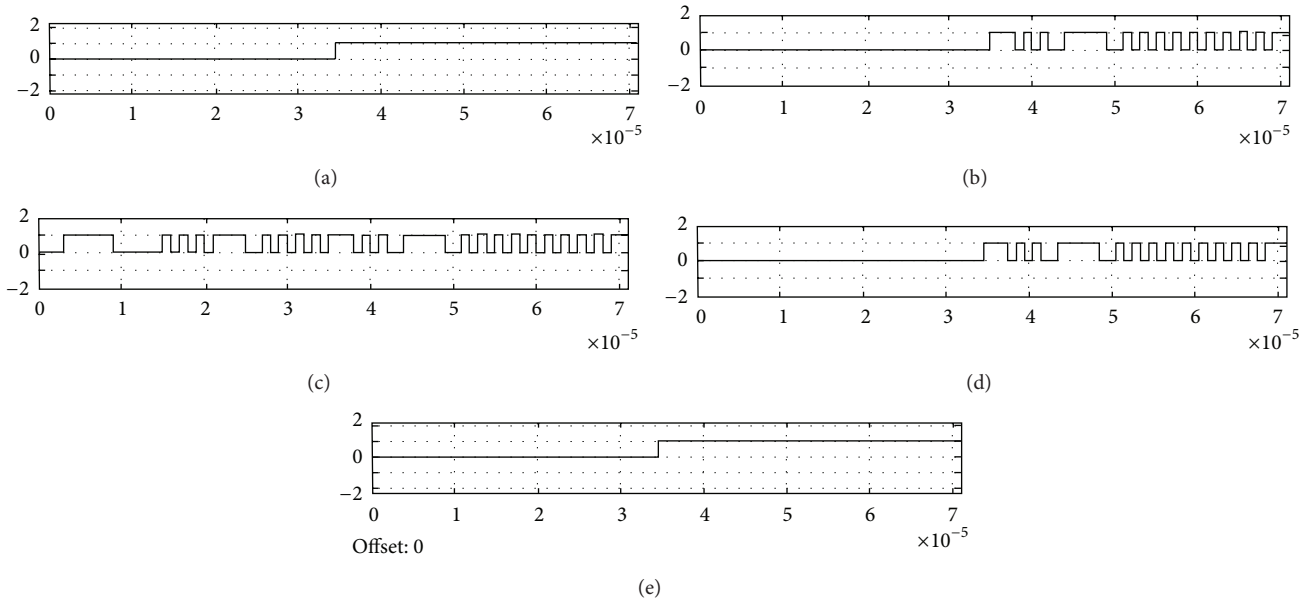

FIGURE 8: (a) System generator Syn_lock, (b) System generator Received bits, (c) Transmitted bits, (d) Hardware cosim Received bits, and (e) Hardware cosim Sync_lock.

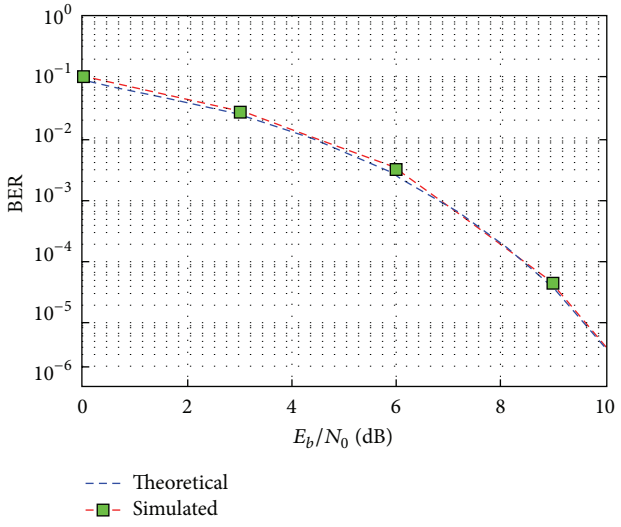

FIGURE 9: BER of telecommand receiver.

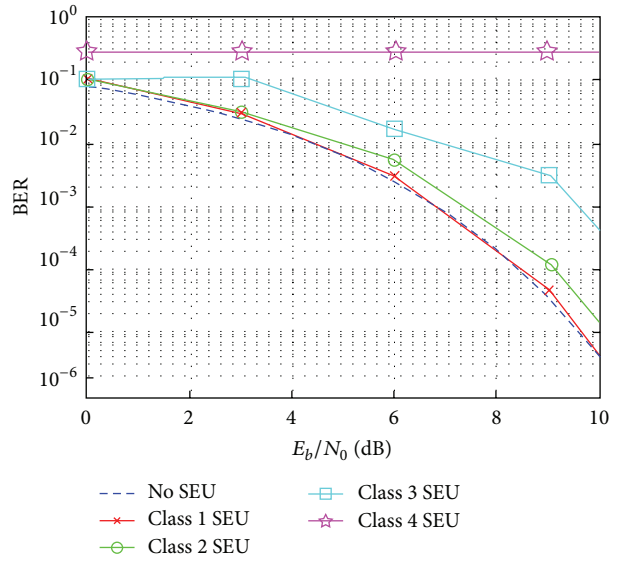

FIGURE 10: SEU effect on BER performance.

compared to [7]. The timing recovery unit of the proposed system consumes almost 60% less slices as compared to [7] and uses no multiplier.

The SEU effect is emulated by inverting a bit in the design. For this purpose, loop filter is selected because it plays a critical role of keeping the demodulator and receiver in the desired working area and an upset in it would have a major impact on receiver's performance. Class 1 SEU, is introduced by inverting the LSB of the loop filter. Class 2 SEU is simulated by flipping the middle order bit of the loop filter. Higher order bit is flipped for class 3 SEU. The MSB of the loop filter is inverted for class 4 SEU. The effect of SEU on BER performance with respect to different classes is shown in Figure 10.

It can be observed from Figure 10, that all classes of SEUs have different impact on BER performance. Class 1 and 2 SEUs cause minor degradation in BER and are not critical. These errors can be corrected using standard techniques. Class 3 and 4 SEUs have a devastating impact on BER; redundancy must be used in order to enhance the BER.

TMR and RPR application increases the overall size of the designed system by introducing its replicas. Therefore, a different FPGA platform was required that can meet the

Table 2: Resource comparison of TMR and RPR + TMR on VIRTEX 4.

Logic utilization	TMR Used	RPR + TMR Used	Available	Resource reduction (%)
Slice	2,572	1,901	24,576	26.08
Slice flip flops	3,149	1,817	49,152	42.29
4-input LUTS	2,721	2,240	49,152	17.68

resource requirements. We decided to implement TMR and the combination of RPR and TMR using Virtex 4 XC4VSX55-10FF1148 FPGA. Both methods mitigate SEUs successfully, and their resource comparison is presented in Table 2. The results show that the hybrid approach is more efficient in terms of resources as compared to TMR. The combination of RPR and TMR consumes 26% less slices, 42% less slice flip-flops, and almost 18% less 4-input LUTS as compared to TMR.

5. Conclusion

This paper presents a new technique for software defined radiation tolerance of baseband module for a LEO satellite telecommand receiver. The combination of RPR and TMR is used in the receiver module for SEU mitigation. This hybrid approach has shown to be very effective and consumes far less resource than a customary TMR protected receiver. The adopted scheme uses a resource efficient implementation of Costas loop for carrier recovery and early late gate sampling algorithm for timing recovery. The optimized receiver module has BER performance identical to theoretical results, with minor degradation due to implementation losses. It has been concluded that by focusing on targeted implementation of RPR in systems involving arithmetic operations, a lot of resources can be saved as compared to complete TMR system. Future work would include RF front end connected with the FPGA hardware to perform real time measurements and change the RPR redundancy factor (k) to evaluate its impact on systems BER performance.

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