

## Research Article

# Companding Realizations of the Nonlinear Energy Operator

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Realizations of the nonlinear energy operator (NEO), using the concept of companding filtering, are introduced and compared in this work. For this purpose, the Log-Domain and Sinh-Domain filtering techniques have been followed. Both topologies are constructed from differentiator and multiplier blocks which have been realized through the utilization of nonlinear transconductor cells. Both of the proposed topologies offer the capability of ultra-low voltage operation, thanks to the employment of MOS transistors in the weak inversion. Considering a single power supply voltage of 0.5 V, the behavior of the proposed NEO realizations has been simulated using the Analog Design Environment of the Cadence software and the design kit of the TSMC 130 nm process. Comparison results show that the Sinh-Domain realization offers a more power efficient design than that offered by the Log-Domain realization.

## 1. Introduction

Owing to its efficiency for estimating the instantaneous product of amplitude and frequency of a signal, the NEO is a very powerful tool for handling biomedical signals. A number of NEO realizations have been already introduced in the literature [1–4]. The topology in [1] operates in a supply voltage 1.8 V, while a dual  $\pm 1.65$  V supply voltage scheme has been used in [3]. A power supply voltage 2 V has been utilized in the topology in [4], while the topology in [2] operates at 0.6 V.

Conventional linear Operational Transconductance Amplifiers (OTAs) have been utilized for realizing the topologies in [1, 3]. A drawback of these realizations is the restriction for handling signals with relatively low amplitude, so that the conditions for small-signal operation are fulfilled, and the transconductance parameter of the corresponding MOS transistors can be employed. The same restriction is also valid for the realization in [2], where the small-signal transconductance parameter of current mirror has been utilized for realizing the required resistors.

Companding realizations do not suffer from the aforementioned limitation, due to the fact that an externally linear system could be constructed from nonlinear active blocks.

Thus, there is an absence of employment of linearization techniques and/or small-signal operation conditions for achieving the linear operation of the whole system. Therefore, for given amplitude of the input current, the bias current could be chosen smaller than that in the case of the conventional linear systems [5–13]. In the Log-Domain implementation in [4], the required nonlinear transconductors have been constructed from translinear loops formed by bipolar transistors operated in forward active region.

In biomedical applications, an ultra-low power voltage environment is present, and also the power dissipation of the system should be as low as possible for increasing the life of the implanted device. Thus, MOS transistors operating in the weak inversion must be employed for the realization of the nonlinear transconductors.

Realizations of the NEO, employing the concept of Log-Domain and Sinh-Domain filtering, are introduced in this work. The employment of MOS transistors operating in subthreshold region offers the advantage of operation in a single power supply voltage equal to 0.5 V, which is the minimum among the already known NEO realizations. The paper is organized as follows: the realization of the NEO using the concept of Log-Domain filtering is given in Section 2,

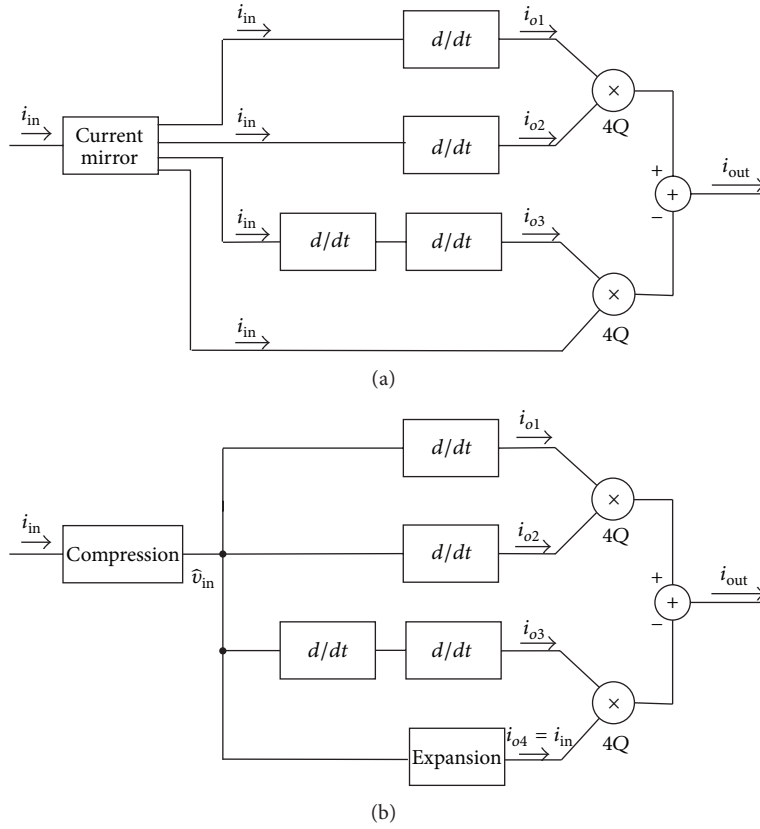


FIGURE 1: FBD of the NEO realization using the (a) conventional and (b) companding filtering.

while the corresponding Sinh-Domain realization is given in Section 3. The evaluation and comparison of the performance of the proposed systems are given in Section 4, by employing the Analog Design Environment of the Cadence software and the design kit provided by the TSMC 130 nm process.

## 2. Log-Domain Realization of NEO

The Functional Block Diagram (FBD) of the NEO realization using the conventional filtering is given in Figure 1(a), where the operation described by (1) is performed to the input signal  $i_{in}(t)$  as follows:

$$i_{out}(t) = \left( \frac{d}{dt} i_{in}(t) \right)^2 - i_{in}(t) \cdot \left( \frac{d^2}{dt^2} i_{in}(t) \right). \quad (1)$$

Following the concept of companding filtering, the input current should be converted into a compressed voltage which will be processed by the nonlinear intermediate blocks. The produced nonlinear compressed output voltages are converted into linear currents in order to preserve the linear operation of the whole system. This is demonstrated in the FBD in Figure 1(b). According to this FBD, the building blocks required for realizing the NEO are compression and expansion blocks, differentiators, and four-quadrant multipliers in order to realize the required quadrature and product terms.

In the case that the concept of the Log-Domain filtering will be followed for realizing the required differentiators, the conversion of the input current ( $i_{in}$ ) into a compressed voltage ( $\hat{v}_{in}$ ) and the expansion of the intermediate output voltages into linear currents ( $i_{o1}-i_{o4}$ ) will be described by the following set of complementary operators:

$$\hat{v}_{in} = \text{LOG}(i_{in}) \equiv V_{DC} + nV_T \cdot \ln \left( \frac{i_{in} + I_o}{I_o} \right), \quad (2)$$

$$i_{oi} = \text{EXP}(\hat{v}_{oi}) \equiv I_o \cdot e^{(\hat{v}_{oi} - V_{DC})/nV_T} - I_o \quad i = 1, \dots, 4. \quad (3)$$

In (2)-(3),  $I_o$  and  $V_{DC}$  are a dc current and a dc voltage, respectively,  $V_T$  is the thermal voltage, and  $n$  is the subthreshold slope factor of a MOS transistor. Also, variables with a circumflex represent compressed voltages [7–9, 13].

Using (3), the expression in (1) could be alternatively rewritten as in (4)

$$\begin{aligned} \text{EXP}[\hat{v}_{out}(t)] &= \left( \frac{d}{dt} \text{EXP}[\hat{v}_{in}(t)] \right)^2 \\ &\quad - \text{EXP}[\hat{v}_{in}(t)] \cdot \left( \frac{d^2}{dt^2} \text{EXP}[\hat{v}_{in}(t)] \right). \end{aligned} \quad (4)$$

The realization of Log-Domain circuits is performed by employing nonlinear transconductors denoted as E+ and E–

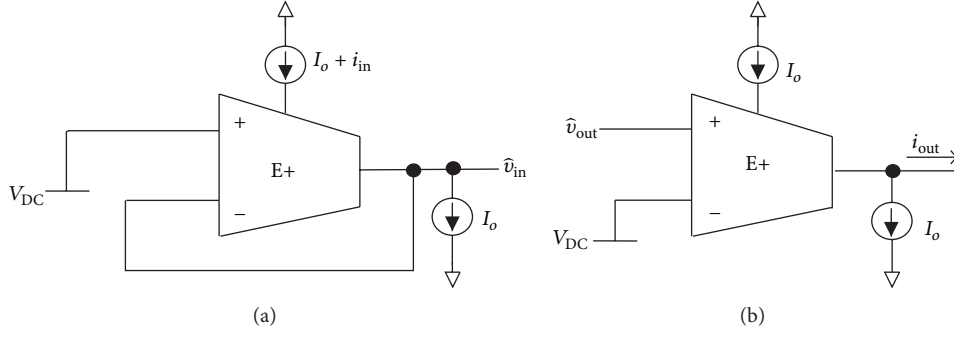


FIGURE 2: Realization of (a) compression and (b) expansion in the Log-Domain.

cells [8, 9, 13]. The expression of the output current for both of them is given by the formula in (5) as

$$i_{out} = I_o \cdot e^{(\hat{v}_{in+} - \hat{v}_{in-})/nV_T}, \quad (5)$$

where  $\hat{v}_{in+}$  and  $\hat{v}_{in-}$  are the voltages at their noninverting and inverting inputs, respectively.

Using (3) and (5), it is easily derived that the compression of the input current is achieved by an appropriately configured E+ cell, as it is depicted in Figure 2.

The topology of a Log-Domain differentiator is presented in Figure 3. The current that flows through the capacitor  $\hat{C}$  is given by the expression

$$i_C = \hat{C} \frac{d\hat{v}_{out1}}{dt} = I_o \cdot e^{(\hat{v}_{in} - \hat{v}_{out1})/nV_T} - I_o. \quad (6)$$

Multiplying both terms in (6) with the factor  $e^{(\hat{v}_{out1} - V_{DC})/nV_T}$  and employing the definition of the EXP operator in (3), it is derived, after some algebraic manipulation, that

$$\frac{\text{EXP}(\hat{v}_{out1})}{\text{EXP}(\hat{v}_{in})} = \frac{i_{out1}}{i_{in}} = \frac{1}{\hat{\tau}s + 1}, \quad (7)$$

where  $\hat{\tau} = \hat{C}nV_T/I_o$  is the realized time constant.

The output current of the E+ cell at the top of the Figure 3 is equal to  $i_{in}$ ; taking into account that the output current is given by the expression  $i_{out} = i_{in} - i_{out1}$  and employing (7), the realized transfer function is

$$H(s) = \frac{i_{out}}{i_{in}} = \frac{\hat{\tau}s}{\hat{\tau}s + 1}. \quad (8)$$

According to (8), the topology in Figure 3 approximates a differentiator within a frequency range where the condition  $f \ll I_o/2\pi\hat{C}nV_T$  is valid.

The topology of the proposed current-mode multiplier, constructed from only E cells, is depicted in Figure 4. This is based on the concept introduced in [14], where conventional OTAs have been employed. The upper leftmost E+ cell is configured in a way that the input current  $i_1$  is converted into a compressed voltage given by (2). The same operation is performed by the E+ cell which is handling the other input current  $i_2$ . The output current of the multiplier could be expressed as

$$i_{out} = i_{out1} - (i_1 + i_2 + I_o). \quad (9)$$

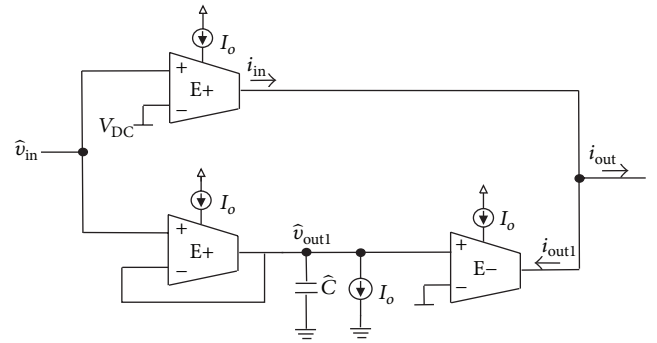


FIGURE 3: Topology of differentiator in the Log-Domain.

Using (2) and (5), the intermediate output current  $i_{out1}$  is expressed as

$$i_{out1} = \frac{(i_1 + I_o) \cdot (i_2 + I_o)}{I_o}. \quad (10)$$

Substituting (10) into (9), the derived expression for the output current is

$$i_{out} = \frac{i_1 \cdot i_2}{I_o}. \quad (11)$$

Owing to the fact that either input currents could be positive or negative, the topology in Figure 4 is a four-quadrant multiplier. In addition, the following restriction should be fulfilled:  $i_1 + I_o > 0$  and  $i_2 + I_o > 0$ . These are imposed from the fact that the currents  $i_1 + I_o$  and  $i_2 + I_o$  are bias currents for E cells, and therefore, the topology in Figure 4 is a class-A current-mode multiplier.

### 3. Sinh-Domain Realization of NEO

Another possible realization of the NEO is through the utilization of the concept of Sinh-Domain filtering. Compared with their Log-Domain counterparts, Sinh-Domain filters offer better compression for both positive and negative values of the input current and an intrinsic class-AB operation. Thus, they can handle currents with a level greater than that of the bias current. On the other hand, the circuit complexity is increased in comparison with that needed in the case of Log-Domain filters [6, 10, 11].

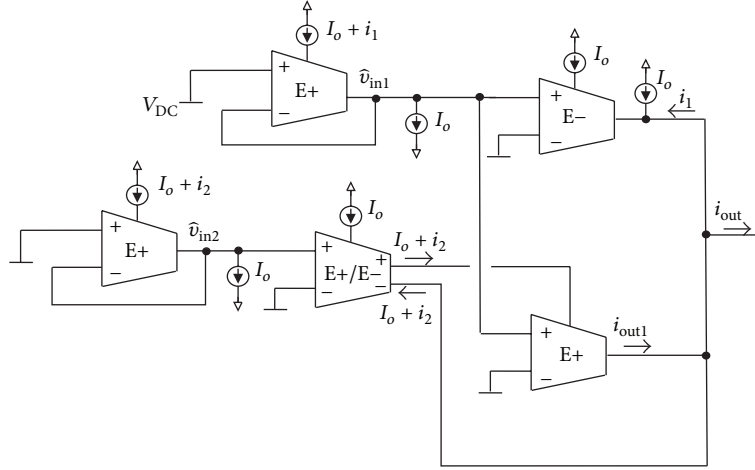


FIGURE 4: Four-quadrant multiplier using E cells.

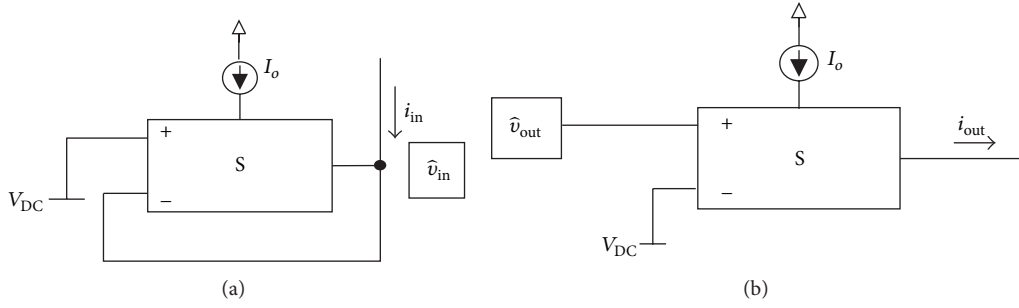


FIGURE 5: Realization of (a) compression and (b) expansion in the Sinh-Domain.

The realization of the required compression and expansion operations denoted in the FBD in Figure 1(b) will be performed by employing appropriate transconductor cells which are mentioned in the literature as S cells. Their output current is given by the expression in (12) as

$$i_{\text{out}} = 2I_o \cdot \sinh\left(\frac{\hat{v}_{\text{in}+} - \hat{v}_{\text{in}-}}{nV_T}\right), \quad (12)$$

where  $\hat{v}_{\text{in}+}$  and  $\hat{v}_{\text{in}-}$  are the voltages at their noninverting and inverting inputs, respectively, [6, 11].

In addition, the set of complementary operators introduced given in (13)-(14) will be used as follows:

$$\hat{v} = \text{SINH}^{-1}(i) \equiv V_{\text{DC}} + nV_T \cdot \sinh^{-1}\left(\frac{i}{2I_o}\right), \quad (13)$$

$$i = \text{SINH}(\hat{v}) \equiv 2I_o \cdot \sinh\left(\frac{\hat{v} - V_{\text{DC}}}{nV_T}\right). \quad (14)$$

Using (12)-(14), the topologies that perform the compression and expansion in the Sinh-Domain are depicted in Figure 5 [6, 11].

A Sinh-Domain first-order high-pass filter is demonstrated in Figure 6. The current that flows through the capacitor  $\hat{C}$  is given by the expression

$$\begin{aligned} i_C &= \hat{C} \frac{d\hat{v}_{\text{out}1}}{dt} \\ &= 2I_o \\ &\cdot \frac{2I_o \cdot \sinh(\hat{v}_{\text{in}} - V_{\text{DC}})/nV_T - 2I_o \cdot \sinh(\hat{v}_{\text{out}1} - V_{\text{DC}})/nV_T}{2I_o \cdot \cosh(\hat{v}_{\text{out}1} - V_{\text{DC}})/nV_T} \end{aligned} \quad (15)$$

Using the definition of the sinh operator in (14) and performing some algebraic manipulation, it is derived from (15) that

$$\frac{\text{SINH}(\hat{v}_{\text{out}1})}{\text{SINH}(\hat{v}_{\text{in}})} = \frac{i_{\text{out}1}}{i_{\text{in}}} = \frac{1}{\hat{\tau}s + 1}, \quad (16)$$

where  $\hat{\tau} = \hat{C}nV_T/2I_o$  is the realized time constant.

The output current is established as  $i_{\text{out}} = i_{\text{in}} - i_{\text{out}1}$ , and employing (16), the transfer function in (8) is also realized by the topology in Figure 6. Thus, it approximates a differentiator within a frequency range where the condition  $f \ll I_o/\pi\hat{C}nV_T$  is valid.

A four-quadrant class-AB current multiplier topology, constructed from S cells, has been already proposed in

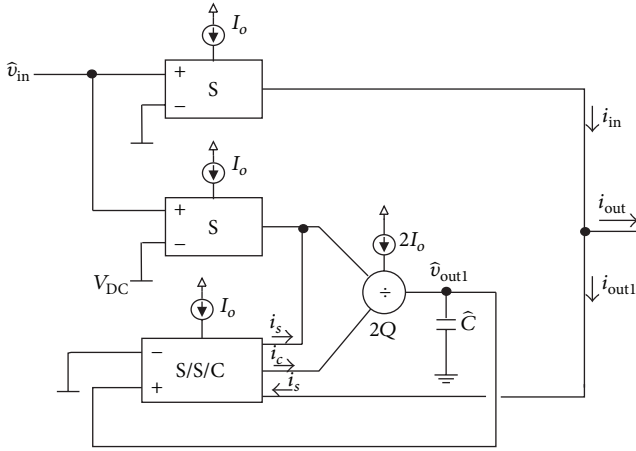


FIGURE 6: Topology of differentiator in the Sinh-Domain.

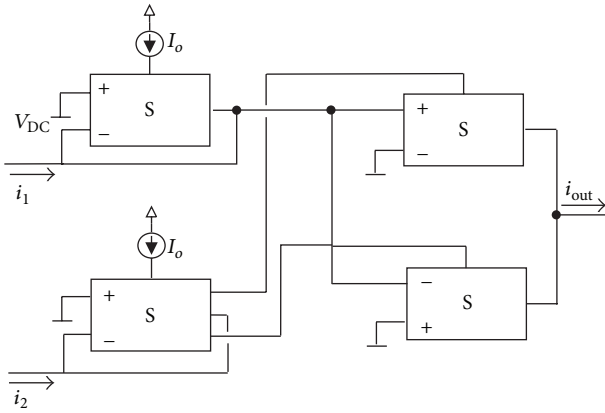


FIGURE 7: Four-quadrant multiplier using S cells.

[15, 16]. In order to facilitate the reading, the topology is recalled in Figure 7, while the expression for the output current is given by (11).

#### 4. Simulation and Comparison Results

**4.1. Simulation and Results.** The behavior of both Log-Domain and Sinh-Domain differentiators has been evaluated through the Analog Design Environment of the Cadence software. MOS transistor parameters provided by the TSMC 130 nm CMOS technology have been used in simulations. The employed E+ and S cells are given in Figures 8 and 9, respectively. It should be mentioned at this point that the required E- cells could be realized through the utilization of an extra current mirror at the output of a E+ cell, while the required replicas of the hyperbolic sine outputs of the S cells could be implemented using multiple output current mirrors.

With respect to the Log-Domain realization, the power supply voltages were chosen to be  $V_{DD} = 0.5$  V and  $V_{DC} = 250$  mV, while the dc current  $I_o$  was equal to  $0.6$  nA. The aspect ratios (i.e., the ratio of the width over the length of the channel of a MOS transistor) of  $M_{p1}$ - $M_{p2}$ ,  $M_{p3}$ - $M_{p4}$ , and  $M_{p5}$  in Figure 8 were chosen to be  $1\text{ }\mu\text{m}/1\text{ }\mu\text{m}$ ,  $1\text{ }\mu\text{m}/10\text{ }\mu\text{m}$ , and

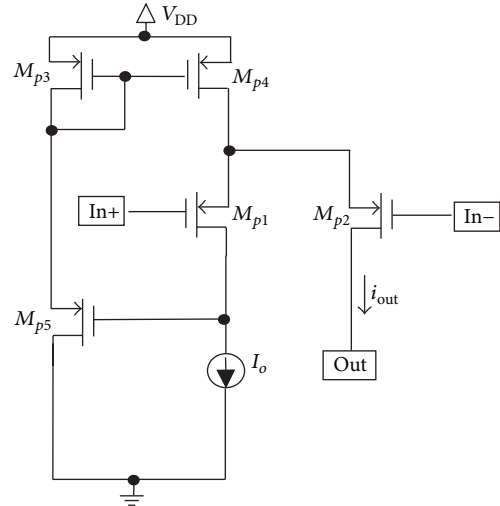


FIGURE 8: Circuitry of an E+ cell.

$1\text{ }\mu\text{m}/6\text{ }\mu\text{m}$ , respectively. The choice of these values has been performed in order to keep the operation of MOS transistors in the subthreshold region. In other words, the following conditions should be fulfilled:  $V_{GS} - V_{TH} < -100$  mV, where  $V_{GS}$  is the gate-source voltage and  $V_{TH}$  is the threshold voltage, and  $V_{DS} > 100$  mV, where  $V_{DS}$  is the drain-source voltage. The obtained gain and phase responses of the Log-Domain differentiator are given in Figure 10. Taking into account that the frequency range of Action Potentials (APs) is within 100 Hz and 10 kHz [1], it is readily obtained from the provided plots that the topology fulfils the aforementioned requirement.

The behavior of the Sinh-Domain differentiator has been evaluated through the utilization of the following bias scheme:  $V_{DD} = 0.5$  V and  $V_{DC} = 250$  mV,  $I_o = 0.3$  nA. The choice of the halved bias current, with regards to the Log-Domain realization, has been done in order to achieve the same impedance level for both realizations, and this is achieved from the fact that a time constant in the Log-Domain is given by the formula:  $\tau = \hat{C}nV_T/I_o$ , while the corresponding formula in the Sinh-Domain is  $\tau = \hat{C}nV_T/2I_o$ . The aspect ratios of  $M_{p1}$ - $M_{p8}$ ,  $M_{p9}$ - $M_{p10}$ , and  $M_{n1}$ - $M_{n8}$  were chosen to be  $1\text{ }\mu\text{m}/1\text{ }\mu\text{m}$ ,  $1\text{ }\mu\text{m}/6\text{ }\mu\text{m}$ , and  $1\text{ }\mu\text{m}/10\text{ }\mu\text{m}$ , respectively. The simulated frequency responses of the Sinh-Domain differentiator are given in Figure 11. According to the provided plots, the gain response is linear with the frequency, while the phase response is almost constant at  $90^\circ$  within the frequency range of APs (100 Hz–10 kHz).

The time-domain behaviour of the proposed NEO realizations will be studied through the consideration of an EEG stimulus [17]. In the case of Log-Domain realization, the maximum amplitude of the EEG signal that could be successfully handled (i.e., recognition of the APs) is equal to  $0.15$  nA, and the corresponding input and output waveforms are depicted in Figure 12.

Due to the class-AB nature of the Sinh-Domain realization, an EEG signal with maximum amplitude about  $0.45$  nA could be handled, and the simulated waveforms are provided

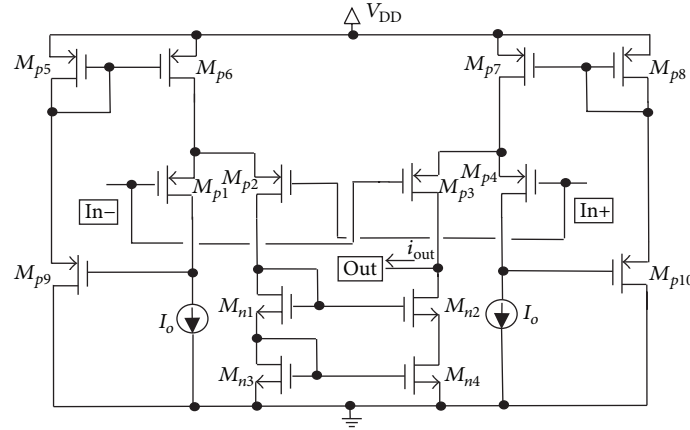


FIGURE 9: Circuitry of an S cell.

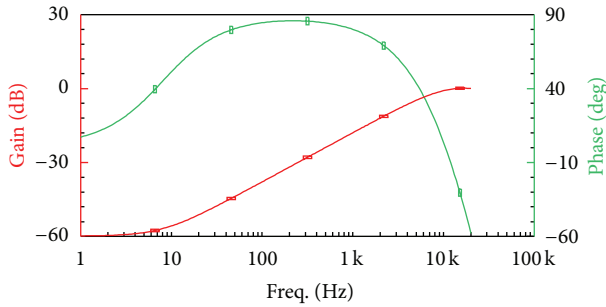


FIGURE 10: Gain and phase responses of the topology in Figure 3.

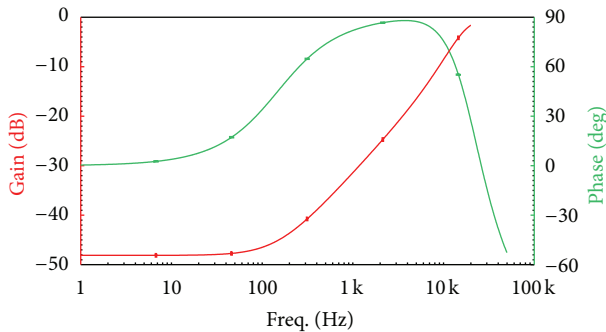


FIGURE 11: Gain and phase responses of the topology in Figure 6.

in Figure 13. The total power dissipation of the whole Log-Domain system was 31.4 nW, while the corresponding value for the Sinh-Domain system was 63.4 nW.

**4.2. Discussion.** According to the provided simulation results, the Sinh-Domain realization is capable of handling a maximum signal with amplitude three times the amplitude of the signal that could be successfully handled by the corresponding Log-Domain realization. On the other hand, the dc power dissipation of the Sinh-Domain realization is doubled compared to that of the Log-Domain realization. Therefore, the Sinh-Domain realization is attractive in terms

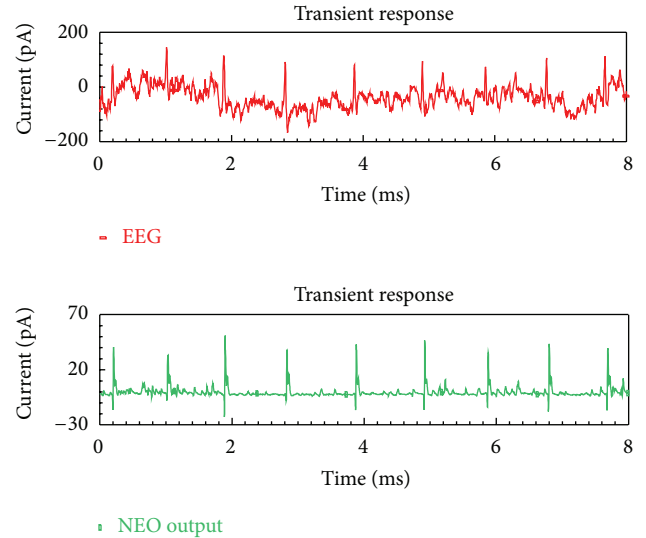


FIGURE 12: Input and output waveforms of the proposed Log-Domain NEO realization.

of power efficiency, and this is originated from its inherent class-AB operation. On the other hand, the Log-Domain realization offers a simpler circuitry than that of its Sinh-Domain counterpart.

With regards to the power supply voltage environment, the topologies in [1–4] operate in supply voltages 1.8V,  $\pm 1.65$ V, 2V, and 0.6V, respectively. Both the companding realizations operate in a 0.5 V supply voltage which is the minimum among the topologies under consideration. This is originated from their companding nature, where the intermediate voltages are compressed versions of the voltages of corresponding conventional topologies.

The corresponding values of power dissipation were 170 nW for the topology in [1],  $2.7 \mu$ W for the topology in [3],  $7.2 \mu$ W for the topology in [4], and 76.2 nW for the topology in [2]. Thus, the proposed configurations offer the minimum required power dissipation compared with the corresponding already proposed schemes. Taking also into account that they



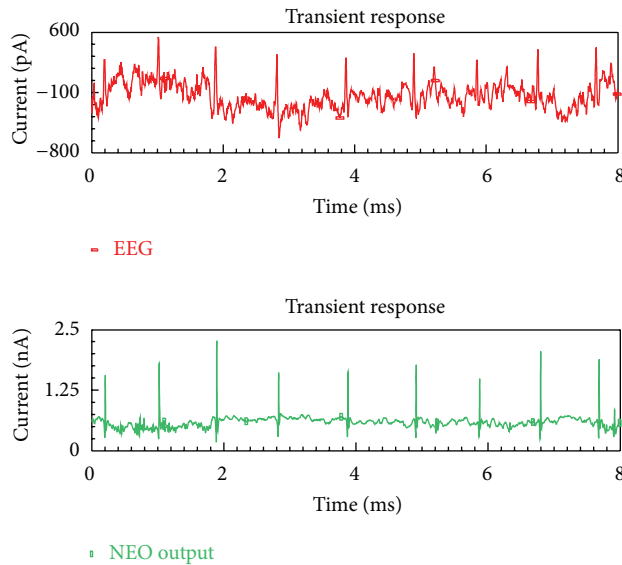


FIGURE 13: Input and output waveforms of the proposed Sinh-Domain NEO realization.

are capable of operating in a 0.5 V power supply voltage, which is the minimum among the topologies under consideration, it is concluded that they simultaneously offer the benefits of both reduced power consumption and power supply voltage. On the other hand, the proposed topologies have the drawback of the increased circuit complexity, and this is originated from the inherent nonlinear internal nature, where there is absence of any small-signal (linear) approximation.

## 5. Conclusion

The proposed companding realizations of NEO are attractive candidates for realizing high-performance biomedical signal processing systems. This is originated from the performed comparison results, where it was proved that they are capable of operating in an ultra-low voltage environment and simultaneously have the minimum power dissipation among the corresponding already published topologies. The Sinh-Domain realization offers more power efficiency compared to its Log-Domain counterpart.

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