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Research Article

High-Efficient Circuits for Ternary Addition

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New ternary adders, which are fundamental components of ternary addition, are presented in this paper. They are on the basis of a logic style which mostly generates binary signals. Therefore, static power dissipation reaches its minimum extent. Extensive different analyses are carried out to examine how efficient the new designs are. For instance, the ternary ripple adder constructed by the proposed ternary half and full adders consumes 2.33 μW less power than the one implemented by the previous adder cells. It is almost twice faster as well. Due to their unique superior characteristics for ternary circuitry, carbon nanotube field-effect transistors are used to form the novel circuits, which are entirely suitable for practical applications.

1. Introduction

On-chip interconnections have become a serious challenge as more and more modules are packed into a chip. They dissipate lots of energy, increase response time, and cause coupling effects by adding more capacitance, resistance, and inductance to a circuit [1]. Multiple-valued logic (MVL) is an alternative solution to interconnect complexity and growing power dissipated by wires [2]. It reduces the amount of wires inside and outside a chip dramatically as more complex designs require a large number of wires for connecting circuit components. In addition, MVL has the high potential for increasing computational speed, reducing switching activity, and implementing many arithmetic and logic functions in a single chip [2, 3]. Among many MVL systems, ternary logic (also known as three-valued logic) has soared in popularity due to its simplicity and efficiency [4, 5].

In spite of potential superiorities of ternary logic, binary is still the dominant logic for circuit design in the industry. One of the main reasons is the intrinsic behaviour of transistors. The on-off characteristic of a transistor makes it an ideal device to implement Boolean algebra. However, dualism does not correspond to real-world applications effectively. Another reason why ternary logic is not as popular as its binary counterpart is mainly because of the lack of sufficient practical, high-performance logic gates and computational components. To make ternary logic applicable in practice, efficient circuits must be developed before all else.

Voltage-mode MVL circuits are based on multithreshold designs [6, 7]. Therefore, traditional metal-oxide-semiconductor field-effect transistor (MOSFET) is not entirely suitable candidate for MVL implementation due to the fact that MOS devices are inherently single-threshold [8]. Since the introduction of new nanoscale devices such as quantum-dot cellular automata (QCA) and carbon nanotube field-effect transistor (CNTFET), many worthwhile endeavours have been made to present novel ternary circuits with high efficiency. The unique characteristic which makes CNTFET technology highly appropriate for ternary circuitry is the ability of adjusting threshold voltage by altering the diameter of CNTs under the gate terminal [9]. The tuneable threshold voltage brings essential flexibility which is a great necessity for ternary designs. Furthermore, CNTFETs operate far faster and even consume less power in comparison with traditional MOS devices [10, 11]. Although commercial CNTFET chips are not ready yet, many valuable achievements have been

made so far. The implementation of CNTFET-based logic gates has been reported in [12, 13]. In addition, the first carbon nanotube computer has been recently developed [14].

A gate-level implementation for ternary half adder (THA) has been presented by Dhande and Ingole [15]. The main drawback is having a very large number of transistors. Lin et al. [16] have replaced some ternary gates with binary ones to reduce transistor count and decrease static power dissipation. Their design has 158 transistors (THA-158T). The final attempt is a NAND-based structure presented by Moaiyeri et al. [17]. In spite of a great reduction, it still needs 112 transistors (THA-112T). A new ternary full adder (TFA) has been presented by Ebrahimi et al. [18]. It is on the basis of two cascaded so-called THAs, in which the output carry is not produced. A carry generator subcircuit produces the final carry from the initial inputs and the output of the first pseudo-THA. The entire block requires 106 transistors (TFA-106T). Another TFA, which directly generates both outputs (Sum and C_{out}) from the input variables, has recently been presented by Keshavarzian and Sarikhani [19]. It needs 132 transistors to form the whole adder cell (TFA-132T).

In this paper, new ternary adders are presented on the basis of a logic style where a large portion is founded upon binary structures. As a result, static power dissipation reaches its minimum extent. The new adder cells operate very rapidly and have a reasonable number of transistors compared with the ones presented in the literature so far. Moreover, they benefit from full-swing operation, capability of working in high frequencies, and strong driving power.

Due to the inaccurate chip fabrication of CNTFET technology, diversity of using CNTs with different diameters decreases the manufacturability issue. Nevertheless, fabrication of multichirality CNTs is inevitable for ternary circuitry due to the fact that ternary circuits are based on multi-V_t designs [6, 7]. The entire novel ternary circuits are developed by CNTs with only three different diameters as it is very common in ternary logic circuitry [16–19]. The proposed designs show low sensitivity to undesired environmental and process variations.

The rest of the paper is organized as follows: Section 2 will express how we are motivated to design new circuits. The proposed ternary adders are presented in Section 3. Section 4 includes simulation results and comparisons. Eventually, Section 5 concludes the paper.

2. Motivation

Implementation of ternary logic is based on an additional voltage level in comparison with binary logic. The voltage level of $V_{\text{dd}}/2$ stands for the logic value "1" in the unbalanced ternary notation [20], whereas zero and V_{dd} voltages represent the logic values of "0" and "2," respectively. Voltage dividers such as resistors [21] or capacitors [22] are used to divide voltage. Current flows through the path established from the power supply to the ground each time voltage division occurs. A significant portion of the total power consumption in ternary circuits is static power. Although the usage of capacitors leads to less power dissipation, they provide weak current drivability.

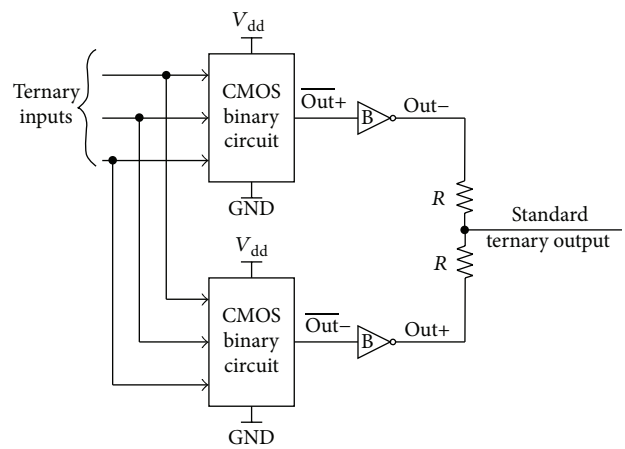

Figure 1: The utilized logic style for implementing new adder cells.

A great advantage of complementary-symmetry metal-oxide-semiconductor (COS-MOS, or CMOS) technology for implementing logic functions is the elimination of continuous static current in binary circuits, due to the fact that either the pull-down or the pull-up network is switched off. This is the reason why some recent works have replaced as many ternary gates as possible with binary ones [16]. A comparison between the average power consumption of THAs presented by Dhande and Ingole [15] and Lin et al. [16] demonstrates that it is more beneficial to use CMOS-based binary circuits as much as possible. The fewer times voltage division takes place, the less power dissipates. In this paper, one of the main targets is to use a logic style in which voltage division occurs as few times as possible so that the static power is reduced to its smallest amount.

The logic style directly influences delay, power consumption, and area characteristics, which are the most important parameters for performance evaluation. There are two definitions of a ternary function other than the standard one. The first (second) interpretation is negative (positive) ternary, denoted by − (+), in which the logic value "1" is replaced with "0" ("2") [23]. Therefore, they are in fact binary functions. Figure 1 illustrates the utilized logic style, which is based upon (1). Positive and negative complementary outputs ($\overline{\text{Out+}}$ and $\overline{\text{Out−}}$) are first generated. Then, binary inverters convert $\overline{\text{Out+}}$ and $\overline{\text{Out−}}$ to Out− and Out+, respectively. Finally, two transistors perform voltage division to generate STOut (1). Therefore, voltage division takes place only once for implementing a ternary function. This logic style is employed in this paper to design new ternary adders.

$$\text{STOut} = \frac{\left(\overline{\overline{\text{Out+}}}\right) + \left(\overline{\overline{\text{Out−}}}\right)}{2} = \frac{(\text{Out−}) + (\text{Out+})}{2}. \quad (1)$$

3. New Single-Bit Ternary Adders

3.1. New Ternary Half Adder. Adder is a fundamental component for all arithmetic operations such as subtraction, multiplication, and division. Half adder is the simplest adder block which performs addition of two input signals. The

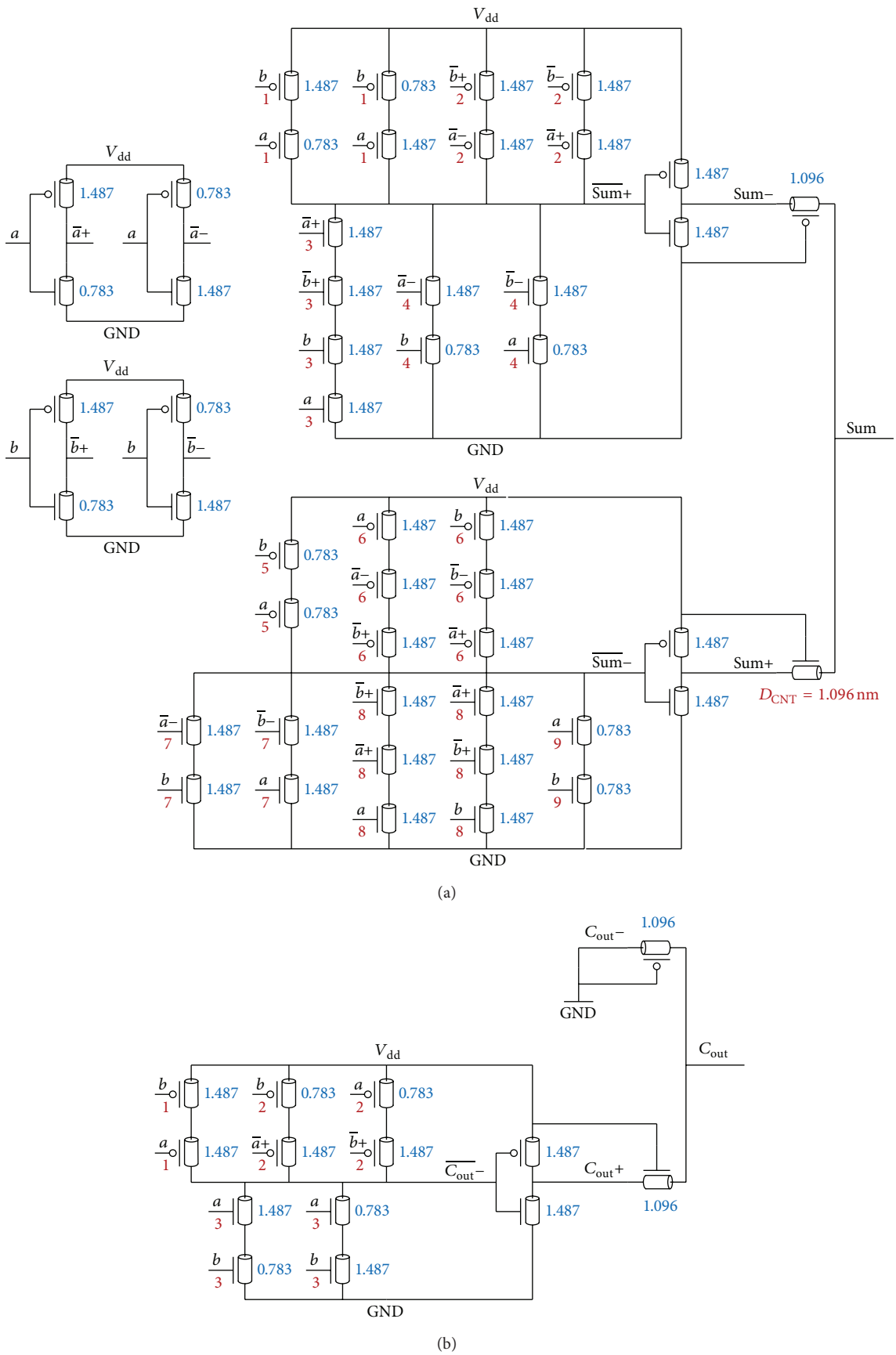

Figure 2: The proposed ternary half adder (#Tube = 3), (a) Sum generator subcircuit, (b) Carry generator subcircuit.

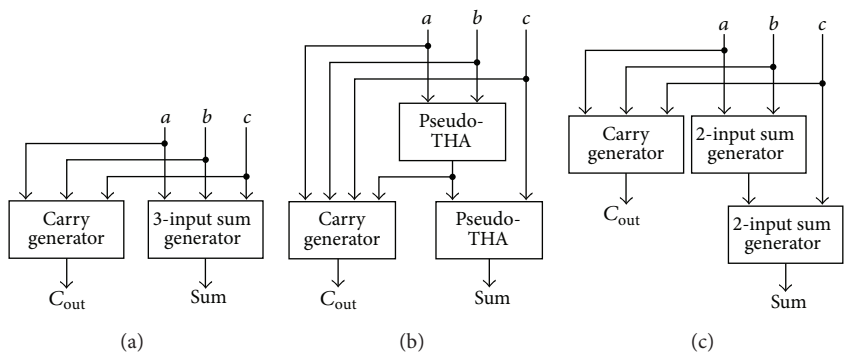

FIGURE 3: Strategies of building a ternary full adder block, (a) the block diagram of TFA presented by Keshavarzian and Sarikhani [19], (b) the block diagram of TFA presented by Ebrahimi et al. [18], and (c) the block diagram of the proposed TFA.

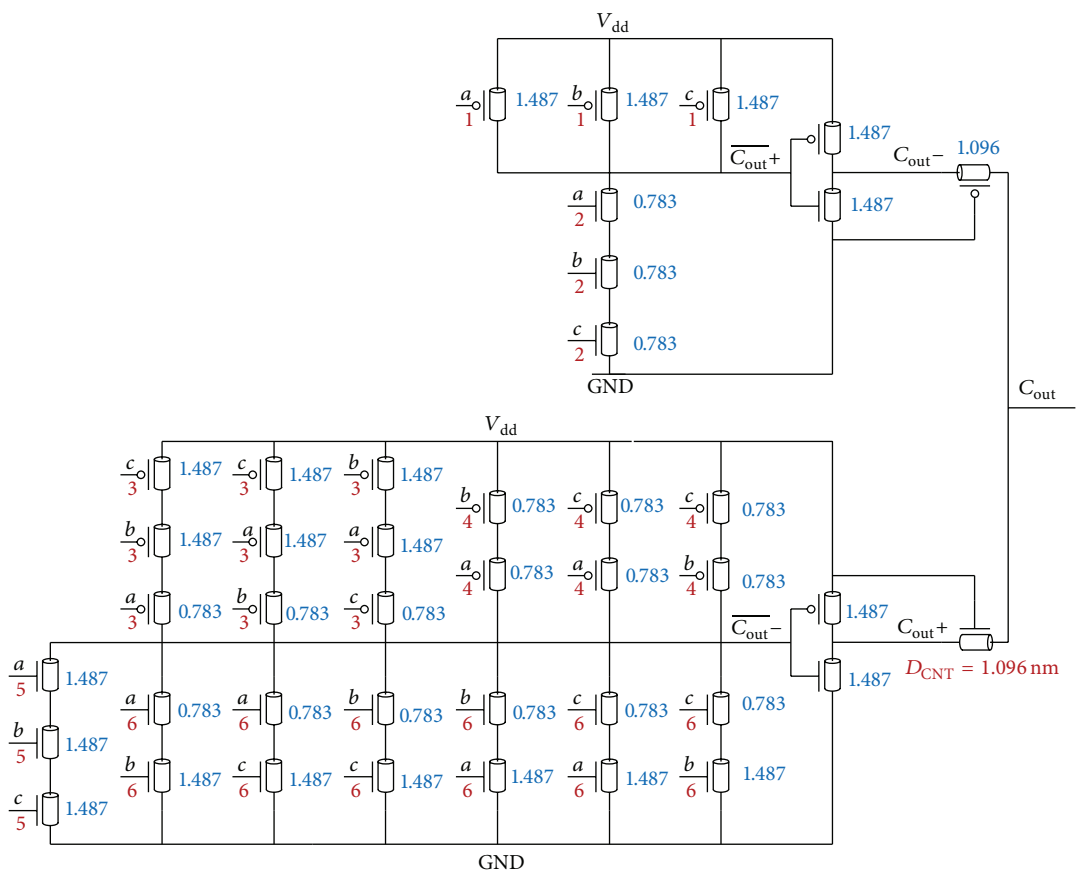

FIGURE 4: The proposed carry generator subcircuit for TFA (#Tube = 3).

proposed ternary half adder is illustrated in Figure 2, in which diameters of CNTs are indicated for each transistor. For CNTFETs with diameters of 1.489 nm, 1.096 nm, and 0.783 nm, the chirality numbers are (19, 0), (14, 0), and (10, 0), and subsequently the threshold voltages are 0.289 V, 0.392 V, and 0.549 V, respectively, ((2), (3)) [24]. The (n_1, n_2) indices are the chirality numbers which indicate wrapping vector along which a sheet of graphite is rolled up to form a carbon nanotube (CNT). These CNTs are used as the channel of the transistor. The diameter of an SWCNT can be as small as 0.4 nm [25]. The typical diameters change between 0.7 nm and 3 nm with mean diameter of 1.7 nm [26].

$$D_{CNT} = 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 \times n_2}, \quad (2)$$

$$V_{th} \approx \frac{0.43}{D_{CNT}\,(\text{nm})}. \quad (3)$$

The final outputs (Sum and C_{out}) are generated in a parallel manner. Two different subcircuits create $\overline{\text{Sum}}$+ and

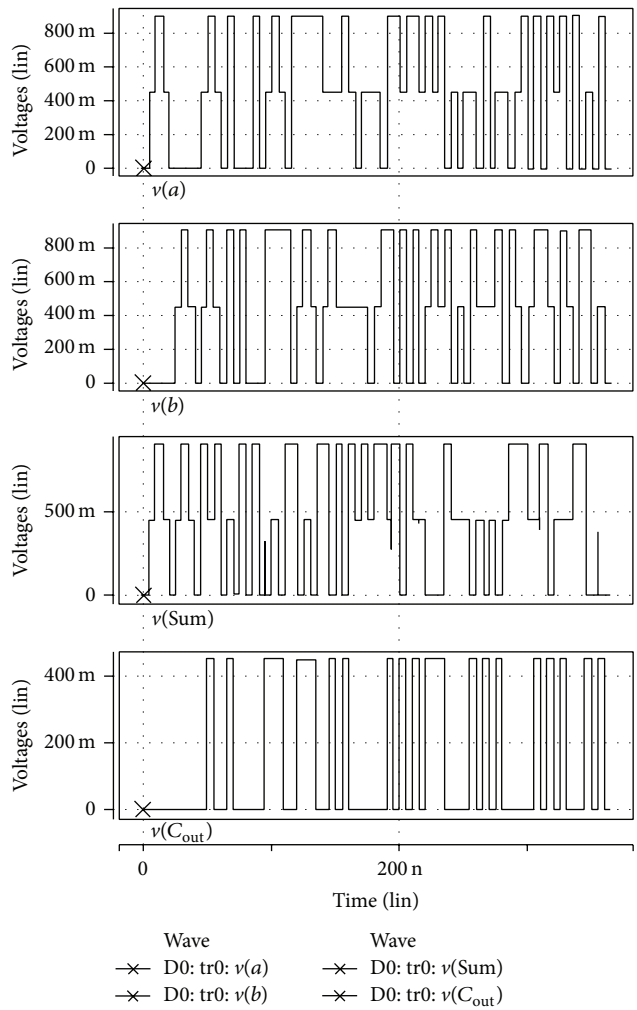

Figure 5: Transient response of the proposed THA.

Table 1: Midoutput values of the Sum generator subcircuit.

a	b	$\overline{a}+$	$\overline{a}-$	$\overline{b}+$	$\overline{b}-$	Sum	$\overline{\text{Sum}}+$	Path(s)	$\overline{\text{Sum}}-$	Path(s)
0	0	2	2	2	2	0	2	**1**	2	**5**
0	1	2	2	2	0	1	2	**1**	0	**7, 8**
0	2	2	2	0	0	2	0	**4**	0	**7**
1	0	2	0	2	2	1	2	**1**	0	**7, 8**
1	1	2	0	2	0	2	0	**3**	0	**8**
1	2	2	0	0	0	0	2	**2**	2	**6**
2	0	0	0	2	2	2	0	**4**	0	**7**
2	1	0	0	2	0	0	2	**2**	2	**6**
2	2	0	0	0	0	1	2	**2**	0	**9**

$\overline{\text{Sum}}-$ (Figure 2(a)) by taking input values shown in Table 1. The first set of transistors, which are marked with "1," connects the node $\overline{\text{Sum}}+$ to the power supply when either $(a, b) = (0, 0)$ or $(a, b) = (0, 1) \mid (1, 0)$, considering input permutations. Two other parallel paths, on which transistors are marked with "2," are supplemented in order to connect the output node to V_{dd} when either $(a, b) = (2, 2)$ or $(a, b) = (1, 2) \mid (2, 1)$. Within the pull-down network, the third path connects the node $\overline{\text{Sum}}+$ to the ground whenever $(a, b) = (1, 1)$. Finally, the fourth set of transistors is switched on when

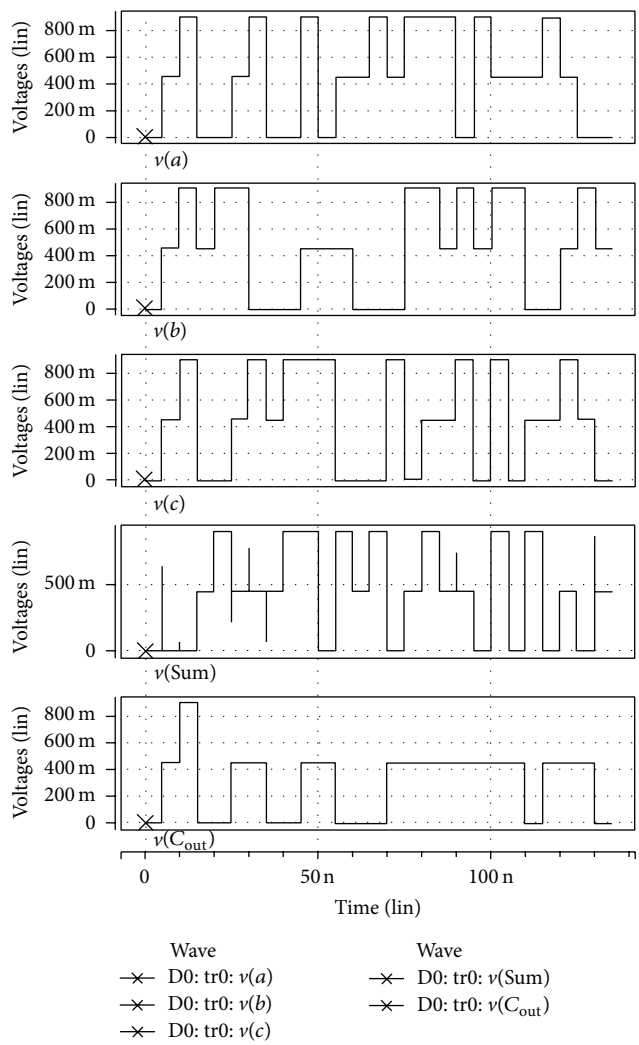

Figure 6: Transient response of the proposed TFA.

Table 2: Midoutput values of the carry generator subcircuit for THA.

a	b	$\overline{a}+$	$\overline{a}-$	$\overline{b}+$	$\overline{b}-$	C_{out}	$C_{out}-$	$\overline{C_{out}}-$	Path(s)
0	0	2	2	2	2	0	0	2	**1**
0	1	2	2	2	0	0	0	2	**1**
0	2	2	2	0	0	0	0	2	**2**
1	0	2	0	2	2	0	0	2	**1**
1	1	2	0	2	0	0	0	2	**1**
1	2	2	0	0	0	1	0	0	**3**
2	0	0	0	2	2	0	0	2	**2**
2	1	0	0	2	0	1	0	0	**3**
2	2	0	0	0	0	1	0	0	**3**

$(a, b) = (0, 2) \mid (2, 0)$. Table 1 summarizes the way paths connect the nodes $\overline{\text{Sum}}+$ and $\overline{\text{Sum}}-$ to the appropriate voltage source, in light of different input patterns.

The same concept leads us to the output carry generator subcircuit (Figure 2(b)). Table 2 shows which transistors set up the proper path to connect the midoutput $\overline{C_{out}}-$ to the proper voltage source. $C_{out}-$ is always "0." Therefore, it is constantly connected to GND. PT and NT inverters (PTI and NTI) are also required to produce $\overline{a} + /\overline{b}+$ and $\overline{a} - /\overline{b}-$, respectively (Figure 2(a)). The entire block has 64 transistors, and it is mostly composed of binary parts, in which either the pull-down or pull-up network is switched off. Therefore,

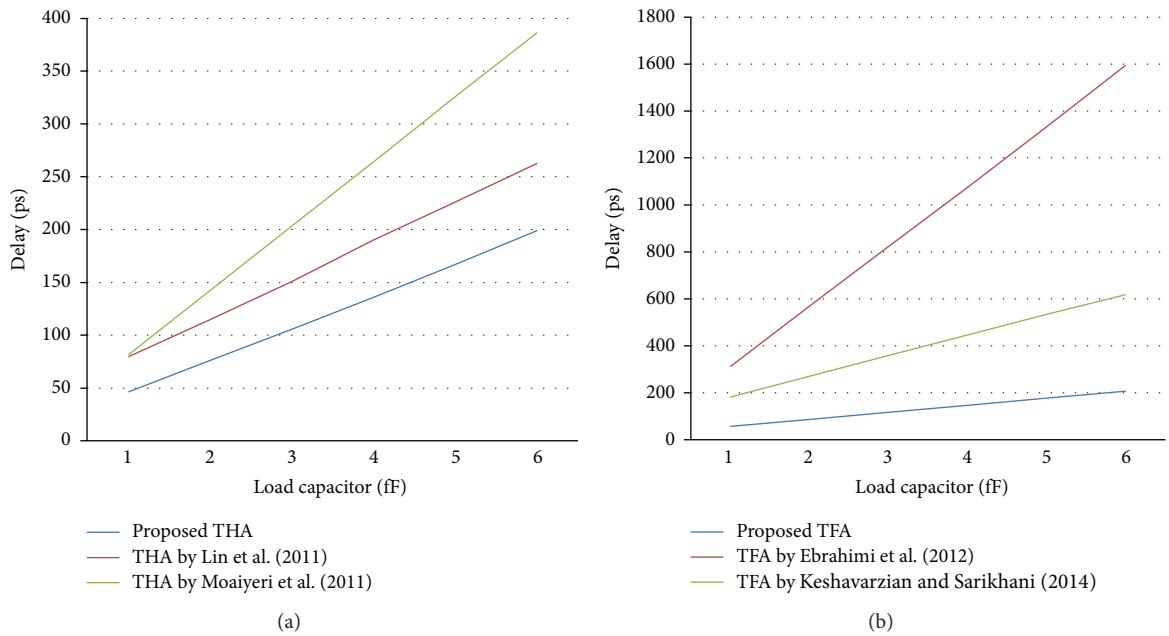

Figure 7: Delay versus load capacitors, (a) THAs, (b) TFAs.

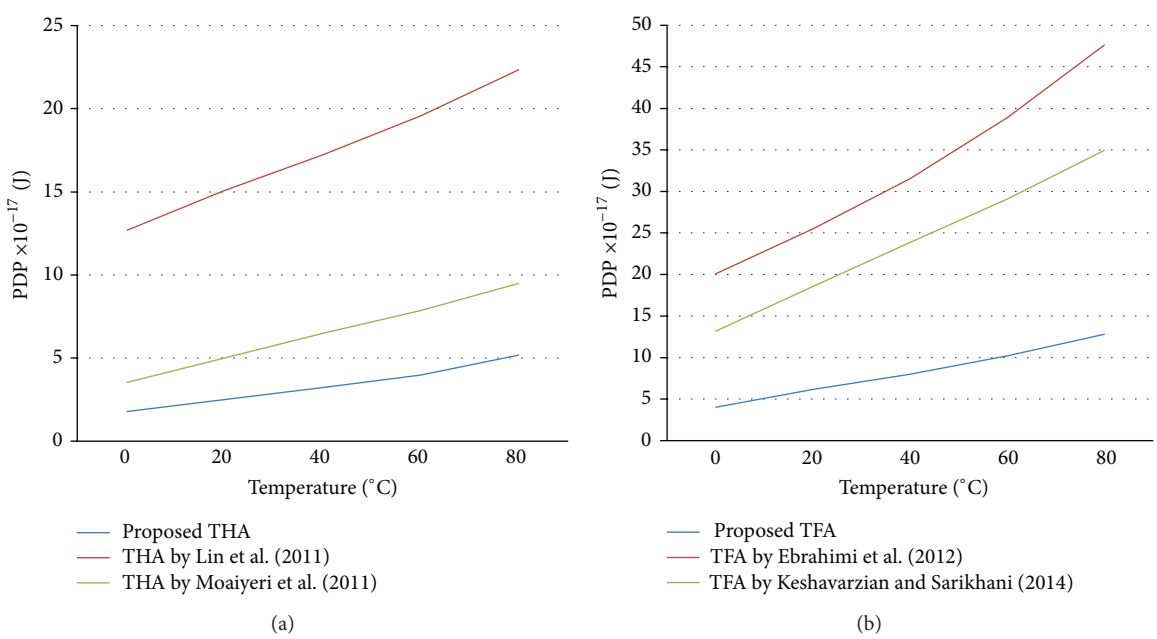

Figure 8: PDP versus temperature variations, (a) THAs, (b) TFAs.

static current does not flow within the subcircuits which generate midoutputs.

3.2. New Ternary Full Adder. Full adder performs addition of three input signals. A ternary full adder, whose block diagram is depicted in Figure 3(a), has been presented by Keshavarzian and Sarikhani [19]. Both outputs (Sum and C_{out}) are directly generated from the input variables. Ebrahimi et al. [18] have proposed another TFA. Figure 3(b) reveals how the final outputs are generated within its block. The output carry is considered as a function of the initial inputs as well as the output of the first pseudo-THA.

The output carry of the proposed TFA is produced directly from the initial inputs (Figure 3(c)). In this manner, output carry is generated far faster, which is a great advantage especially in a ripple adder structure. On the other hand, the proposed Sum generator subcircuit (Figure 2(a)) is cascaded twice to create the final output Sum. The direct approach of generating the output Sum requires multiple pass-transistors in series, which cause slow operation. This is the reason

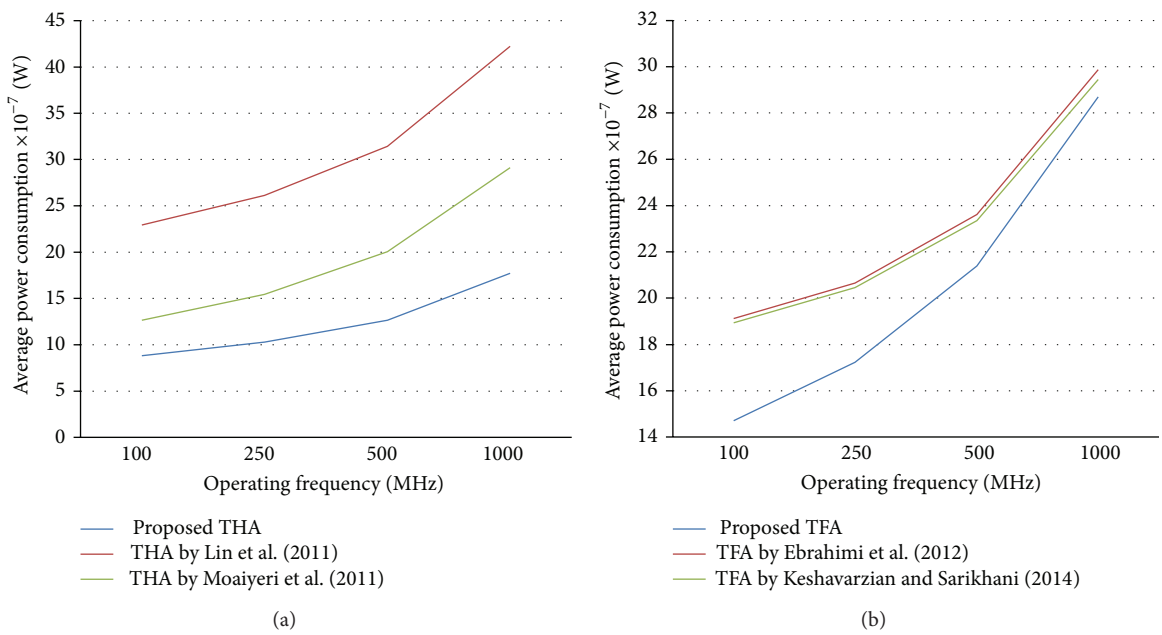

Figure 9: Average power consumption versus operating frequencies, (a) THAs, (b) TFAs.

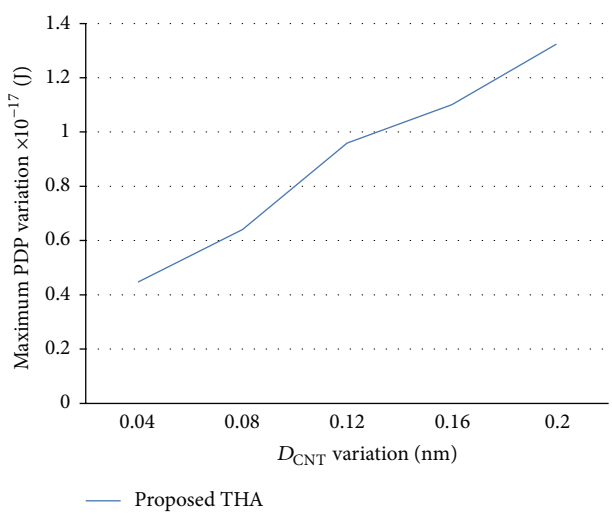

Figure 10: Maximum PDP variation versus D_{CNT} variation.

why Keshavarzian and Sarikhani [19] supplement a ternary buffer in order to rectify the drawback to some extent. Unlike the output Sum, C_{out} is a simple function, which is entirely appropriate to be implemented directly from the initial inputs.

The proposed carry generator subcircuit for TFA is shown in Figure 4. Table 3 shows how transistors connect the midoutputs $\overline{C_{out}}+$ and $\overline{C_{out}}-$ to the proper voltage source depending on what input pattern is considered (Table 3, Second Column), regardless of its permutations. Two-input Sum generator subcircuits (Figure 2(a)) are cascaded in series to create the output Sum (Figure 3(c)). Although it is also possible to obtain the final output Sum directly from the initial inputs, the number of pass-transistors in series increases inside the body of the subcircuit, and hence it leads to deficient overall performance. As a result, cascaded Sum generators are preferable. The entire full adder cell has 142 transistors.

4. Simulation Results

High-performance and state-of-the-art CNTFET-based designs are selected for comparison. Extensive simulation setups are taken into account to examine new adder cells in several aspects. All circuits are simulated with Synopsys HSPICE and 32 nm CNTFET technology [27, 28] in three power supply voltages (1 V, 0.9 V, and 0.8 V) at room temperature. This compact SPICE model includes all

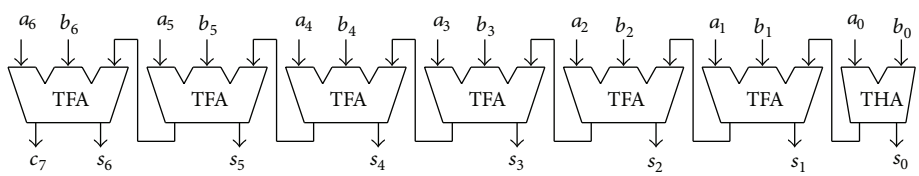

Figure 11: A 7-TIT ternary ripple adder constructed by a THA and six TFAs.

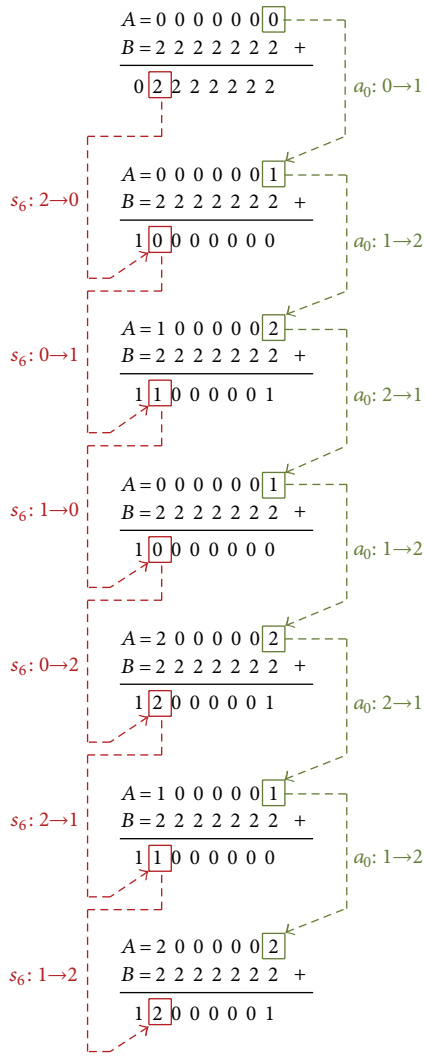

Figure 12: Input patterns which are fed to the ternary ripple adders to measure maximum delay.

nonidealities such as Schottky barrier effects, parasitic Drain/Source/Gate capacitances and resistances, and CNT charge Screening Effects. A brief description of the parameters of the CNTFET model, which has been designed for unipolar MOSFET-like devices with one or more CNTs, is shown in Table 4.

Fan-out of 4 ternary inverters (FO4) was employed as the output load in order to provide a realistic simulation setup. Transient responses of the proposed THA and TFA in 100 MHz operating frequency are plotted in Figures 5 and 6, respectively. Average power consumption during all transitions is also measured. Finally, power-delay product (PDP) is a balance between delay and power factors (4). Simulation results are shown in Table 5. The best results are shown in boldface for better clarification.

$$\mathrm{PDP} = \mathrm{Max}\,(\mathrm{Delay}) \times \mathrm{Avg}\,(\mathrm{Power})\,. \tag{4}$$

There are three nanotubes under the gate terminal of all transistors (#Tubes = 3). Channel length is 32 nm (L_g = 32 nm), and the distance between the centers of two adjacent CNTs under the gate of a transistor is set 20 nm (Pitch = 20 nm). Transistor width of a CNTFET can be approximately

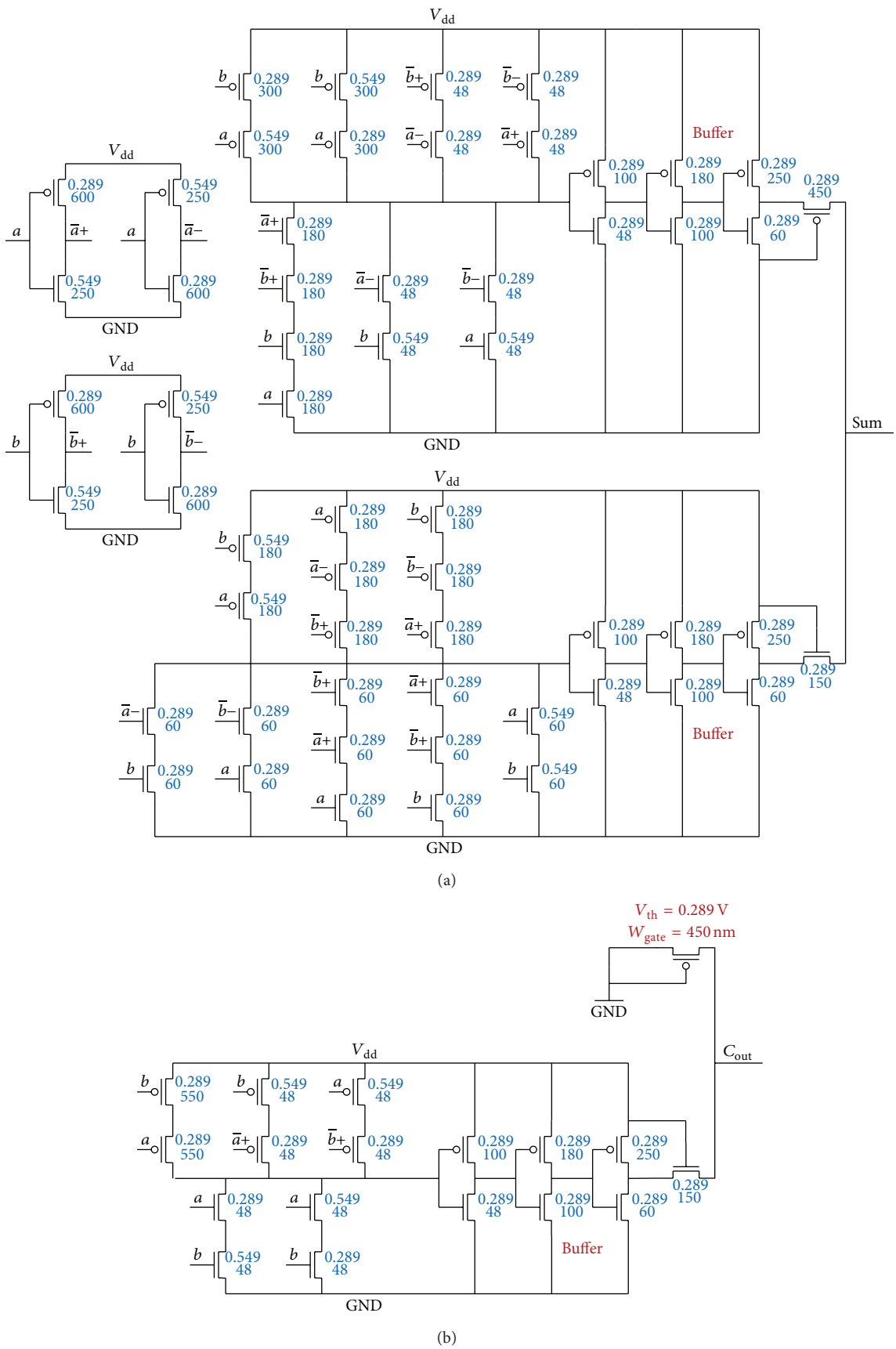

Figure 13: MOSFET implementation of the proposed ternary half adder.

Table 3: Midoutput values of the carry generator subcircuit for TFA.

$\sum$ (Inputs)	Input pattern	C_{out}	$\overline{C_{out}}+$	Path(s)	$\overline{C_{out}}-$	Path(s)
0	(0, 0, 0)	0	2	**1**	2	**3, 4**
1	(0, 0, 1)	0	2	**1**	2	**3, 4**
2	(0, 0, 2)	0	2	**1**	2	**4**
2	(0, 1, 1)	0	2	**1**	2	**3**
3	(0, 1, 2)	1	2	**1**	0	**6**
3	(1, 1, 1)	1	2	**1**	0	**5**
4	(0, 2, 2)	1	2	**1**	0	**6**
4	(1, 1, 2)	1	2	**1**	0	**5, 6**
5	(1, 2, 2)	1	2	**1**	0	**5, 6**
6	(2, 2, 2)	2	0	**2**	0	**5, 6**

Table 4: CNTFET model parameters.

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{dd}/L_{ss}	The length of doped CNT drain/source-side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20 pF/m
Efi	The Fermi level of the doped S/D tube	6 eV

calculated by (5) [29], where W_{min} is the minimum width of the gate. Therefore, by considering this equation, each transistor width is 60 nm. In addition to delay, power, and PDP, total number of transistors and total width of the adder cells (6) are also reported in Table 6 as reasonable criteria of area competence.

$$W_{gate} \approx \text{Max}\left(W_{min}, \#\text{Tubes} \times \text{Pitch}\right), \quad (5)$$

$$\text{Total Cell Width} = \sum_i \text{Width}\left(T_i\right). \quad (6)$$

Simulation results demonstrate the absolute superiority of the proposed circuits. The new designs consume the least power due to their unique structure which is mainly composed of binary parts. For example, the given THA consumes 1.411 μW and 0.384 μW less power in 0.9 V power supply than the designs presented by Lin et al. [16] and Moaiyeri et al. [17], respectively. Voltage division occurs only twice to create the final outputs (Sum and C_{out}), whereas it happens several times in each ternary component of previous THAs. In addition, the performance of the proposed THA is approximately twice higher than the design introduced in [17], while it has also 48 fewer transistors. Moreover, previous ternary half adders require a $V_{dd}/2$ voltage reference. It causes additional on-chip interconnection, which is in contrast with initial MVL targets. The logic style utilized in this paper eliminates the requirement of any extra voltage source.

It takes four successive pass-transistors to charge or discharge the output nodes of the design given by Ebrahimi et al. [18]. It causes poor driving power especially when the circuit faces long wires or high load capacitors. As a result, it operates very slowly. In the proposed structures, the binary inverters situated in the middle isolate CMOS binary circuits from load capacitors, and they bring sufficient driving power for charging and discharging output loads. This is exactly what the ternary buffer in TFA-132T does. In spite of six pass-transistors in series, it operates faster than TFA presented in [18]. To examine driving capability more accurately, capacitors ranged from 1 fF up to 6 fF are applied as output loads. The results of this experiment are plotted in Figure 7. Delay parameter does not increase sharply as output capacitors enlarge, and the new structures operate efficiently despite the existence of large load capacitors.

In addition, the output value of the first pseudo-THA has to be generated first in TFA-106T to produce the output carry. The same output is only generated from the initial inputs in the new design. Therefore, it gets ready 76% faster than in the structure presented in [18]. The delay of the output carry for the given TFA in 0.9 V power supply is 22.192 psec, while the same parameter is 94.942 psec for the previous design.

To observe how temperature variation affects the performance of the proposed circuits, simulations are repeated with different ambient temperatures ranged from 0°C to 80°C. The result of this experiment is depicted in Figure 8. The performance of the proposed designs does not alter sharply in the presence of temperature fluctuations.

Since static power is a large fraction of average power consumption in ternary circuits, it is also measured separately for all designs. To measure static power dissipation, static (DC) input signals are applied to the circuits so that switching activity does not occur. This measurement must be repeated nine times for different input patterns of a 2-input ternary function (THA). It has to be repeated $3^3 = 27$ times if

Table 5: Simulation results of one-digit adders.

Design	V_{dd} = 0.8 V			V_{dd} = 0.9 V			V_{dd} = 1 V		
	Delay (psec)	Power (μW)	PDP (aJ)	Delay (psec)	Power (μW)	PDP (aJ)	Delay (psec)	Power (μW)	PDP (aJ)
					Ternary half adder				
Proposed THA	**38.74**	**0.282**	**10.94**	**28.42**	**0.880**	**25.01**	**25.43**	**2.778**	**70.66**
THA by Lin et al. [16]	91.40	0.771	70.43	66.64	2.291	152.7	54.03	5.817	314.3
THA by Moaiyeri et al. [17]	50.35	0.415	20.88	39.49	1.264	49.91	35.08	3.806	133.5
					Ternary full adder				
Proposed TFA	**58.94**	**0.456**	**26.89**	**43.95**	**1.472**	**64.68**	**35.66**	**4.595**	**163.9**
TFA by Ebrahimi et al. [18]	189.5	0.597	113.1	139.4	1.893	263.9	116.8	5.463	638.3
TFA by Keshavarzian and Sarikhani [19]	119.2	0.607	72.32	102.4	1.912	195.9	81.98	5.413	443.8

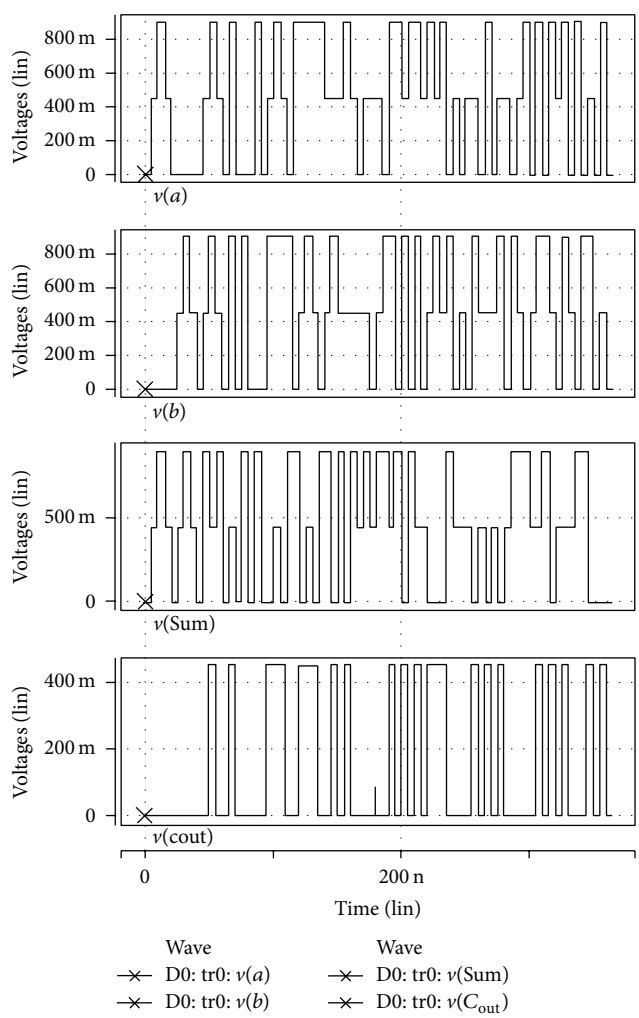

Figure 14: Transient response of the proposed THA with MOSFET technology.

Table 6: Area comparison.

Design	#Transistors	Total cell width (nm)
	Ternary half adder	
Proposed THA	**64**	**3840**
THA by Lin et al. [16]	158	9480
THA by Moaiyeri et al. [17]	112	6720
	Ternary full adder	
Proposed TFA	142	8520
TFA by Ebrahimi et al. [18]	**106**	**6360**
TFA by Keshavarzian and Sarikhani [19]	132	7920

a ternary function has three input variables (TFA). The average and the maximum static powers are reported in Table 7. Static power dissipation reaches its minimum extent in the proposed designs due to their unique structure which is mostly composed of binary parts. For instance, voltage division occurs only twice for the presented THA when all of the input variables equal "2," whereas it happens six times and four times in THA-158T and THA-112T, respectively.

Capability of working in high frequencies is put into practice for the proposed structures as well. Figure 9 shows how sharply power increases by the increase of operating frequency from 100 MHz to 1 GHz. The new circuits operate efficiently in high frequencies, and they consume less power than previous designs.

One of the challenges in CNTFET fabrication is that the diameter of carbon nanotubes cannot be set very precisely. D_{CNT} varies with a standard deviation from 0.04 nm to 0.2 nm for each mean diameter value [30]. To observe how tolerant the proposed designs are against process variation, Monte Carlo transient analysis is taken into consideration.

Table 7: Static power comparison.

Design	Average static power $\times 10^{-7}$ (W)	Maximum static power $\times 10^{-7}$ (W)
	Ternary half adder	
Proposed THA	**5.2661**	**11.058**
THA by Lin et al. [16]	16.540	49.030
THA by Moaiyeri et al. [17]	6.4400	18.767
	Ternary full adder	
Proposed TFA	**6.4724**	**13.829**
TFA by Ebrahimi et al. [18]	10.897	21.250
TFA by Keshavarzian and Sarikhani [19]	11.290	26.604

Table 8: Simulation results of 7-TIT ternary ripple adders.

Design	Delay (psec)	Power (μW)	PDP (fJ)	#Transistors	Total width (nm)
Ripple adder by the proposed THA and TFA	**187.84**	**7.5778**	**1.4234**	916	54960
Ripple adder by THA-112T and THF-132T	371.84	9.9079	3.6841	**904**	**54240**

This analysis is performed with a reasonable number of 30 iterations, in which the simulation is repeated 10 times and the largest deviation is reported. The statistical significance of 30 iterations is quite high. There is a 99% probability that over 80% of all possible component values operate properly if a circuit operates correctly for all of the 30 iterations [31]. Distribution of the diameter is assumed as Gaussian with 6-sigma distribution, which is a reasonable assumption for large number of fabricated CNTs [32]. The results of this experiment are shown in Figure 10 for the proposed ternary half adder, which is highly robust and tolerant against process variation.

Single-bit adder cells are used to form larger adders. In order to test the practicability of the new designs in a large circuit, a seven-Ternary digIT (7-TIT) ripple adder is constructed by combining a THA and six TFAs (Figure 11). THA-112T and TFA-132T are also put together to form another ternary ripple adder for comparison.

To measure worst-case delay, different input patterns are fed to the adder blocks (Figure 12) in a way that a transition propagates from the input of the first stage (a_0) to the outputs of the last stage (s_6). This input pattern is designed in a way it causes all possible transitions in the output Sum of the last stage (s_6). A long duration of iterative input pattern is also fed to the adder blocks to measure average power consumption. Simulation results are reported in Table 8. Although the proposed ripple adder has a few more transistors, it consumes less power and it operates far faster than the structure built by the previous adder cells.

Eventually, to provide a comparison between MOSFET and CNTFET technologies, the proposed ternary half adder is also implemented with 32 nm channel length bulk CMOS [33]. A brief description of the parameters of this model is shown in Table 9. The MOSFET implementation of the proposed THA is illustrated in Figure 13. Each transistor is marked with a pair of numbers. The upper number indicates threshold voltage and the lower number is the width of the transistor (W_{gate}). Due to weaker on-current driving capability of bulk CMOS technology [34], buffers are supplemented, after the midoutputs are generated, to strengthen output signals. Driving power in MOSFETs is 3-4 times weaker than CNTFETs [35]. Therefore, transistor widths are also extended enough to overcome this deficiency, paying the price of enlarging area. Transient response of this adder cell is plotted in Figure 14. The whole cell is simulated under the same conditions as mentioned before for the CNTFET-based THAs. Table 10 shows the simulation results of both technologies. They demonstrate the fact that CNTFETs are absolutely more promising candidates for ternary circuitry. The CNTFET-based THA operates 44 times faster, consumes approximately 10 times less power, and occupies 3.3 times less area than its MOSFET counterpart.

5. Conclusions

New ternary adders have been proposed in this paper based on a logic style which is mostly composed of binary parts. Therefore, static power consumption reaches its minimum amount. Extensive different analyses have been carried out to examine efficiency in all aspects. The proposed designs benefit from low power consumption, high driving power, full-swing operation, and capability of working in low voltages and high frequencies. They can be used in larger circuits and practical environments.

A comparison between MOSFET and CNTFET has been also provided to conclude the superior technology for ternary circuitry. Due to more flexibility of adjusting the desired threshold voltage and high on-current driving capability, CNTFETs are definitely more promising devices for implementing ternary circuits in the future. Simulation

Table 9: Bulk CMOS model parameters.

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
L_{eff}	The effective gate channel length	12.6 nm
R_{dsw}	The source and drain resistance per unit channel width	150 Ω-μm
T_{ox}	The gate oxide thickness	1 nm
C_{gbo}	The gate-to-bulk overlap capacitance per unit channel length	25.6 pF/m
C_{gdl}/C_{gsl}	The overlap capacitance between gate and lightly doped drain/source region	265.3 pF/m

Table 10: Simulation results of the new THA with MOSFET and CNTFET technologies.

Design	Delay (psec)	Power (μW)	PDP (fJ)	#Transistors	Total width (nm)
The proposed THA with MOSFET technology	1248	8.257	10.30	76	12762
The proposed THA with CNTFET technology	**28.42**	**0.880**	**0.025**	**64**	**3840**

results confirm that a CNTFET-based ternary design surpasses MOSFET implementation in terms of speed, power consumption, and area.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References

[1] H. O. Ron, K. W. Mai, and A. Fellow, "The future of wires," *Proceedings of the IEEE*, vol. 89, no. 4, pp. 490–504, 2001.

[2] E. Özer, R. Sendag, and D. Gregg, "Multiple-valued logic buses for reducing bus energy in low-power systems," *IEE Proceedings: Computers and Digital Techniques*, vol. 153, no. 4, pp. 270–282, 2006.

[3] E. Dubrova, "Multiple-valued logic in VLSI: challenges and opportunities," in *Proceedings of the NORCHIP '99 Conference*, pp. 340–349, 1999.

[4] B. Hayes, "Third base," *American Scientist*, vol. 89, pp. 490–494, 2001.

[5] S. L. Hurst, "Multiple-valued logic—its status and its future," *IEEE Transactions on Computers*, vol. 33, no. 12, pp. 1160–1179, 1984.

[6] Y.-B. Kim, "Integrated circuit design based on carbon nanotube field effect transistor," *Transactions on Electrical and Electronic Materials*, vol. 12, no. 5, pp. 175–188, 2011.

[7] Y. Yasuda, Y. Tokuda, S. Zaima, K. Pak, T. Nakamura, and A. Yoshida, "Realization of quaternary logic circuits by n-channel MOS devices," *IEEE Journal of Solid-State Circuits*, vol. 21, no. 1, pp. 162–168, 1986.

[8] H. Inokawa, A. Fujiwara, and Y. Takahashi, "A multiple-valued logic with merged single-electron and MOS transistors," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM '01)*, pp. 7.2.1–7.2.4, December 2001.

[9] S. Lin, Y.-B. Kim, and F. Lombardi, "A novel CNTFET-based ternary logic gate design," in *Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS '09)*, pp. 435–438, Cancun, Mexico, August 2009.

[10] J. Appenzeller, "Carbon nanotubes for high-performance electronics: progress and prospect," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 201–211, 2008.

[11] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1853–1864, 2003.

[12] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, "Logic circuits with carbon nanotube transistors," *Science*, vol. 294, no. 5545, pp. 1317–1320, 2001.

[13] V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, "Carbon nanotube inter- and intramolecular logic gates," *Nano Letters*, vol. 1, no. 9, pp. 453–456, 2001.

[14] M. M. Shulaker, G. Hills, N. Patil et al., "Carbon nanotube computer," *Nature*, vol. 501, pp. 526–530, 2013.

[15] A. P. Dhande and V. T. Ingole, "Design & implementation of 2-bit ternary ALU slice," in *Proceedings of the International Conference on IEEE Science of Electronics, Technology of Information and Telecommunication*, pp. 17–21, 2005.

[16] S. Lin, Y.-B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," *IEEE Transactions on Nanotechnology*, vol. 10, no. 2, pp. 217–225, 2011.

[17] M. H. Moaiyeri, A. Doostaregan, and K. Navi, "Design of energy-efficient and robust ternary circuits for nanotechnology," *IET Circuits, Devices and Systems*, vol. 5, no. 4, pp. 285–296, 2011.

[18] S. A. Ebrahimi, P. Keshavarzian, S. Sorouri, and M. Shahsavari, "Low power CNTFET-based ternary full adder cell for nanoelectronics," *International Journal of Soft Computing and Engineering*, vol. 2, pp. 291–295, 2012.

[19] P. Keshavarzian and R. Sarikhani, "A novel CNTFET-based ternary full adder," *Circuits, Systems, and Signal Processing*, vol. 33, no. 3, pp. 665–679, 2014.

[20] J. A. Mol, J. van der Heijden, J. Verduijn, M. Klein, F. Remacle, and S. Rogge, "Balanced ternary addition using a gated silicon nanowire," *Applied Physics Letters*, vol. 99, no. 26, Article ID 263109, 2011.

[21] A. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," *IEEE Transactions on Nanotechnology*, vol. 4, no. 2, pp. 168–179, 2005.

[22] M. H. Moaiyeri, R. F. Mirzaee, A. Doostaregan, K. Navi, and O. Hashemipour, "A universal method for designing low-power

carbon nanotube FET-based multiple-valued logic circuits," *IET Computers and Digital Techniques*, vol. 7, no. 4, pp. 167–181, 2013.

[23] E. Trias, J. Navas, E. S. Ackley, S. Forrest, and M. Hermenegildo, *Negative Ternary Set-Sharing*, vol. 5366 of *Lecture Notes in Computer Science*, 2008.

[24] M. H. Moaiyeri, R. F. Mirzaee, K. Navi, and A. Momeni, "Design and analysis of a high-performance CNFET-based Full Adder," *International Journal of Electronics*, vol. 99, no. 1, pp. 113–130, 2012.

[25] Z. K. Tang, L. Y. Zhang, N. Wang et al., "One-dimensional superconductivity in 0.4 nm single-walled carbon nanotubes," *Proceedings of the Electrochemical Society*, pp. 587–595, 2002.

[26] M. S. Dresselhaus, G. Dresselhaus, and P. Avouris, *Carbon Nanotubes: Synthesis, Structure, Properties, and Applications*, Springer, 2001.

[27] J. Deng, *Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45nm node and carbon nanotube field effect transistors [Ph.D. thesis]*, Stanford University, 2007.

[28] "Stanford University CNFET Model," http://nano.stanford.edu/models.phpwebsite.

[29] Y. B. Kim and Y.-B. Kim, "High speed and low power transceiver design with CNFET and CNT bundle interconnect," in *Proceeding of the 23rd IEEE International SOC Conference (SOCC '10)*, pp. 152–157, Las Vegas, Nev, USA, September 2010.

[30] H. Shahidipour, A. Ahmadi, and K. Maharatna, "Effect of variability in SWCNT-based logic gates," in *Proceedings of the 12th International Symposium on Integrated Circuits (ISIC '09)*, pp. 252–255, December 2009.

[31] S. Lin, Y.-B. Kim, and F. Lombardi, "Design and analysis of a 32 nm PVT tolerant CMOS SRAM cell for low leakage and high stability," *Integration, the VLSI Journal*, vol. 43, no. 2, pp. 176–187, 2010.

[32] K. El Shabrawy, K. Maharatna, D. Bagnall, and B. M. Al-Hashimi, "Modeling SWCNT bandgap and effective mass variation using a Monte Carlo approach," *IEEE Transactions on Nanotechnology*, vol. 9, no. 2, pp. 184–193, 2010.

[33] Predictive Technology Model, http://ptm.asu.edu.

[34] C. García and A. Rubio, "Manufacturing variability analysis in carbon nanotube technology: a comparison with bulk CMOS in 6T SRAM scenario," in *Proceedings of the 14th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS '11)*, pp. 249–254, April 2011.

[35] F. Ali Usmani and M. Hasan, "Carbon nanotube field effect transistors for high performance analog applications: an optimum design approach," *Microelectronics Journal*, vol. 41, no. 7, pp. 395–402, 2010.