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Editorial

Advanced VLSI Architecture Design for Emerging Digital Systems

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With physical feature sizes in VLSI designs decreasing rapidly, existing efficient architecture designs need be reexamined. Advanced VLSI architecture designs are required to further reduce power consumption, compress chip area, and speed up operating frequency for high performance integrated circuits. With time-to-market pressure and rising mask costs in the semiconductor industry, engineering change order (ECO) design methodology plays a main role in advanced chip design. Digital systems such as communication and multimedia applications demand for advanced VLSI architecture design methodologies so that low power consumption, small area overhead, high speed, and low cost can be achieved.

This special issue is dedicated to aspects of VLSI architecture design and their applications. Special interest focuses on emerging digital systems. This special issue contains eight papers that focus on the power minimization design, efficient hardware Trojan detection, low-area Wallace multiplier, gate-level circuit reliability analysis, low power and high speed arithmetic circuits, power effective fractional-N-PLL frequency synthesizer, power-saving architecture for network on chip, and ECO design.

In the paper entitled "*On-chip power minimization using serialization-widening with frequent value encoding*," the authors address the problem of the high-power consumption of the on-chip data buses by exploring a new framework for memory data bus. In particular, serialization-widening (SW) of data bus with frequent value encoding (FVE) is proposed to minimize the power consumption of the on-chip cache data bus.

In the paper entitled "*Efficient hardware trojan detection with differential cascade voltage switch logic*," the authors present to exploit the inherent feature of differential cascade voltage switch logic (DCVSL) to detect hardware trojans (HTs) at runtime. By examining special power characteristics of DCVSL systems upon HT insertion, the authors can detect HTs, even if the HT size is small. Simulation results show that the method achieves up to 100% HT detection rate. The evaluation on ISCAS benchmark circuits shows that the scheme obtains a HT detection rate in the range of 66% to 98%.

In the paper entitled "*Low-Area Wallace multiplier*," the authors propose a reduced-area Wallace multiplier without compromising on the speed of the original Wallace multiplier. The proposed designs are synthesized using Synopsys Design Compiler in 90 nm process technology and achieve the lowest area cost as compared to other tree-based multipliers. The speed of the proposed and reference multipliers is almost the same.

In the paper entitled "*Gate-level circuit reliability analysis: a survey*," the authors provide an overview of some typical methods for reliability analysis with special focus on gate-level circuits that are either large or small, with or without

reconvergent fan-outs. It is intended to help the readers gain an insight into the reliability issues and their complexity as well as optional solutions. Understanding the reliability analysis is also a first step towards advanced circuit designs for improved reliability in the future research.

In the paper entitled "*Performance analysis of modified drain gating techniques for low power and high speed arithmetic circuits*," the authors present several high performance and low power techniques for CMOS circuits. In these design methodologies, drain gating technique and its variations are modified by adding an additional NMOS sleep transistor at the output node. This method helps to achieve faster discharge and thereby provides higher speed. Intensive simulations are performed using Cadence Virtuoso in a 45 nm standard CMOS technology at room temperature with supply voltage of 1.2 V. Comparative analysis of the present circuits with standard CMOS circuits shows smaller propagation delay and lesser power consumption.

In the paper entitled "*Optimization of fractional-N-PLL frequency synthesizer for power effective design*," the authors design a low power fractional-N phase-locked loop (FNPLL) frequency synthesizer for industrial application, which is based on VLSI. The design of FNPLL has been optimized using different VLSI techniques to acquire significant performance in terms of speed with relatively less power consumption.

In the paper entitled "*Design of smart power-saving architecture for network on chip*," the authors present a novel architecture, namely, smart power-saving (SPS), for low power consumption and low area in virtual channels of NoC. Comparing with related works, the new proposed method reduces with 37.31%, 45.79%, and 19.26% on power consumption and reduces with 49.4%, 25.5%, and 14.4% on area, respectively.

Finally, in the paper entitled "*Engineering change orders design using multiple variables linear programming for VLSI design*," the authors present an engineering change orders (ECO) design using multiple variable linear programming for VLSI design. The authors adopt linear programming technique to plan and balance the spare cells and target cells to meet the new specification according to logic transformation. The proposed method solves the related problem of resource for ECO problems and provides a hardware-efficient solution.

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