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Research Article

Finite Element Analysis of System-Level Electronic Packages for Space Applications

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Thermal analysis was required in order to aid in the design and testing of a radiation tolerant computing (RTC) system using a radiation sensor. During development of the system, different test beds were employed in order to characterize the radiation sensor and its supporting electronic systems. The most common preliminary tests are high altitude balloon tests which allow the sensor to experience cosmic radiation at high altitudes, consistent with space flight operations. In this study, finite element analysis (FEA) was used to evaluate primary system architecture, system support structures, and the flight payload in order to determine if the system would survive preliminary and future testing. ANSYS FEA software was used to create thermal models which accurately simulated convective cooling, system heat generation, and solar radiation loading on the exterior of the payload. The results of the models were then used to optimize payload PC board (PCB) design to ensure that the internal electronic systems would be within acceptable operating temperatures.

1. Introduction

Cosmic radiation has several detrimental effects on digital integrated circuits used in space electronics. These effects include high-energy particles passing through the semiconductor material creating an ionized electron-hole pair causing faults in its programming [1, 2]. Hence space flight computers must be additionally hardened against radiation strikes. Heavy duty shielding can often be used to help harden electronics against radiation when weight is not an issue. However, most flight applications require a minimal mass design in order to save fuel and improve overall efficiency and maneuverability. Therefore, thick shielding is not the preferred method of radiation hardening when limiting mass is a concern. In order to develop radiation hardened electronics, our group designed and developed a new radiation tolerant computing (RTC) system that requires less time to repair these electrical systems [3, 4]. The RTC system employs position sensitive radiation sensors to detect the affected areas thereby implementing targeted repair protocols. The sensor detects the potential for single event upsets (SEUs) due to cosmic radiation and feeds the information to a many tiled computing system implemented on a field programmable gate array (FPGA).

In this study, various high altitude test platforms were employed in order to characterize the radiation sensors response to radiation strikes. Each balloon test consisted of a large balloon attached to several test payloads from various projects. The first type of balloon test was the Balloon Outreach, Research, Exploration, and Landscape Imaging System (BOREALIS) test sponsored by the Montana Space Grant Consortium (MSGC). This test consisted of a large atmospheric weather balloon that carried a string of test payloads up to an altitude of just below 100,000 feet. Each BOREALIS flight typically ascends to its maximum altitude at a nearly constant rate of roughly 5 m/s. Once the maximum altitude is reached, the external pressure acting on the weather balloon is reduced so much that it causes the balloon to burst. Once the balloon bursts, string of payloads falls until the air is dense enough to deploy the parachute recovery system. Typically, the total balloon flight time is *around two hours*. The second balloon test used was the NASA/LSU High Altitude Balloon

Student Program (HASP). The HASP test platform carries the test platforms up to a maximum altitude of approximately 36 kilometers or 120,000 feet over a total flight time ranging *between 15 and 20 hours*.

In order to test the RTC system at altitude, a payload had to be designed that would support the system structure and ensure that adequate operating temperatures were maintained throughout the flight in order to prevent mechanical or electrical system failure. To aid in test payload design, multiple finite element analysis (FEA) simulations were performed to help ensure that the RTC system would not thermally fail during the first flight. Since test flight opportunities are limited, it was important to ensure that the design would work the first time. To accurately model the thermal loading experienced in each test flight, the external thermal environment had to be carefully considered. Each flight was subjected to convection cooling as it ascended through coldest portion of the atmosphere. While the atmospheric convection takes away some heat from the payload during ascent, incoming thermal energy due to solar radiation is of a much greater concern. Thus the solar radiation, especially at maximum altitude where the thin atmosphere does not affect the amount of incoming energy, will have to be given full consideration during thermal analysis of the package. In order to limit thermal energy due to incident radiation, the exterior of the payload was made with insulating material coated with a high emissivity, low absorptivity paint. Ambient temperature versus altitude can be seen in Figure 1 according to the NASA Glenn Research Center's Earth atmosphere model [5].

The paper is organized as follows. The Experimental discusses the design and testing of the test payload that includes sensor boards, an FPGA board, and amplifier boards. Electrical functionality of the package under extreme thermal conditions performed in the laboratory is also discussed. The payload was then flown in a high altitude balloon and FPGA package temperature was recorded during the flight. This test data was then used to verify the finite element model developed to simulate heat transfer between the FPGA board and surrounding package materials and environment. Once validated, the model is then used to perform a parametric study to understand the effect of the gap between the copper ground plane of the FPGA board and the corner bushings on the package thermal management system. The outcome of the work will have a profound impact on the exploration research as it gives guidelines for design of test payloads. In addition, the results obtained from the parametric FEA study will give guidelines to future engineers regarding the design of PC boards for application in space electronics.

2. Experimental

2.1. Payload Thermal Testing. Before the radiation tolerant computing (RTC) system could be tested with high altitude balloons, a test payload had to be designed so that the test payload could withstand the environmental conditions during the BOREALIS and HASP flights. As previously discussed, the amount of time the test payload spends in the lower atmosphere is much less than that of the time spent in the upper atmosphere. Therefore, while convection heat transfer would provide some cooling effect to the outside of the payload, it was certainly not as significant as the amount of thermal energy being transferred into the payload due to solar radiation or internal heat generation of the system during operation. In order to ensure that the internal systems would not get too cold during their ascent, cold room tests were performed to simulate the time spent in the cold region of the atmosphere. To perform the test, the test package was placed in the MSU's SubZero Laboratory (http://www.coe.montana.edu/ce/subzero/) and the payload internal temperature was monitored. The test revealed that the internal systems would never reach a temperature below 20°C, which was well above the minimum acceptable operating temperature for FPGAs. These early tests concluded that cooling would not be a concern for the system. Thus, the major concern was due to the solar heating the payload would experience at the maximum test altitudes. The balloon test payload physical structure for the HASP [6] flight designed using SolidWorks computer aided design software is shown in Figure 2.

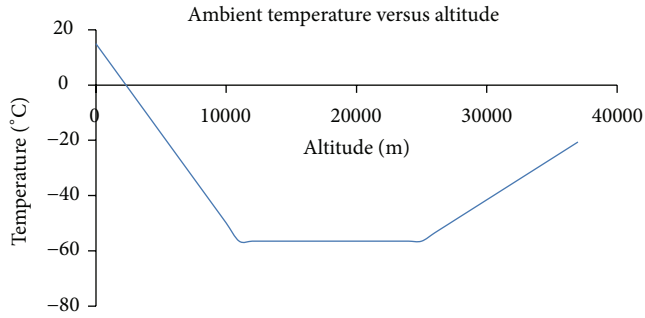

Figure 1: Atmospheric temperature versus altitude.

2.2. High Altitude Balloon Tests. The next step was to test the performance of the developed payload (Figure 2) in actual flight conditions. To do this, the payload was attached to the HASP flight frame and launched. A thermocouple was attached to the FPGA processor in order to record its temperature throughout the HASP flight. The measured device temperature during the flight is shown in Figure 3. It is apparent from the collected data that the FPGA reached a maximum temperature of approximately 50°C or 323 K. The sharp spikes and discontinuities are a result of the signal being dropped during the download of information sets. It is clear from the temperature profile that there is some cooling of the device during the first 200 minutes of data collection as the structure passes through the cold layer of the atmosphere. During the next 340 minutes of data collection when the payload stayed at the maximum altitude, heating of the device is observed (approximately 50°C). It may be mentioned here that once the HASP test frame is launched, it takes around two hours to reach its maximum float altitude. This maximum altitude is reached at a climb rate of about 1000 feet per minute, or 5 m/s. Once maximum altitude was reached, the balloon floated for approximately ten hours while the various other payloads conduct tests. After 18 hours of total flight time, the balloon

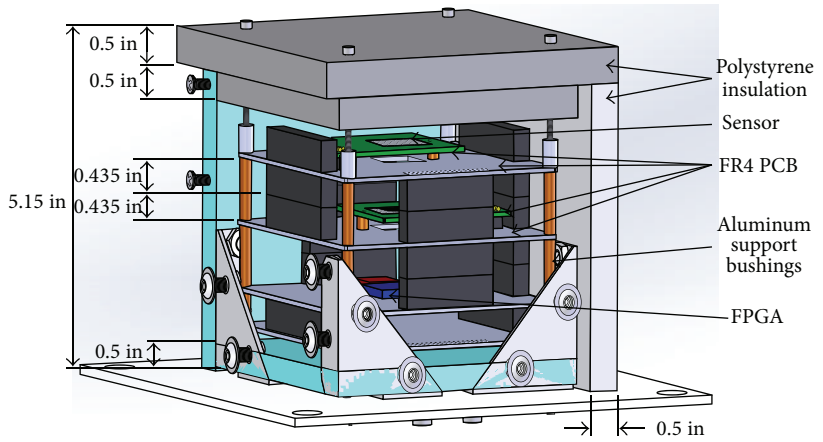

Figure 2: HASP test payload.

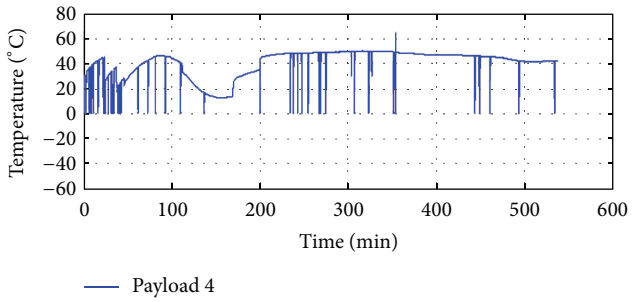

Figure 3: HASP actual temperature versus time data.

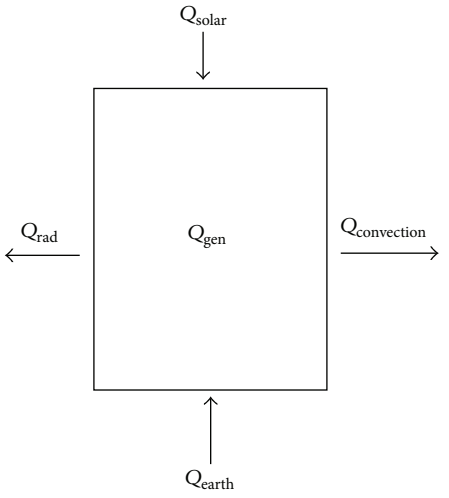

Figure 4: Test payload thermal energy balance.

was released from the flight frame. Then the flight frame freely falls down to around 90,000 feet where the parachute deploys and begins to slow the decent. From there, the entire apparatus floats down to Earth in just under an hour.

3. Finite Element Thermal Analyses

As mentioned earlier, each FPGA device used for the RTC system continuously generates more than 2 W. That, along with the surrounding system architecture, produced a total system generation of approximately 7 W. The payload thermal energy balance at any point of the flight can be seen in Figure 4, where Q denotes thermal energy transfer. While heat is transferred through all of the exterior surfaces of the payload, only the total heat transfer for each mode of transfer is shown in the energy balance figure. Although convection cooling occurred during the relatively short ascent portion of the balloon flights, the long maximum altitude float of the HASP flight is critical from thermal point of view. At maximum altitude, the heat transfer due to convection is completely negligible because of the extremely thin atmosphere. Thus the cooling effect through convection during the majority of the HASP flight is minimal. Also, with little to no atmosphere present, none of the incoming solar energy would be absorbed or reflected, allowing all of the solar radiation to hit the test payload uninhibited.

In order to test for the worst thermal conditions of the HASP flight, the developed FEA model represented only the eight-to-ten-hour float at 120,000 feet. At this altitude, convection heat transfer, both inside and outside the payload, was neglected. In order to apply realistic thermal loads due to solar radiation, the amount of thermal energy incident on the payload first had to be calculated. While Figure 4 shows only one term for thermal energy, Q_{solar}, the actual value of energy differs for each face of the payload. This is due to the orientation, location, and time of day and year that the payload is launched at.

3.1. Solid Modeling. In order to stay within software node and element limits, as well as to reduce solution times, geometry simplification was crucial. All of the fasteners that held the insulation in place were eliminated. The internal RTC system stack was also reduced to include only the circuit boards that produced the most heat. These boards were modeled as a solid volume made entirely of the FR4 material. FR4 is a glass reinforced epoxy material used to make printed

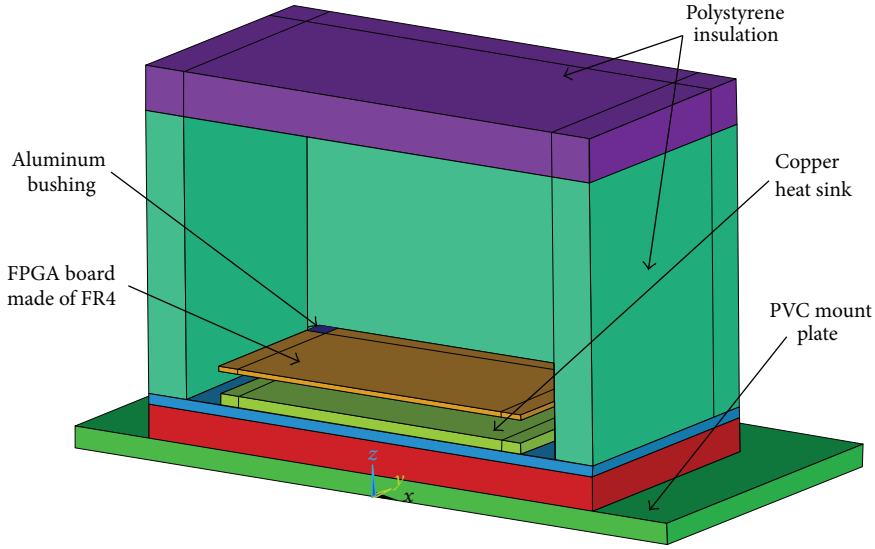

Figure 5: HASP payload model, final configuration.

circuit boards. It consists of fiberglass cloth in an epoxy resin substrate. Most printed circuit boards use copper ground planes in order to more easily ground several electrical components without running individual traces between each component and the ground terminal. The ground plane is usually an extremely thin copper layer that is embedded in the surrounding FR4 material. The surrounding payload structure included the PVC mount plate, a bottom piece of polystyrene insulation on top of that, and the side and top pieces of the polystyrene insulation as seen in Figure 5. Due to symmetries in geometric and loading conditions, only half of the payload was analyzed.

The copper ground plane used underneath the FPGA board was included in the model because, as will be seen later, the ground plane acts as a heat conduction path that allows heat to dissipate more rapidly than through the FR4 material. The copper ground plane for the FPGA board was only $0.0045''$ thick.

The model also included the corner support bushings that went all the way through the insulation. These bushings connect the FPGA board and copper heat sink. While it is difficult to see the bushings in Figure 5, they are more clearly seen as the red volumes in Figure 6. This portion of the geometry is also important as it allows thermal energy to be conducted through the ground plane to the aluminum support and eventually to the exterior of the payload. Once there, the thermal energy could be radiated outward towards the Earth. A copper heat sink was also connected to the corner support bushings directly below the FPGA board. The goal was to direct thermal energy out of the bushings and into the heat sink. It is important to note that while the specific FPGA component and all other electrical components are not shown, their thermal effects were included in the model. Specifically, the FPGA heat generation, which is the major source of heat generation on the PCB, was added as a thermal heat source on the surface of the board.

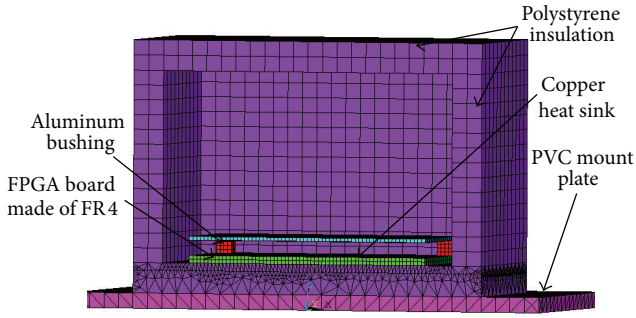

Figure 6: Complete discretized model.

3.2. Element Selection and Meshing. It is mentioned earlier that general purpose finite element software ANSYS [7] was used in this study. Figure 6 shows the complete meshed geometry for the model. Most of the structure was modeled using thermal solid elements called SOLID70. The element allows for three-dimensional thermal conduction [8] and has eight nodes, each with a single degree of freedom that is temperature. Although the lower order SOLID70 element allows the meshing of irregular geometry, it often results in unstable elements being created. This instability is attributed to extreme angles between the edges of narrow degenerate elements along with poor aspect ratios. In order to mesh some of the more complex regions of the geometry, a higher order thermal solid element called SOLID90 was used. These higher order element regions were limited to the internal ground planes in the PCB structure and can be seen as the smallest elements in a later picture. The last element used in the analysis was used to allow for thermal surface effects such as radiation. The element called SURF152 is a two-dimensional element that was applied on the outside faces of the 3D solid thermal elements. This versatile element allowed

Table 1: Relevant thermomechanical material properties.

Material	Thermal conductivity (W/m-K)	Specific heat (J/kg∗K)	Emissivity*	Density (kg/m^3)
FR4	0.27	915	N/A	1820
Polystyrene insulation	0.036	1200	N/A	30
Aluminum	177	875	0.1	2790
White paint	0.000017	N/A	0.99	801
Plastic interconnects	3.976	1500	N/A	1610
Copper	401	385	0.05	8933
PVC plate	0.19	900	0.85	527

*Emissivity not specified for materials with minimal thermal radiation.

for the use of an extra node that was out in space away from the surface element. This extra node was used to set reference temperatures for either radiation or convection effects. This analysis used the extra node for reference temperatures of both space and the Earth's ground. This allowed the top and sides of the test payload to radiate heat out into space and the bottom of the structure to radiate heat back towards Earth.

The very thin copper ground plane presented a problem with regards to meshing. In order to mesh the ground plane accurately, the elements in the copper ground plane had to be very small. The incredibly small thickness of the ground plane meant that a longer horizontal element length would create a very poor aspect ratio for the element. In order to maintain an acceptable aspect ratio, gradient meshing was adopted where a finer mesh size was defined on the ground plane as well as on any other geometries which shares coincident nodes such as the FPGA board and the support bushings. Thermal properties of all the materials used for the model are shown in Table 1.

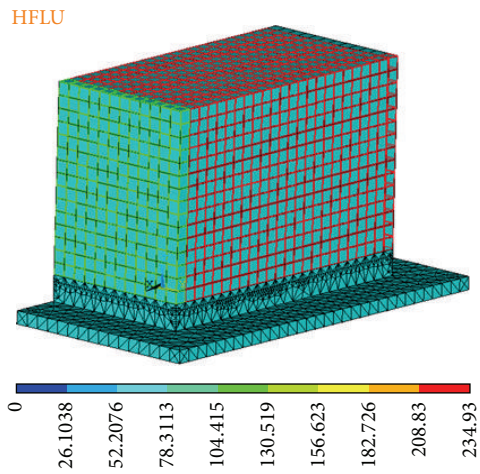

Figure 7: Discretized model showing surface heat flux due to solar radiation as an input.

3.3. Thermal Loading and Boundary Conditions. The first thermal load applied was the internal heat generation of the FPGA board. This was implemented as a body load and was applied to the ground plane in the FPGA board over its volume. As mentioned earlier the amount of generation was varied to understand its effects on chamber thermal management.

The second set of thermal loads applied to the model included the loads due to the incident solar irradiation. These loads were applied to the SURF152 elements as a heat flux. Surface emissivity, absorptivity, and the radiation form factor were all accounted for. The emissivity and absorptivity were controlled as material properties for the thin surface elements. Form factors calculated for the payload were 0.651 for the top face, 0 for the north face, 0.646 for the east face, 0.398 for the south face, and 0 for the west face. Calculations were done using solar angles and times for the date and time when maximum altitude was reached, as well as the launch location in Fort Sumner, NM. This calculation is detailed in the appendix section of [9]. The final form of the model with exterior applied flux loads can be seen in Figure 7. It can be noted here that the surface heat flux values vary as the angles of incidence on different surfaces vary.

3.4. Parametric Study. For future development and testing of the radiation tolerant computing system, the FEA model created in this study was made parametric for any additional alterations to the model geometry, as well as the internal system heat generation. The parameters that were varied were FPGA heat generation and the gap between the copper ground plane and corner bushings. One such alteration was the simple variation of internal heat generation values. While initial studies used the heat generated by a single FPGA processor, different heat generation values were used to see the effect of multiple such processors. It may be mentioned here that bushings are used to keep all the PC boards separated while securing them to the payload structure. In addition, the aluminum bushings help conduct heat from various PC boards to the copper heat sink. Gaps in FR4 PC boards are generally incorporated to ensure electrical isolation while the copper ground plane is needed for circuit design.

Effects of the gap between the copper ground plane and the corner bushings on package thermal managements are important because future PCB designs may include different gaps. The expected result of a gap in the copper material would be an increase in maximum temperature experienced by the system structure. This would be due to the much lower

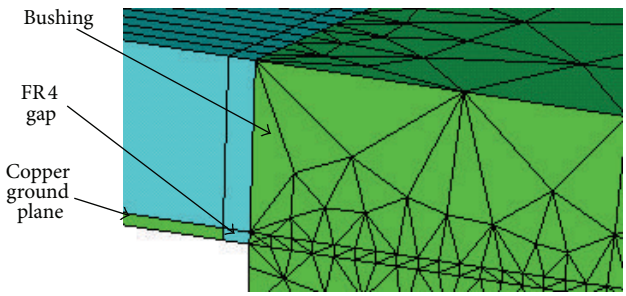

Figure 8: Gap in copper ground plane.

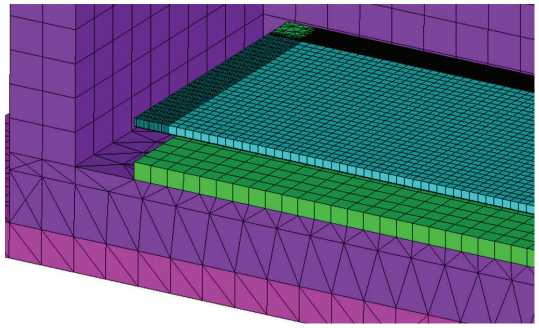

Figure 9: Mesh refinement after gap addition.

thermal conductivity in the FR4 material filling the gap in the copper material. By varying the gap thickness, the effect on the maximum temperature reached in the structure could be tested. The gap width ranged from zero, meaning there was direct contact between the copper ground plane and bushings, to 0.01 inches of FR4 material in between the ground plane and the bushing. The addition of the small gap in the ground plane made further volume subdivision and subsequent mesh density refinement necessary for the model to maintain accuracy while staying under the maximum node count limit of the software. The ground plane gap and the element mesh density can be seen in Figures 8 and 9, respectively.

4. FEA Results and Discussion

4.1. High Altitude Steady State and Transient Analysis. As previously mentioned, the most critical thermal condition that the payload is subjected to is when it is at the maximum altitude because the maximum amount of solar energy would be hitting the payload for up to ten hours. Both a steady state and transient analyses were run at this condition with the same meshing, thermal loading, and boundary conditions as described in previous section. The steady state temperature distribution, in Kelvin, can be seen in Figures 10 and 11 for the entire structure, for the FPGA board and aluminum support bushings, respectively.

It is clear from the temperature contour plots that the maximum temperature of 322.2 K or 49°C was attained in the FPGA board during the long high altitude float of the payload that is within the acceptable temperature range for FPGA.

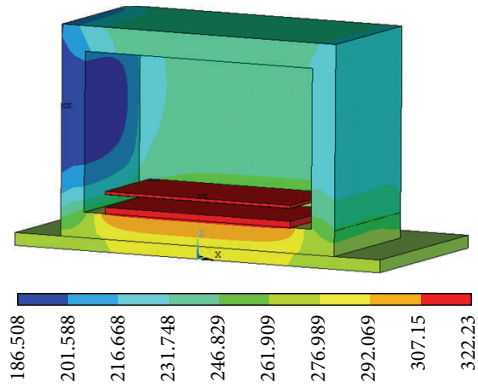

Figure 10: Max altitude steady state temperature results in degrees Kelvin.

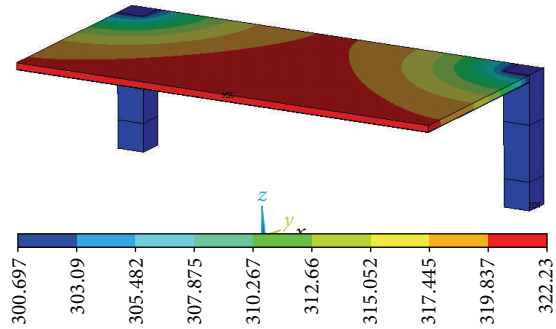

Figure 11: Max altitude steady state temperature distribution in FPGA board in degrees Kelvin.

The use of aluminum support bushings helped with thermal management as the heat will flow from the high temperature FPGA board to bottom heat conductor through the bushings. This is supported by the monotonous thermal gradients. Note the cooler temperature regions radiating outward from the support bushings in Figure 11. Further support of the aluminum bushings directing heat flow out the bottom of the structure can be seen by looking at the temperature distribution of the bottom of the payload as seen in Figure 12. As the copper heat sink is mounted in the central region of the PVC plate, this region exhibits higher temperature than the outer edges due to the increased transfer of thermal energy from the heat sink.

Next, the transient thermal analysis was performed to model the maximum altitude portion of the actual HASP flight as closely as possible. The variation of maximum FPGA board temperature with time of flight is shown in Figure 13. It is clear from the temperature-time plot that the payload attained the steady state condition within 20,000 seconds or 5.5 hours into the flight. The maximum temperature attained at this time is 316.1 K.

Figures 14 and 15 show the temperature distribution after 10 hours in the transient analysis. The package temperature distribution at this point of time is very similar to that of the steady state model which is expected as the payload has

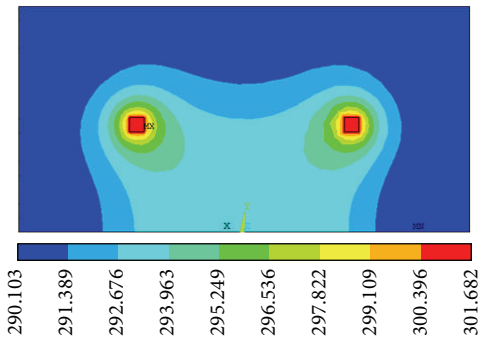

Figure 12: Max altitude steady state temperature distribution in degrees Kelvin, bottom view.

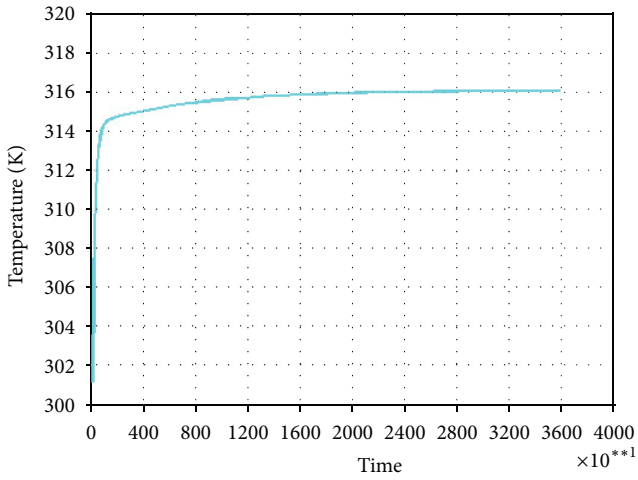

Figure 13: Max temperature [K] versus time [s].

Table 2: Maximum FEA temperature results comparison.

Model	Max temp. [K]	Difference from measured temperature
Steady state	322.23	0.16%
10-hour transient	316.1	1.86%

already reached steady state condition. The maximum temperatures calculated using transient analysis are a little lower than those of the steady state analysis.

The maximum temperatures from the steady state and transient analyses, along with their difference from the actual recorded maximum temperature of 49 deg C (Figure 3), are shown in Table 2. These results show that both maximum altitude thermal models were extremely accurate in predicting maximum temperatures reached in the FPGA structure with an error of less than 1.86% when compared with the recorded data shown in Figure 3. The results of the maximum altitude thermal model are very important in further design optimization of the payload package as they are the only results that could be compared to the measured temperature data.

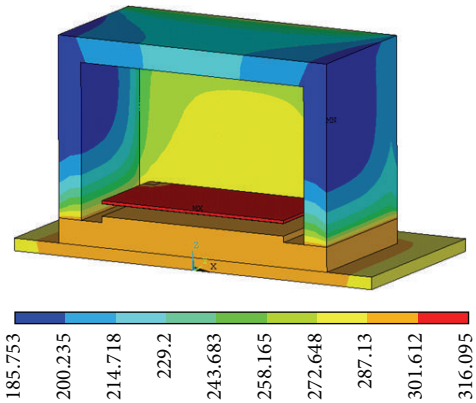

Figure 14: Max altitude 10-hour transient temperature results in degrees Kelvin.

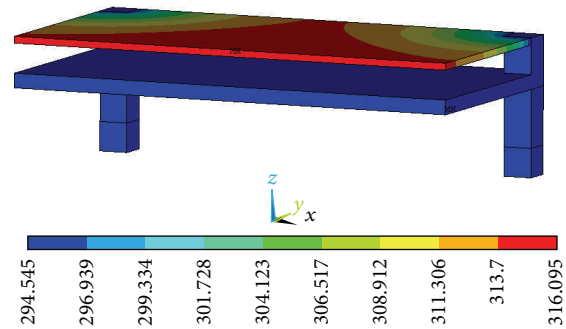

Figure 15: Max altitude 10-hour transient FPGA temperature distribution in degrees Kelvin.

4.2. Parametric Study. As previously described, the internal heat generation and copper ground gap width were varied for the maximum altitude payload analysis. This part of the analysis is important for any future packaging that may involve different number of FPGA parts. The gap between the copper ground plane and the bushings is also important in payload design that can only be achieved based on the manufacturers' tolerance limit. Since the steady state analysis required relatively small run times compared to transient analysis and also predicted the maximum package temperature very accurately, the parametric analyses were performed only using the steady state FEA model.

By changing the internal heat generation from the current value of 1.63 W to a maximum of 6 W, a trend was found between maximum FPGA temperature and the heat generation rate. After running the simulation for each individual heat generation rate, the maximum temperature was plotted showing a linear response between heat input and maximum temperature as seen in Figure 16. By fitting a linear trend line to the data from Figure 16, it was shown that the maximum FPGA temperature went up 22.6 K for each additional watt of heat generation in the steady state, maximum altitude analysis.

As expected, the addition of a gap in the copper ground plane also resulted in an increase in maximum temperature

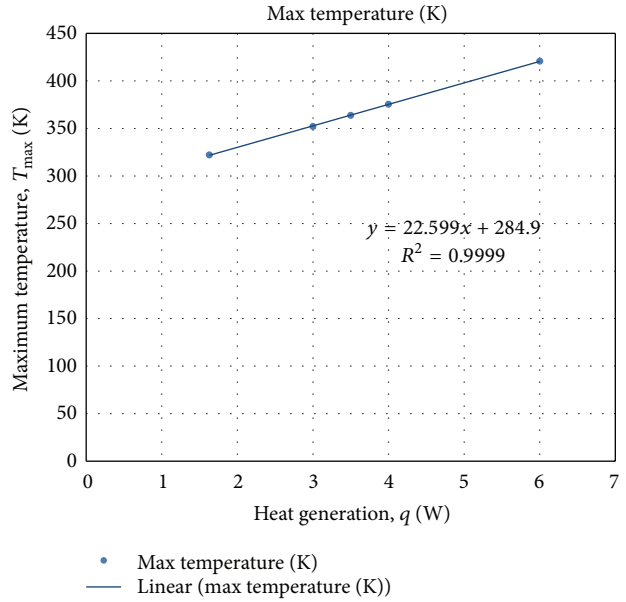

Figure 16: Maximum temperature versus heat generation.

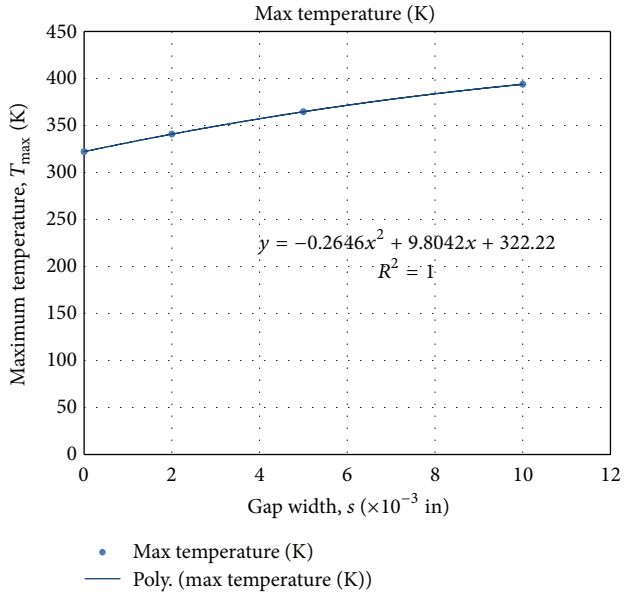

Figure 17: Max temperature versus ground plane gap thickness.

of the FPGA board because the larger the gap the higher the thermal resistance to conduct heat from the copper ground plane and the aluminum bushings (Figure 17). This response was quadratic and can be represented by the following equation:

$$T_{max} = -0.265s^2 + 9.804s + 322.2, \quad (1)$$

where T_{max} is the maximum package temperature in K and s is the gap in mils. The quadratic nature of temperature variation is intuitively correct as the cross section of the gap increases quadratically with gap and the thermal conductance is linear with the cross-sectional area.

The temperature data from this ground plane gap study shows how the copper ground planes help conduct heat out of the FPGA board. While increasing the gap does increase the maximum temperature, the total temperature increase is not as significantly affected by gap distance as it is by an increase in heat generation.

5. Summary

The thermal FEA models used in this study were very useful in predicting accurate maximum temperature results for the high altitude test flights. The use of parametric input code allowed quick and easy adjustments to key features of the model such as insulation thicknesses, material thermal properties, and thermal loading. These features significantly aided in material selection and component design. The results correlating varying system heat generation, ground plane gap distance, and maximum temperature should prove useful in future design configurations of the test platform. While gap distance is not as critical of a factor, system heat generation certainly is. If the system heat generation is increased significantly, the maximum temperature in the FPGA board will soon exceed the allowable operating temperature. In order to counteract this effect, the rate in which heat is conducted away from the generation source will need to be increased. The rate of thermal conduction would be increased by the addition of copper ground planes to the structure, but the ground planes cannot interfere with the electronic systems functionality. In the case of drastic increase to heat generation, a more effective thermal management solution would be to use heat pipes to conduct heat away from the heat generation source to the exterior radiating surfaces of the payload. Careful analysis of the heat pipe would be necessary in order to ensure that enough heat was conducted to the payload exterior. A simple one-dimensional conduction analysis could be performed for any necessary heat pipes to ensure adequate heat conduction rates. The rate at which thermal energy would leave the heat pipe would be dependent on the exterior surface it connects to and how quickly it could radiate heat out to its surroundings. The current maximum altitude FEA models provide a good simulation of how much thermal energy can be radiated back out to Earth or space depending on orientation and external temperatures.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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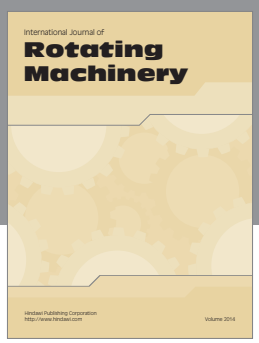

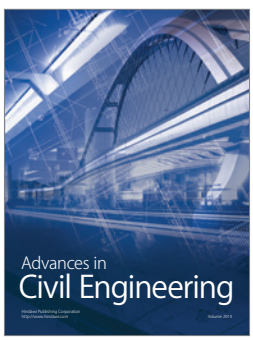

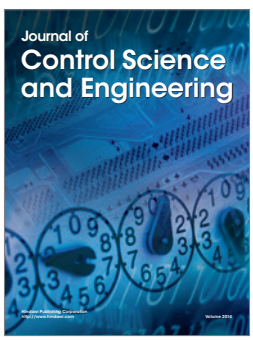

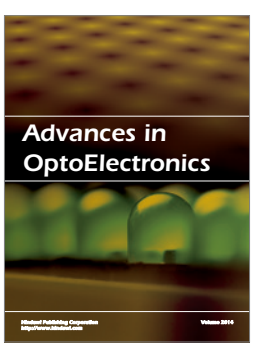

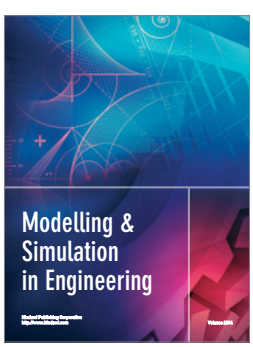

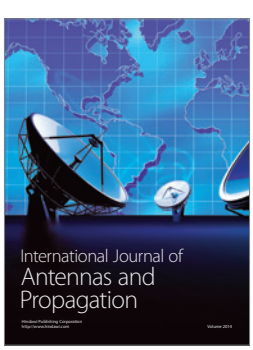

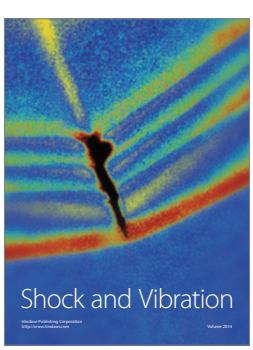

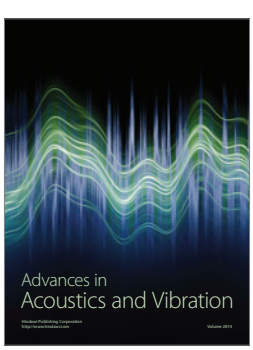

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