Hindawi Publishing Corporation
Journal of Materials
Volume 2016, Article ID 6123268, 7 pages
http://dx.doi.org/10.1155/2016/6123268

Research Article

Investigating Phase Transform Behavior in Indium Selenide Based RAM and Its Validation as a Memory Element

Swapnil Sourav, Amit Krishna Dwivedi, and Aminul Islam

Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand 835215, India

Correspondence should be addressed to Swapnil Sourav; meec1003214@bitmesra.ac.in

Received 30 April 2016; Accepted 17 July 2016

Academic Editor: Te-Hua Fang

Phase transform properties of Indium Selenide (In_2Se_3) based Random Access Memory (RAM) have been explored in this paper. Phase change random access memory (PCRAM) is an attractive solid-state nonvolatile memory that possesses potential to meet various current technology demands of memory design. Already reported PCRAM models are mainly based upon Germanium-Antimony-Tellurium ($Ge_2Sb_2Te_5$ or GST) materials as their prime constituents. However, PCRAM using GST material lacks some important memory attributes required for memory elements such as larger resistance margin between the highly resistive amorphous and highly conductive crystalline states in phase change materials. This paper investigates various electrical and compositional properties of the Indium Selenide (In_2Se_3) material and also draws comparison with its counterpart mainly focusing on phase transform properties. To achieve this goal, a SPICE model of In_2Se_3 based PCRAM model has been reported in this work. The reported model has been also validated to act as a memory cell by associating it with a read/write circuit proposed in this work. Simulation results demonstrate impressive retentivity and low power consumption by requiring a set pulse of 208 μA for a duration of 100 μs to set the PCRAM in crystalline state. Similarly, a reset pulse of 11.7 μA for a duration of 20 ns can set the PCRAM in amorphous state. Modeling of In_2Se_3 based PCRAM has been done in Verilog-A and simulation results have been extensively verified using SPICE simulator.

1. Introduction

With the rapid expansion of modern technologies, researchers have been motivated towards nonvolatile memory elements [1]. Nonvolatile elements such as spin transfer torque (STT) based magnetic tunnel junction (MTJ) and spin valve are promising candidates for nonvolatile Random Access Memory (MRAM) [2–4]. Nonvolatile memory elements are more reliable and convenient to be included in any circuit architecture with a prolonged data holding and retention capabilities as compared to the conventional volatile memory elements [3, 5]. Phase change random access memory (PCRAM) has emerged as a promising candidate to replace the traditional memory circuits [6]. Phase change memory (PCM) technology has made rapid progress in a short time, having demonstrated low power consumption, nonvolatility, and compatibility with the present CMOS technology without having adverse scaling effects. Rapid switching, and prolonged data holding capacity and scalability characteristics of PCRAM match up with various potential applications across the memory-storage hierarchy [1]. PCM has capabilities to meet the requirements of nonvolatile memory design which has its potential applications in almost every electronic gadget used in our day-to-day lives. Before the introduction to such phase change memories, flash memories were playing vital roles in the memory design. However, over the past few years, flash memories have been struggling to meet the technology trends exhibiting unpleasant effects of scaling lateral device dimensions, stress-induced leakage current (SILC), and the cell-to-cell parasitic interference between the stored charges in closely packed cells. These effects are mainly observed due to programming with large voltages across ultrathin oxides. Alternatives to such design have been already proposed typically involving replacement of the floating polysilicon gate by some type of charge-trapping layer, such as the Silicon Nitride at the center of the Silicon-Oxide-Nitride-Oxide-Semiconductor (SONOS). Also, Tantalum Alumina Nitride Oxide Semiconductor (TANOS) based structures have been

proposed to overcome data retention issues in the SONOS designs. TANOS based designs are still immune to device-to-device variations in threshold voltage (V_{th}), shot-noise effects, and random telegraph noise mainly due to the hot electron carriers present in the channel. FinFET flash devices or 3D stacking of flash memory is the possible solution reported for the above problems. However, with the scaled technology, it is still getting difficult to obtain the desired memory attributes with such devices. Maintaining the minimum current level to reduce the power consumption is one of the most concerning design issues to be addressed. PCM technology is one of the possible solutions to handle such requirements with prolonged data storage capacity and ability to retain data even after the power supply is turned off.

PCRAM cell stores data in the form of physical state of the material from which it is developed. The resistance margin offered by PCRAM in its two distinct physical states, that is, amorphous and crystalline states, is used to determine the stored data. Researchers have already proposed solid-state PCRAM with GST (Germanium-Antimony-Tellurium ($Ge_2Sb_2Te_5$)) material [7]. However, next generation memories require better write endurance with minimal read/write current required for changing the phase of the material. Other materials need to be explored to replace the traditionally used GST material in order to boost up the phase change memory performance. Recent developments have reported various other possible materials for the fabrication of phase change RAM including GeTe, In_2Se_3, InSb, SbTe, GaSb, InSbTe, and GaSeTe [8]. Among them, In_2Se_3 has emerged as a potential candidate for the VLSI chip designers due to its wider range of electrical resistivity and higher electrical resistivity offered as compared to compound GST based designs [9]. This work addresses challenges for the phase change technology for In_2Se_3 based PCRAM which include the design of PCM cells for low set/reset current, requirement to control device-to-device variability, and undesirable changes in the phase change material that can be induced during the fabrication processes. Further, issues related to operation of PCM devices, including retention, device-to-device thermal cross talk, endurance, and bias-polarity effects, have been also addressed. Apart from these, several fabrication issues limit the performance of PCRAM. High programming current pulse to generate the thermal energy needed for inducing the phase change, Joule heating induced power dissipation, intercell thermal interference, and scaling difficulties are some issues which require researchers' attention [10]. As the performance of PCRAM depends mainly upon the choice of material used for the design, In_2Se_3 material based PCRAM have been reported as the possible solution to the above-mentioned issues.

In view of the above, this paper makes the following contributions:

(1) Modeling of In_2Se_3 based PCRAM is presented.

(2) The reported model has been validated as a non-volatile memory element.

(3) A read/write circuit that can produce the required amount of current to flip the phase of material is reported.

(4) Finally, comparisons are drawn to strengthen the facts mentioned in this paper.

The rest of the paper is organized as follows. Section 2 presents the comparative study of various other possible fabricating materials for the PCRAM. Description of In_2Se_3 based PCRAM model is reported in Section 3. Validation of In_2Se_3 based PCRAM model as a memory element is presented in Section 4. Simulation results and discussion are mentioned in Section 5. Finally, concluding remarks are made in Section 6.

2. Phase Change Materials for PCRAM

Difference in the resistance value offered by phase change material in its two distinct states, that is, amorphous and crystalline states, is explored to design a phase change memory (PCM). Memory attributes of PCRAM mainly depend upon the choice of phase change material. Among various PCM, Germanium-Antimony-Tellurium ($Ge_2Sb_2Te_5$ or GST) materials are commonly used for designing of PCRAM. However, recently researchers have explored various other PCM such as GeTe, In_2Se_3, InSb, SbTe, GaSb, InSbTe, and GaSeTe, to enhance the performance of the PCRAM. This work is focused towards the modeling of PCRAM using In_2Se_3 as its main constituent.

Nonvolatile memories designed with phase change materials possess various advantages as compared to their CMOS counterpart. Phase change materials offer impressive memory attributes such as high density, bitwise switching, smooth access, and prolonged data storage capacity without any leakage effects and scaling effects [10]. However, PCRAM faces other challenges such as reliability, read/write endurance, thermal cross talk, and bias-polarity effects [11]. To overcome these issues researchers have proposed different techniques to enhance its reliability by engineering with the phase change materials. The resistance margin offered by the phase change material in two distinct states, that is, amorphous and crystalline states, determines various important design attributes.

PCRAM stores data in the form of resistance offered by its two different physical states. Amorphous phase of phase change material offers a high resistance path through it which is termed as "reset state" or logic "0" state. Similarly, crystalline phase of the phase change material offers a low resistance path through it which is termed as "set state" or logic "1" state. Switching between these two states can be easily achieved by passing a required amount of current to configure the phase change material in set/reset state. The value of current required to flip from one state to another depends mainly upon the choice of the phase change material. For instance, PCRAM design with GST material requires a set current (I_{SET}) of 600 μA and a reset current (I_{RESET}) of 1200 μA. As low power consumption is one of the vital parameters for the memory design, researchers are trying to reduce the amount of set/reset current required by the phase change material by exploring other possible phase change materials.

Further, reliability of PCRAM can be improved by choosing phase change materials offering larger margin in

terms of resistance between the two physical states of the material. Apart from this, swift operation, high scalability, and low power dissipation are other important properties of PCRAM which can be engineered by exploring other possible phase change materials. Wide range of flexibilities offered in the design of PCRAM makes it one of the most optimized candidates for the next generation nonvolatile memory design [12].

Currently, GST material is the most preferred material used for the fabrication of PCRAM. However, various other materials are also under investigation. This paper presents study of In_2Se_3 as a phase change material and its possible application as a PCRAM cell. Various advantages of In_2Se_3 material over the conventionally used GST material are summarized here:

(i) Highly doped GST material is required to obtain large resistances in the order of kΩ. However, In_2Se_3 based PCRAM offers reset resistance of 630 kΩ even with low doping profile.

(ii) It is highly acquiescent for multiple operation.

(iii) In_2Se_3 needs inherently low (set/reset) current due to its high resistance.

(iv) Phase isolation problems are associated with the traditionally used GST material [8].

Since In_2Se_3 offers a larger resistance margin between its two distinct states, as compared to GST materials, thus, device failure due to phase decomposition can be prevented by using In_2Se_3 materials. In_2Se_3 is also used as a phase change resistor, due to its wider change of electrical resistivity and higher value electrical resistivity compared to compound GST [9]. These offered advantages over GST based PCRAM design attract researchers to explore In_2Se_3 based PCRAM for possible solution to the current nonvolatile memory design issues [13, 14]. Figure 1 shows block diagram of In_2Se_3 based PCRAM cell. The change of phase from amorphous to the crystalline and vice versa can be achieved by heating the material by passing the required amount of current (I) as shown in Figure 1. Thus, application of electrical pulses (in the form of current) results in Joule heating mechanism of phase change materials. This allows PCRAM material to preserve two different phases, that is, crystalline phase (set or "1" state) and an amorphous phase (reset or "0" state). The basic principle of operation of PCRAM is to make the phase change material switch between an amorphous state (reset) and a crystalline state (set) by injecting different electrical pulses and thus set/reset operation can be performed.

3. Characteristics of Indium Selenide Based PCRAM

In order to develop the model of In_2Se_3 based PCRAM cell, there are some vital features which the model should fulfill [1]. These include (1) high resistance in the amorphous state (OFF state), (2) transformation to conducting ON state exhibiting negative differential conductivity when the input voltage exceeds a threshold voltage (V_{th}), (3) switch to low resistance

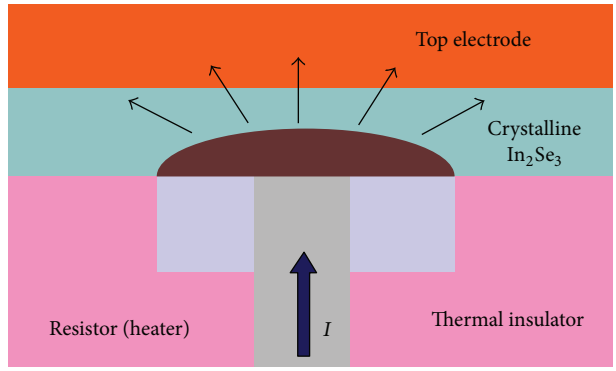

Figure 1: Block diagram representation of In_2Se_3 based PCRAM cell.

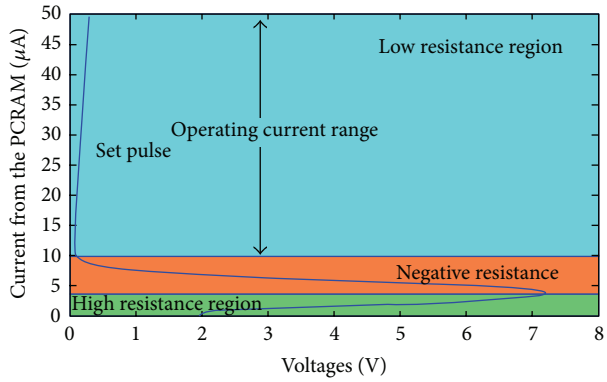

Figure 2: I-V characteristics of In_2Se_3 based PCRAM cell.

in the crystalline state, and (4) crystallization input pulse of lower amplitude and longer duration than the amorphization pulse (as shown in Figure 2). Keeping this in mind, PCRAM model is reported in this work.

Figure 2 shows that the resistance of PCRAM changes between crystalline and amorphous state at set-reset region according to the crystal fraction ratio. The NDR region shows negative differential resistance between the set-reset and ON regions.

In existing PCRAM modeling methodologies, Joule heating, heat dissipation, and crystalline fraction are derived and correlated using the equations mentioned below [9]. From the subsequent work done in [9, 10], it can be examined that the PCRAM model evaluates the resistance of phase change material based on the crystalline state. Temperature calculation is composed of two parts: Joule heating (W_J) and heat dissipation (W_D) which can be expressed as

$$\frac{dT_{\mathrm{PCM}}}{dt} = \frac{W_J - W_D}{CV}, \tag{1}$$

where T_{PCM} is the temperature of the PCM, C is the heat capacity, and V is the volume of the active region of In_2Se_3 material in the PCRAM cell (see Figure 1). The temperature of the PCRAM cell is increased due to the Joule heating which is

generated by the current (I_{PCM}) passing through it. The power supplied to the PCRAM cell can be expressed as

$$W_i = I_{PCM} \times V_{PCM} = I_{PCM}^2 \times R_{PCM}, \quad (2)$$

where I_{PCM} and R_{PCM} are the total current passing through the cell and the resistance of the cell, respectively. The temperature difference in crystalline and amorphous phase of the PCRAM cell causes power dissipation to the surroundings in the form of heat dissipation which is given as

$$W_D = \frac{\partial Q}{\partial t} = k\frac{T_{PCM} - 300^{\circ}\text{K}}{d_{PCM}}, \quad (3)$$

where Q is heat dissipated, W_D is the heat dispersion power of In_2Se_3 material of the PCRAM cell, and k is the thermal conductivity of In_2Se_3 material and d_{PCM} is the distance covered by applied electric pulse inside the PCM cell during which T_{PCM} is decreased to 300°K. The power dissipated is evaluated as

$$W_0 = \left(\frac{kV}{l^2}\right)\Delta T, \quad (4)$$

where k, V, and l are the thermal conductance, the heating volume, and the thickness of PCRAM material in the cell, respectively.

The phase change resistance model determines the resistance of the In_2Se_3 material of the PCRAM cell based on the crystalline state resistance (R_{SET}) and amorphous state resistance (R_{RESET}) linearly. The current controlled resistors, R_{SET} and R_{RESET}, can be switched between two different resistance states. The relationship between the resistances (R_{SET} and R_{RESET}) and voltage (v) is expressed as follows:

$$R_{PCM} = R_{SET} + \frac{R_{RESET} - R_{SET}}{1 + e^{((V_{th}-v)/h)}}, \quad (5)$$

where R_{SET}, R_{RESET}, V_{th}, and h are the low resistances, high resistances, and the midresistances between R_{SET} and R_{RESET} and a constant controlling the steepness of slope when switching from R_{SET} to R_{RESET}.

4. Read/Write Driver for the Presented PCRAM Model

This work proposes a read/write driver for the In_2Se_3 based PCRAM model reported here. The circuit level model of the proposed read/write driver for the In_2Se_3 based PCRAM cell is shown in Figure 4. The proposed driver circuit consists of various input ports which include Data_in (D_{IN}), DataBar_in (DB_{IN}), write enable (WR), read enable (RD), sense input (S) for sensing current outputs, and word line (WL). Here, write set (WR_{SET}) and write reset (WR_{RESET}) are used to drive set (I_{SET}) and reset currents (I_{RESET}) from PMOS current mirrors. Thus, PCRAM works in two-phase principle; that is, crystalline phase occurs in "set" mode while amorphous phase occurs in "reset" mode.

4.1. Write Operation of PCRAM. In write operation, there is change in phase of PCRAM material from one state to the other. The resistance of the two states can be read to distinguish two different memory states. The write operation involved the set mode that switches PCRAM from the high resistance state to the low resistance state and the reset mode switches the PCRAM from low resistance state to the high resistance state. So, for performing "set" operation for the presented PCRAM cell, D_{IN} and WR are set to high logic state which turns on transistors N8, N9, and N0 thereby turning off transistors P15 and P16. Thus, low value from N8 sets WR_{SET} high, thereby turning on transistors N0 and N4. If N0 and N4 are turned ON, I_{SET} becomes as large as 235 μA thereby decreasing the resistance R_{SET} of PCRAM by current mirror effect. While performing "reset" operation using the reported PCRAM cell, D_{IN} should be low and WR should be high to turn on transistors N12 and N13 thereby turning off transistors P19 and P20. As transistors N12 and N13 are grounded, this low value is fed to the inverter, thus turning WR_{RESET} high. Hence, transistors N0 and N3 are turned on for "reset" operation. Now I_{RESET} of 18.2 μA makes PCRAM resistance R_{RESET} as high as 630 KΩ by using current mirror effect. There is large difference between the resistances of set phase and reset phase of PCRAM material. For the proper execution of read operation we provide sufficiently high voltage, keeping the current value low in order to avoid write operation [15]. The set operation switches the PCRAM material into crystalline phase whereas the reset operation switches it into amorphous state. During crystalline phase the PCRAM material follows Joule heating mechanism where high value of current is injected in higher crystallization temperature. Correspondingly, in amorphous phase, PCRAM material is heated above its melting point (>600°C) to achieve amorphization [11]. The set state and reset state have a large difference between their resistances; thus, the stored data bits are determined by measuring the resulting current flowing through In_2Se_3 based PCRAM.

4.2. Read Operation of PCRAM. A small voltage is applied to PCRAM material to read the data stored in PCRAM. For reading PCRAM data, first, RD signal is kept high and WR signal is kept low to turn on transistors N1 and N2 and to turn off transistors N0, N3, and N4. At this time the small read current, I_{READ}, as small as 20 μA is applied to PCRAM. When this small I_{READ} is applied, PCRAM resistance does not change because I_{READ} is too small to change the PCRAM resistance [13]. The current outputs of write driver circuit are determined by using sense amplifier (SA), when sense input (S) is high and S_{BAR} is low thereby turning on transistors P12, P13, and N6. Hence, the current flowing through PCRAM can be sensed and compared with read current.

5. Simulation Results and Discussion

Various characteristics obtained using MATLAB have been plotted for the PCRAM model presented in this paper. Here, Figure 5(a) shows exponentially increasing curve between temperature and time of In_2Se_3 materials. Figure 5(b) depicts

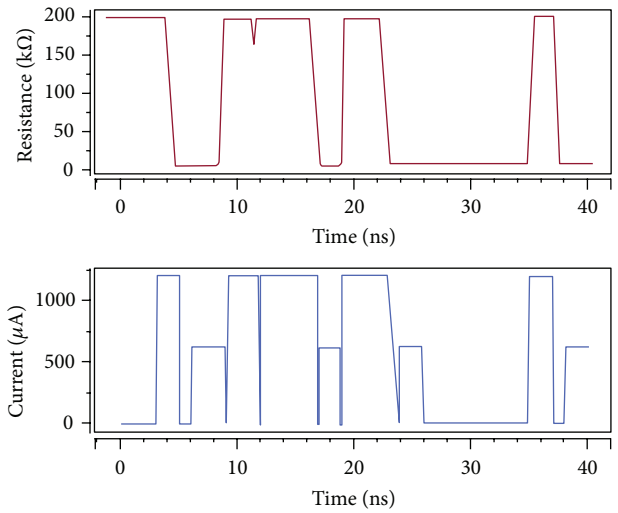

Figure 3: Resistance switching of In_2Se_3 based PCRAM with application of current pulses.

Table 1: Currents obtained during read, set, and reset operations.

Parameters	Currents obtained (A)
Read current	$4.6366E-07$
Set current	$2.3526E-07$
Reset current	$1.8176E-07$

sharp increasing current-voltage curve till 1000 μA and then it becomes constant throughout. Figure 5(c) exhibits that with the increase in current there will be decrease in resistance. Finally Figure 5(d) shows three different types of resistance regions, that is, high resistance region, negative resistance region, and low resistance region.

This paper also presents an effective design of a read/write driver for the reported PCRAM model. Simulated models of the proposed In_2Se_3 based PCRAM and the proposed read/write driver have been written in Verilog-A and executed in SPICE environment to verify the results. Various characteristics of the In_2Se_3 based PCRAM model are shown in Figure 5. The reported characteristics curves are obtained after assisting various signals in the proposed PCRAM model, namely, WL (word line), write enable (WR), read enable (RD), Data_in (D_{IN}), and sense amplifier (SA) to validate the proposed model as a memory element.

Simulated result of *I-V* characteristics of the above proposed PCRAM model is shown in Figure 5 and SPICE simulated result of resistance switching is shown in Figure 3. The output currents of read, set, and reset operation of the proposed model on Indium Selenide materials after simulating on SPICE are tabulated in Table 1.

The model equations reported in this paper have been utilized to propose the PCRAM model. The characteristics curves obtained in this work (see Figure 5) go in line with the work available in the literature. The read/write circuitry reported in this work has been utilized to validate the proposed model. The nonvolatile nature of the PCRAM can be observed by the resistance and current relationships reported in Figure 3 in which the resistance state is still preserved even if the current pulse is removed. Thus, data can be stored in the form of either low or high resistance state and can be retrieved based upon the input signals applied to the read/write circuitry. Further various characteristics properties of Indium Selenide based PCRAM cell are reported in Table 2.

Table 2: Characteristics properties of Indium Selenide based PCRAM.

Parameter	Symbol	Numeric data
Threshold voltage	V_{th}	0.78 V
Holding voltage	V_H	0.45 V
Melting point of In_2Se_3	T_M	600°C
Glass transition point (In_2Se_3)	T_C	373°C
Crystalline state resistance (static resistance of set)	R_{SET}	103 Ω
Amorphous state resistance (static resistance of reset)	R_{RESET}	630 kΩ
Dynamic on-resistance		1 kΩ
Thermal conductivity of In_2Se_3		37 W $cm^{-1}K^{-1}$ (parallel) 120 W $cm^{-1}K^{-1}$ (perpendicular)
Thermal capacity of In_2Se_3	C	1.25 $Jcm^{-3}K^{-1}$
Activation energy of In_2Se_3	E_a	0.17 eV
Boltzmann constant	k_B	1.380×10^{-23} J/K
Volume of PCM cell	V	7×10^{-14} cm^3
Reset current	I_{RESET}	11.7 μA
Set current	I_{SET}	208 μA
Reset pulse width	T_{RESET}	20 ns
Set pulse width	T_{SET}	100 μs
Read current	I_{READ}	5 μA
Read pulse width	T_{READ}	25 ns
Resistance switching ratio	RSR	2×10^5
Electrical resistivity		6.7 ohm-cm
Specific heat		0.27 $Jcm^{-3}K^{-1}$
Reset power	P_{RESET}	80 μW
Set power	P_{SET}	0.25 nW
Reset energy	E_{RESET}	1.6 PJ
Set energy	E_{SET}	25 Fj
Crystallization temp	T_X	477°C

6. Conclusion

This paper emerges with the successful modeling of In_2Se_3 based PCRAM cell. The proposed model has been simulated using SPICE and simulation results have been extensively verified with the same. Also, MATLAB has been utilized to extract various parameters of the reported model. The modeled characteristics of In_2Se_3 based PCRAM cell have been further integrated with the CMOS based read/write circuit. The simulation results show the data operation with the read enable and write enable signals and agree with

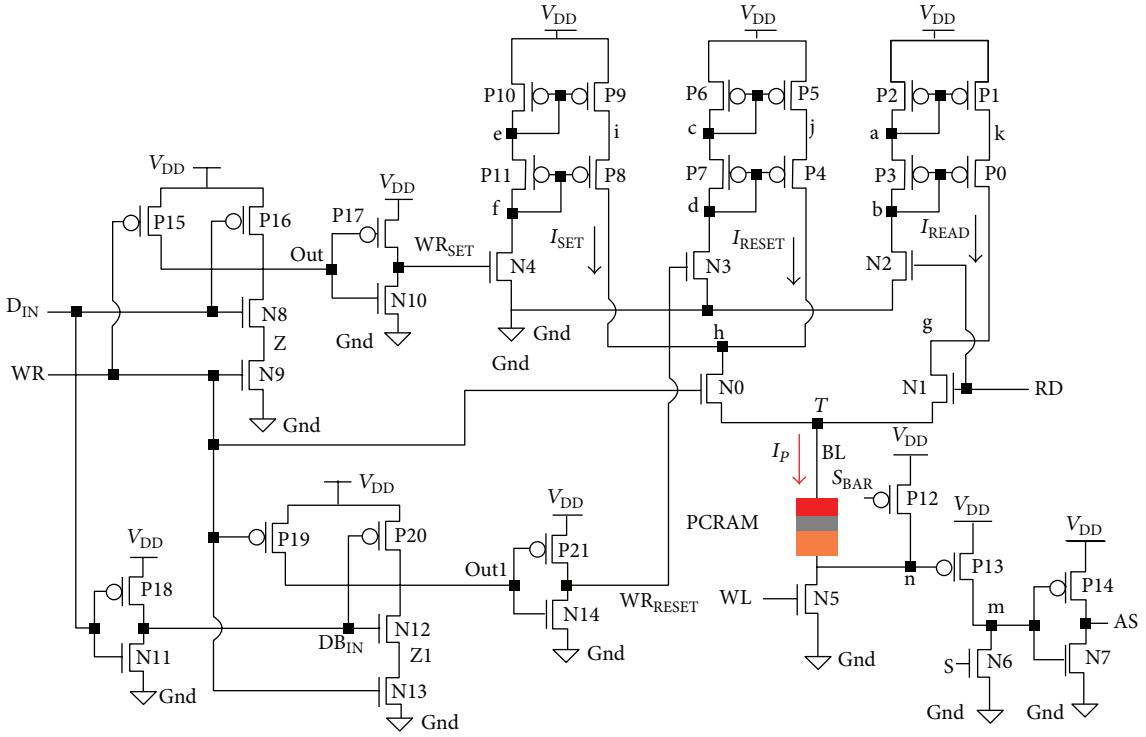

FIGURE 4: Circuit level model of the proposed read/write driver for the In_2Se_3 based PCRAM cell.

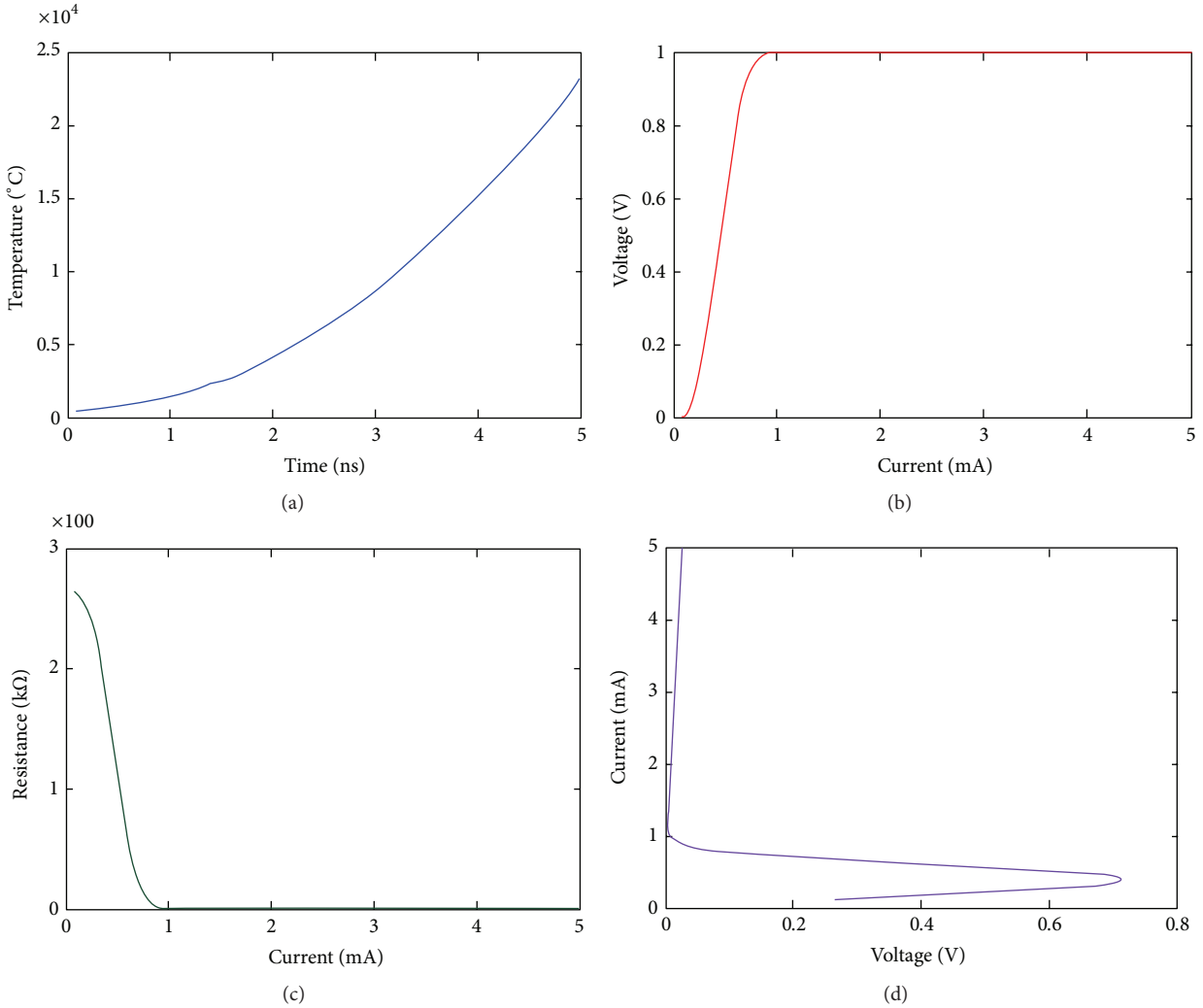

FIGURE 5: *I-V* characteristics of In_2Se_3 based PCRAM cell.

the phase change characteristics of the PCRAM. The output currents of read operation along with set and reset operation of the proposed model on Indium Selenide materials after simulating on SPICE have been also reported. Finally, this validates the nonvolatility of the proposed model by obtaining the current and resistance relationships which suggests that even if the current pulse is removed, the resistance state is still preserved. Thus, information stored in the form of resistance can be resorted even if the supply is removed.

Competing Interests

The authors declare that they have no competing interests.

References

[1] A. K. Dwivedi, S. Kumari, and A. Islam, "Characterization of phase-change material using verilog-a and its validation as a memory element," in *Proceedings of the IEEE Conference on Devices, Circuits and Communications*, Ranchi, India, September 2014.

[2] A. T. Mitchell and R. Bert, "Non-volatile semiconductor memory," US Patent 5,168,334, 1992.

[3] A. K. Dwivedi and A. Islam, "Nonvolatile and robust design of content addressable memory cell using magnetic tunnel junction at nanoscale regime," *IEEE Transactions on Magnetics*, vol. 51, no. 12, pp. 1–13, 2015.

[4] A. K. Dwivedi and A. Islam, "Design of magnetic tunnel junction-based tunable spin torque oscillator at nanoscale regime," *IET Circuits, Devices & Systems*, vol. 10, no. 2, pp. 121–129, 2016.

[5] X. Q. Wei, L. P. Shi, R. Walia et al., "HSPICE macromodel of PCRAM for binary and multilevel storage," *IEEE Transactions on Electron Devices*, vol. 53, no. 1, pp. 56–62, 2006.

[6] X. Q. Wei, L. P. Shi, W. Rajan et al., "Universal HSPICE model for chalcogenide based phasechange memory elements," in *Proceedings of the Non-Volatile Memory Technology Symposium (NVMTS '04)*, pp. 88–91, IEEE Press, Orlando, Fla, USA, August 2004.

[7] R. A. Cobley and C. D. Wright, "Parameterized SPICE model for a phase-change RAM device," *IEEE Transactions on Electron Devices*, vol. 53, no. 1, pp. 112–117, 2006.

[8] B. Yu, X. Sun, S. Ju, D. B. Janes, and M. Meyyappan, "Chalcogenide-nanowire-based phase change memory," *IEEE Transactions on Nanotechnology*, vol. 7, no. 4, pp. 496–502, 2008.

[9] H. Lee, Y. K. Kim, D. Kim, and D.-H. Kang, "Switching behavior of indium selenide-based phase-change memory cell," *IEEE Transactions on Magnetics*, vol. 41, no. 2, pp. 1034–1036, 2005.

[10] X. Sun, B. Yu, G. Ng, M. Meyyappan, S. Ju, and D. B. Janes, "Germanium antimonide phase-change nanowires for memory applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 11, pp. 3131–3135, 2008.

[11] K. C. Kwong, L. Li, J. He, and M. Chan, "Verilog-A model for phase change memory simulation," in *Proceedings of the 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT '08)*, pp. 492–495, Beijing, China, October 2008.

[12] X. Dong, N. P. Jouppi, and Y. Xie, "PCRAMsim: system-level performance, energy, and area modeling for phase-change RAM," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design—Digest of Technical Papers (ICCAD '09)*, pp. 269–275, San Jose, Calif, USA, November 2009.

[13] V. B. Boledzyuk, A. V. Zaslonkin, Z. D. Kovalyuk, and M. M. Pyrlya, "Electrical properties of In_2Se_3 intercalated layered crystals," *Ukrainian Journal of Physics*, vol. 56, no. 4, pp. 376–380, 2011.

[14] K. Bindu, C. Sudha Kartha, K. P. Vijayakumar, T. Abe, and Y. Kashiwaba, "Structural, optical and electrical properties of In_2Se_3 thin films formed by annealing chemically deposited Se and vacuum evaporated in stack layers," *Applied Surface Science*, vol. 191, no. 1–4, pp. 138–147, 2002.

[15] C.-M. Jung, E.-S. Lee, and K.-S. Min, "Continuous and accurate PCRAM current-voltage model," *Journal of Semiconductor Technology and Science*, vol. 11, no. 3, pp. 162–168, 2011.