Hindawi Publishing Corporation Indian Journal of Materials Science Volume 2016, Article ID 7419584, 4 pages http://dx.doi.org/10.1155/2016/7419584



Research Article

Process to Improve the Adherences of Copper to a PTFE Plate

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Received 19 May 2016; Revised 24 July 2016; Accepted 4 August 2016

Academic Editor: Debdulal Das

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A simple low plasma power and roughness free process for improving the adherence of Cu to PTFE is presented. The results show that low pressure and Ar flow combination are the drivers of this improved adherence. Copper Peel Strength Tensile values up to 60 kg/m are obtained which are comparable to those shown in commercial composite dielectrics for high-frequency applications Printed Circuit Boards.

1. Introduction

Polytetrafluoroethylene (PTFE) has an unusual combination of high thermal stability, chemical inertness, and electrical stability. The properties of PTFE have led to many successful chemical and electrical applications, such as electrical cable, lining for reactor, and antisticking coatings for kitchen utensil and tapes. However, its poor adhesion has limited its application in many fields. There have been many studies for improving the surface adherence of the PTFE, such as wet chemical treatment, plasma, and ion bean, but most of these introduce roughness in the surface of the dielectric [1].

The tremendous progress that has been made in the past four decades in miniaturizing and integration transistors onto silicon has contributed to the continuing increase in component, performance, and load density [2]. All progresses have required that transmission lines find a corresponding way for increasing density of the substrate and reducing losses. Moreover, modern applications ranging from high-frequency telecommunications systems to high rate of bytes/s in current computers have set new requirements on Printed Circuit Board (PCB).

There are three characteristics that the PCB shop needs to master successfully process PTFE fabrication boards and if we can meet these three requirements, everything else will be essentially like processing rigid double sided FR-4; the requirements are

- (1) copper surface preparation,
- (2) drilling PTFE materials,

(3) plated through hole and PTFE surface preparation [3].

One of the most popular waveguides in a PCB is the microstrip. Among the figures of merit that help us determine its performance, we can mention the losses; the line losses (α) are composed of two contributions: dielectric losses (α_d) and ohmic losses (α_c) . The α_c depends on DC resistance $(R_{\rm dc})$, AC resistance $(R_{\rm ac})$, and real part of the impedance $(R(Z_0))$, and the resistances are obtained from the following parameters: metal conductivity (σ) , permeability (μ) , frequency (f) and physical dimensions of the line width (w), and thickness of the metal (t) [4].

To incorporate the effect of the surface roughness, an empirical roughness factor (k_r) is added to the formula for $R_{\rm ac}$ (4). The transition frequency for this increase in resistance is dependent on the root mean square (RMS) value of the roughness $(h_{\rm RMS})$, which can be measured directly on the copper foil or estimated from cross sections (see Figure 1).

In a conventional PCB fabrication process, the roughness is used for promoting adhesion of metals to the substrate. Since the rough copper surface affects current flow, it will affect also power dissipation and thus the losses. The traditional way to account for surface roughness losses in a transmission-line model is to use Hammerstad coefficient; it is described in (5).

Equations (1) to (5) show the relationship among all the aforementioned parameters. The roughness is an important factor in the ohmic losses especially when we need a low-loss PCB. $R_{\rm ac}$ is directly proportional to k_r ; $R_{\rm ac}$ is the largest

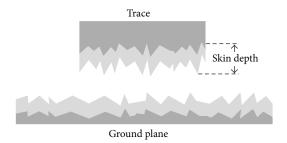


FIGURE 1: Realistic conductors used to manufacture transmission lines exhibit a rough surface called the "tooth structure." When the skin depth is similar to tooth size, power dissipation increased [11].

contribution of the ohmic losses; the Hammerstad coefficient depends on roughness. Thus, by reducing the roughness, the ohmic losses can be reduced.

$$\alpha = \alpha_d + \alpha_c \text{ Np/leng},$$
 (1)

$$\alpha_c = \frac{1}{2} \frac{R_{dc} + R_{ac}}{R(Z_0)} \text{ Np/leng,}$$
 (2)

$$R_{\rm dc} = \frac{1}{\sigma mt} \Omega/{\rm leng},$$
 (3)

$$R_{\rm ac} = \frac{k_r}{w+t} \sqrt{\frac{\pi f \mu}{\sigma}} \ \Omega/{\rm leng},$$
 (4)

$$k_r = 1 + \frac{2}{\pi} \arctan\left(1.4\pi\mu\sigma f h_{\rm RSM}^2\right). \tag{5}$$

In order to reduce the ohmic losses, the Teflon is polished to decrease it and Cu is electrodeposited on its surface as the conductor in this PCB material proposal. The aim of this work is to obtain a good adherence between the Teflon and copper while maintaining the interface Teflon-Cu as polished as possible, because the roughness decreases greatly the performance of a PCB. Actually, the losses are not of the PCB but of the devices built in the PCB.

For instance, in a coplanar waveguide, there are three types of losses: dielectric, ohmic, and radiation/surface wave [4]. In most cases, the radiation losses are neglected; then, we will concentrate on the dielectric and ohmic losses. The dielectric losses (α_d) depend on loss tangent $(\tan \delta)$ and relative permittivity (ε_r) and the dimension of the line: thickness of dielectric (h), width of line (w), and thickness of metal (t). The loss tangent and the permittivity are inherent to the dielectric material. Teflon (PTFE) is selected as substrate material because it has one of the smallest values for both ε_r (2.0-2.3) and $\tan \delta$ (0.00025) [5]. Equations (6) and (7) show the relationship of ε_r and $\tan \delta$ with dielectric losses.

$$\alpha_d = \frac{1}{2}\omega \frac{\sqrt{\varepsilon_{\text{eff}}}}{c} \tan \delta \text{ Np/leng,}$$
 (6)

where $\omega = 2\pi f$ and c = light velocity.

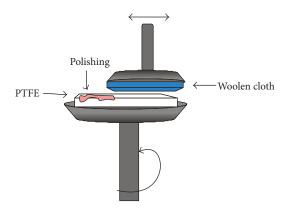


FIGURE 2: Polishing system.

$$\varepsilon_{\text{eff}} = \frac{\varepsilon_r + 1}{2} \frac{\varepsilon_r - 1}{2} F - C,$$

F

$$= \begin{cases} \frac{1}{1.71} \left(1 + 12 \frac{h}{w} \right)^{-1/2} + 0.04 \left(1 - \frac{w}{h} \right)^2, & \left(\frac{w}{h} \right) \le 1, \\ \frac{1}{1.71} \left(1 + 12 \frac{h}{w} \right)^{-1/2}, & \left(\frac{w}{h} \right) \ge 1, \end{cases}$$
(7)

$$C = \frac{\varepsilon_r - 1}{7.9} \frac{t}{h} \sqrt{\frac{h}{w}}.$$

2. Materials and Methods

The process begins by polishing Teflon; this process is a modification of the common glass polishing process, and thus the average surface roughness decreases from 500 to 30 nm RMS.

The polishing procedure is mechanical and performed by using aluminum oxide powder (about $1\,\mu\text{m}$ diameter) in water. The Teflon is polished because of the friction between it and the polishing mixture, illustrated in Figure 2 that depicts the polishing system used in this work.

After the polishing, the roughness of Teflon surface is measured with Atomic Force Microscope (AFM) and an image of the surface is shown in Figure 3. As can be seen in it, the average roughness is around 30 nm measured after the plasma treatment described below. The polishing step is necessary because when the roughness decreases at the interface metal dielectric, the Hammerstad coefficient also decreases.

In Figure 4, we have plotted the behavior of the Hammerstad coefficient as a function of the values of the roughness for frequencies up to 10 GHz. As a comparison, Teflon without polishing ($h_{\rm RMS}=0.5\,\mu{\rm m}$) is also showed, Teflon polished with our process ($h_{\rm RMS}=30\,{\rm nm}$) and a typical value of the commercial PCB ($h_{\rm RMS}=1.8\,\mu{\rm m}$). With a roughness of 30 nm, k_r is almost 1.0 in the whole frequency range and its contribution to the ohmic losses will be negligible.

To improve the Cu adherence, the next step is an argon plasma treatment on the polished PTFE surface. This process

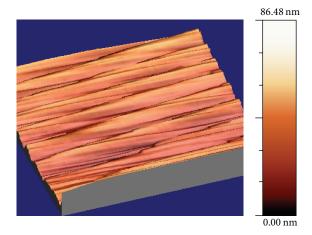
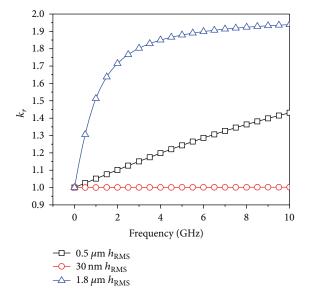


FIGURE 3: Surface of the Teflon after polish.



 $\label{thm:figure 4: Plot of the Hammerstad coefficient using (5) with different values of roughness.$

was done using a Reactive Ion Etching (RIE) system of parallel plates; in Table 1 are shown the different conditions (Ar flow, pressure, and RF power) to obtain better adherence to the polished PTFE surface. The whole process takes 8 minutes. Then, a 0.5-micrometer-thick copper layer is deposited on the PTFE by E-bean evaporation. Subsequently, the copper is thickened by electroplating. In this process, a standard Cu solution is used and the 0.5 microns of copper on the Teflon is the anode and a copper plate is used as cathode. The current density is 0.94 amperes per square decimeter (A/dm²), and the Cu thickness increase to 25 microns after one hour [5].

In this step of the process, one test is done, which is copper peel strength testing. It is worth mentioning that for the lowest flow (10 SCCM) in all cases there was not observed any adherence to the polished Teflon surface.

TABLE 1: Process conditions at the RIE for Cu adherence to the polished Teflon.

Pressure (mTorrs)	Power (watts)	Flow (SCCM*)
30	250	30
10	250	30
5	250	30
30	250	20
10	250	20
5	250	20
30	250	10
10	250	10
5	250	10
30	150	30
10	150	30
5	150	30
30	150	20
10	150	20
5	150	20
30	150	10
10	150	10
5	150	10
30	100	30
10	100	30
5	100	30
30	100	20
10	100	20
5	100	20
30	100	10
10	100	10
5	100	10

^{*} SCCM is standard cubic centimeters per minute, a flow measurement term indicating cm³/min at a standard temperature and pressure.

3. Results and Discussion

Figure 5 shows the resulting Copper Peel Strength Tensile (CPST) on the polished Teflon surface after the different Ar plasma treatments.

The test of copper peel strength was done with XLW (PC) Auto Tensile Tester; we can see this system in Figure 6 and the best result was 3.93 pounds/inch (about 70 kg/m), which is as good as some commercial PCB's or better [6, 7]. This test is useful for knowing the integrity of structures built in a PCB, but the minimum of pressure.

We can observe from Figure 5 that the largest CPST values are obtained at the lowest pressures for all the treatment conditions here used, and the best value for CPST is when the power applied to the plasma is 250 W. This applied power is the same at which H-H Chien [8] observed the largest wetting angle on PTFE; the aforementioned author also notice that larger power applied to the plasma results in decrease in the wetting angle, which means the surface of the PFTE is turning hydrophobic; the later means that there is a decrease in Cu adhesion. Another important fact to note is that in [9, 10] it is reported that larger treatment times (larger than 10 minutes)

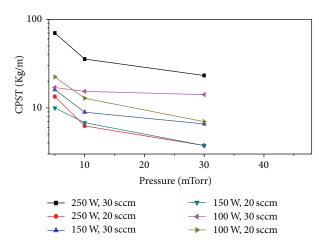


FIGURE 5: Copper Peel Strength Tensile (CPST) on the polished Teflon surface after the different Ar plasma treatments.

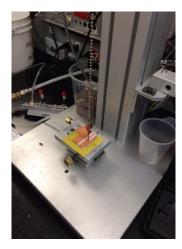


FIGURE 6: System to measure copper peel strength.

and higher applied power will result in increase of the average roughness of the PTFE, property that in this work is kept constant after the mechanical polishing and plasma process and is the main result here obtained. As a result, a better performance and minimum losses are the characteristics of the waveguides and devices built on this PTFE substrate.

4. Conclusions

In this work, a simple and low power plasma process for improving the adherence of Cu to polished Teflon without increasing the roughness is demonstrated. This result is in contrast to many current plasma processes for the same purpose of increasing the adherence of Cu to PTFE that rely on roughening the substrate surface.

The best result of CPST here obtained is comparable to some commercial substrates that use a composite dielectric; moreover, it was performed with a final average roughness of only 30 nm.

The best conditions for improving adherence are low pressure and low plasma power and only 8 minutes of plasma process is enough for achieving good results.

Competing Interests

The authors declare that there are no competing interests regarding the publication of this paper.

Acknowledgments

The authors express their deep sense of gratitude to Svetlana Sejas Garcia and Isola Group for the measurements of the CPST.

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