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Research Article

Demonstration of Ultra-Fast Switching in Nanometallic Resistive Switching Memory Devices

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Interdependency of switching voltage and time creates a dilemma/obstacle for most resistive switching memories, which indicates low switching voltage and ultra-fast switching time cannot be simultaneously achieved. In this paper, an ultra-fast (sub-100 ns) yet low switching voltage resistive switching memory device ("nanometallic ReRAM") was demonstrated. Experimental switching voltage is found independent of pulse width (intrinsic device property) when the pulse is long but shows abrupt time dependence ("cliff") as pulse width approaches characteristic *RC* time of memory device (extrinsic device property). Both experiment and simulation show that the onset of cliff behavior is dependent on physical device size and parasitic resistance, which is expected to diminish as technology nodes shrink down. We believe this study provides solid evidence that nanometallic resistive switching memory can be reliably operated at low voltage and ultra-fast regime, thus beneficial to future memory technology.

1. Introduction

Resistive random access memory (ReRAM) offers a competitive solution to future digital memory, given its superior properties such as long data retention, nanosecond speed, high endurance, multibit capability, and flexible scalability [1, 2]. Extensive studies have been conducted to explore the resistive switching speed, which intends to answer the question: how fast "1" can be converted to "0" [3–8]. Researchers found that, in ion-migration system, such switching speed is strongly correlated with applied voltage. Specifically, a larger voltage can inject more energy to the filamentary system, consequently generating higher temperature to facilitate ion migration. Therefore, it requires shorter time to complete resistive switching process. Further numerical simulation confirms such argument, quantitatively predicting that required switching voltage keeps increasing over 4 times from 100 seconds to 100 nanoseconds [5]. This nonlinear switching kinetics is not preferred to the practical demands of fast speed yet low voltage/power in emerging memory systems. On the other hand, in a real integrated memory array, substantial circuit effect could further worsen the situation by introducing *RC* delay and voltage partition from interconnect lines [9–12]. A feasible solution to aforementioned problem is through non-temperature related system, such as electronic switching ReRAM [13–16]. In general, electronic resistance switching occurs *via* trapping or detrapping of electrons, where negligible temperature effects are involved and switching itself only depends on energy landscapes determined by intrinsic material or structure properties. On the other hand, electrons generally "move" faster than ions given its small mass. In this sense, intrinsic switching speed of electronic devices should exceed that of ionic devices. A subpicosecond electronic switching has been demonstrated in [7].

In this paper, we demonstrate a switching-time independent ReRAM and explicitly address circuit related problems based on a recent developed nanometallic device. Nanometallic ReRAM is a purely electronic, metal-insulator switching memory built on a hybrid structure, which is composed of atomically dispersed metal inside an insulator matrix. Such ReRAMs exhibit outstanding device properties such as long retention and endurance [17], low power [10], and multilevel capability [9, 11, 12]. Although nanometallic ReRAM can be constructed using a large variety of insulator:metal paring [7, 17], here we focus on Si_3N_4:Pt films. We will demonstrate that Si_3N_4:Pt nanometallic ReRAMs can achieve ultra-fast (sub-100 ns) yet low switching voltage and

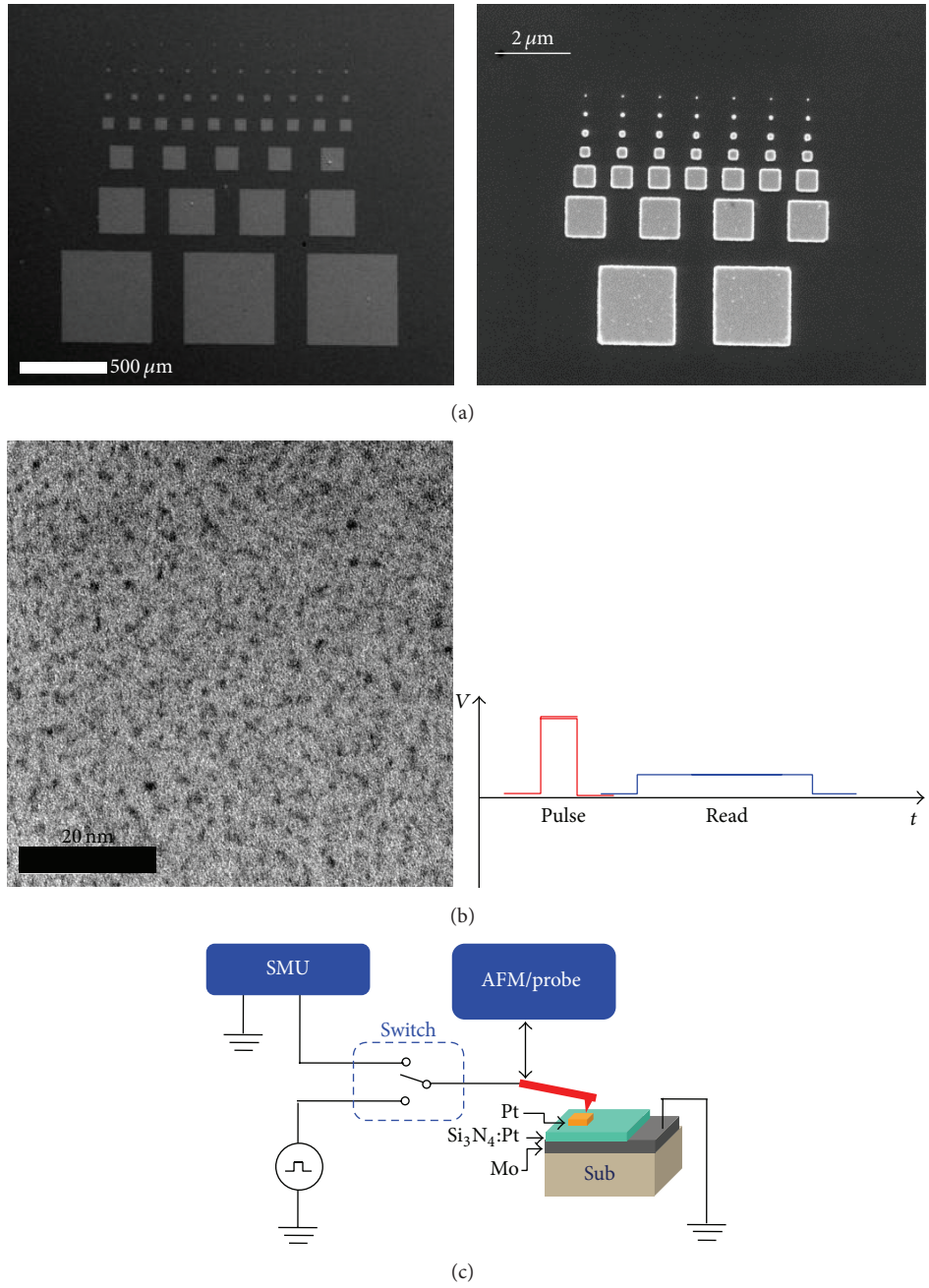

FIGURE 1: (a) Top view SEM image of devices ranging from 512 × 512 μm^2 to 100 × 100 nm^2. (b) Planar view TEM image of 93% $SiN_{4/3}$:7% Pt films. Dark regions are clustered Pt nanoparticles (<1 nm). (c) The schematic for fabricated Mo/Si_3N_4:Pt/Pt devices and the experimental setup.

thus are promising to be implemented in future memory systems.

2. Materials and Method

A Mo film (20 nm thick), as the bottom electrode, was firstly deposited to an unheated SiO_2/Si substrate using DC sputtering. Then the mixture film Si_3N_4:Pt was cosputtered using separate Si_3N_4 and Pt targets in a magnetron sputtering system (Initial chamber pressure of Denton sputter system was better than 3 × 10^{-7} Torr). Afterwards, conventional photolithography and e-beam lithography techniques were used to pattern top electrodes with various sizes, ranging from 512 μm to 5 μm (photolithography) or from 2 μm to 50 nm (e-beam lithography). Eventually, a top Pt electrode (40 nm) was RF-sputter deposited followed by lift-off process. The composition of the nanometallic films was determined to be 93% $SiN_{4/3}$:7% Pt according to Rutherford Backscattered Spectroscopy (RBS). Figure 1(a) shows top view of SEM image of micron and nano devices. Figure 1(b) shows high

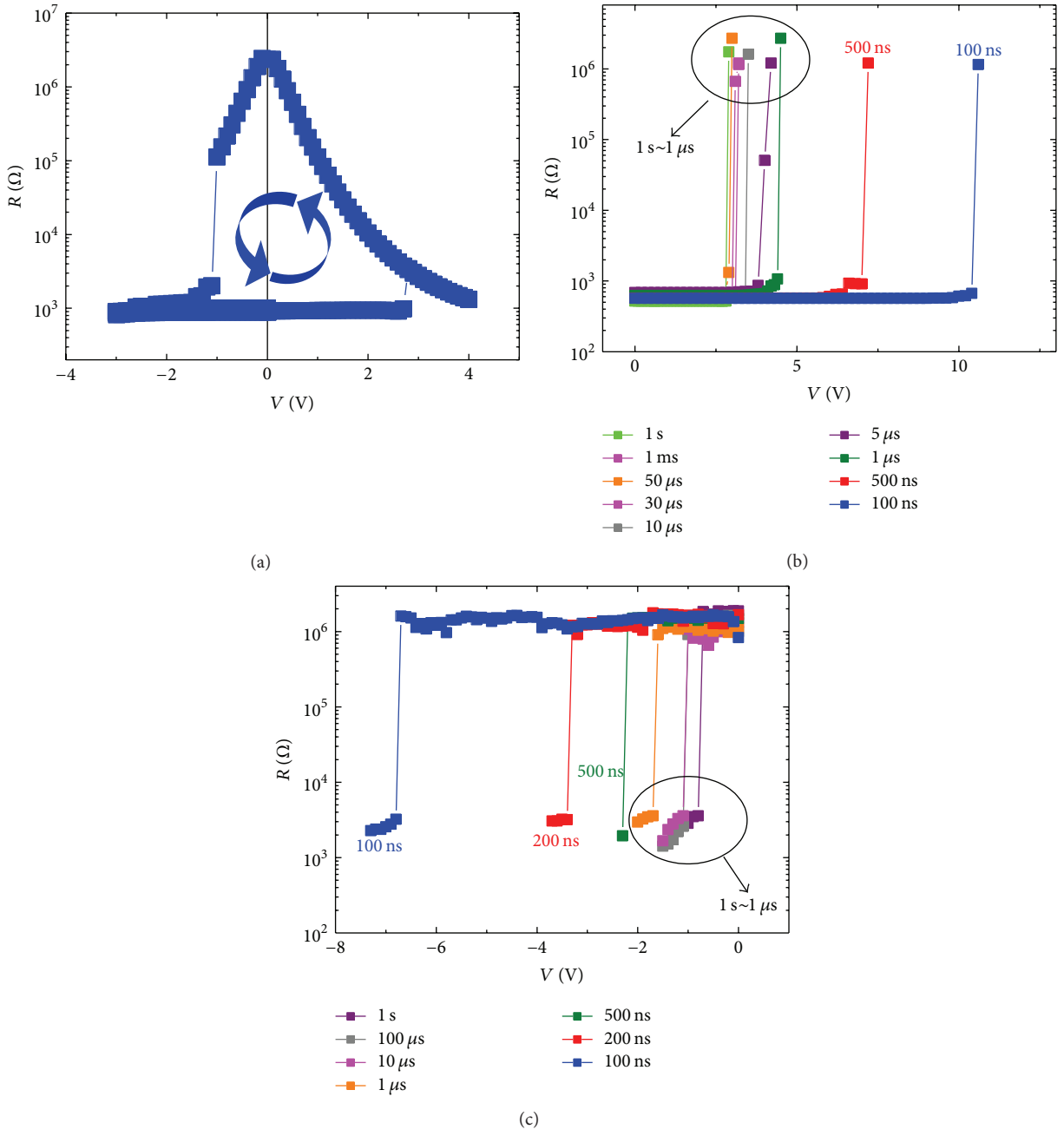

FIGURE 2: (a) Characteristic resistance-voltage (R-V) switching curve. The arrows indicate switching direction. (b) Off → on switching by using different pulse widths for a 400 × 400 μm^2 device. (c) On → off switching by using different pulse widths for a 400 × 400 μm^2 device.

resolution TEM image of fabricated $SiN_{4/3}$:Pt film, where sub-1 nm Pt nanoparticles are distributed evenly in the $SiN_{4/3}$ film. All pads are well separated and sizes were consistent with our nominal sizes. To characterize the device properties, micron devices were tested using a probe station (Signatone S1160) while nano devices were tested using a conducting atomic force microscope (CAFM, Asylum MFP-3D), by routing electrical signal out to a semiconductor analyzer (Keithley 237) or pulse generator (Agilent 81104A). The schematic of experiment setup is shown in Figure 1(c). For pulse width dependence measurement, we used a pump-probe method: excitation pulse signal with certain pulse width (from 20 ns to 1 s) and voltage height was firstly sent to device and then a small DC voltage (0.2 V) was used to probe the resultant resistance states. A switch box was employed to avoid interference between two electrical sources.

3. Results and Discussion

As-fabricated ReRAM devices exhibit bipolar switching behavior, as shown in the R-V curve of Figure 2(a). The R-V curve was obtained using the following voltage sweep sequence: 0 V, to 4 V, to −3 V, and to 0 V. Here a positive bias means current flowing from top to bottom electrode. The

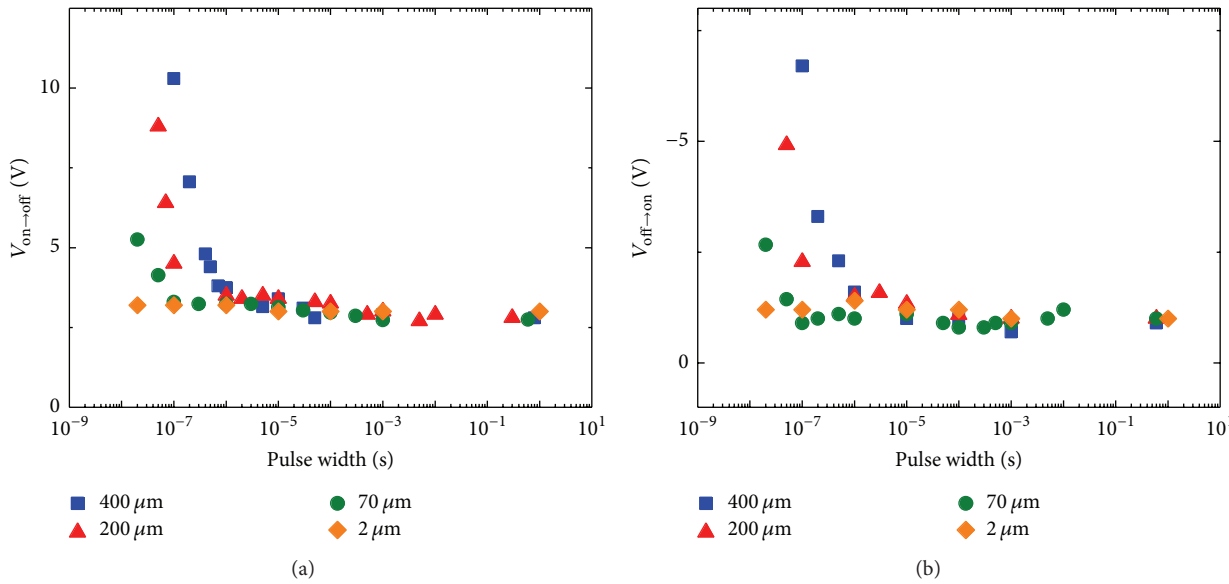

FIGURE 3: (a) Experimentally measured on → off switching voltage *versus* pulse widths for various device sizes. (b) Experimentally measured off → on switching voltage *versus* pulse widths for various device sizes.

fabricated devices are electroforming free and thus show a flat resistance in the *R-V* curve (corresponding to a linear *I-V* curve). With an incremental positive voltage, the device gets abruptly "turned off" at $V_{on\to off} = 3$ V. Next, it stays at an insulating or high-resistance state (HRS), which exhibits a nonlinear *R-V* behavior. Under a negative voltage, the HRS jumps back to low-resistance state (LRS) at $V_{off\to on} = -1$ V. In fact, several intermediate states can be observed until the device reaches its final state. Figure 2(b) shows the on → off switching under different pulse widths and heights for a $400 \times 400\ \mu m^2$ cell. Device was initially set at LRS. Then a pulse sequence (0.1 V → 0.2 V → 0.3 V → etc.) with certain width was sent in and a probe signal was followed to check the resistance after each individual pulse (definition: $R = V/I$ at $V = 0.2$ V). The test was continued until the device jumps to HRS ~MΩ. After resistance change, the cell was reset to LRS using −3 V DC voltage, which ensures each test starting from exactly same condition. As shown in Figure 2(b), on → off switching voltages are independent of pulse widths ranging from 1 s to 10 μs. As pulse widths are shorter than ~μs, on → off switching voltage rapidly increases. As pulse width reaches 100 ns, required voltage is as high as 10 V. Similar phenomenon was observed for off → on switching process in Figure 2(c): off → on switching voltage keeps ~−1 V until pulse width <μs, followed by a rapid increase up to −9 V for 100 ns pulse. It is worthwhile to mention that off → on resistance further decreases with higher voltage, indicating multilevel resistance exists, which is consistent with earlier reports [7, 9–11]. The switching voltage defined in this paper refers to the critical voltage for the first abrupt drop of resistance.

Similar phenomenon occurs for other sizes as well. As shown in Figures 3(a) and 3(b), every size shows a constant switching voltage up to a threshold pulse width ("cliff"). However, such cliff varies with device lateral dimensions. Smaller sizes exhibit cliff behavior at shorter pulse while larger sizes start to show cliff behavior at a longer pulse. For nano devices with sizes less than $2 \times 2\ \mu m^2$, both on → off and off → on switching voltages are completely independent of pulse width within our testing range (from 20 ns to 1 s). The detailed transient behavior during off → on and on → off is generally abrupt within our instrument capability, which has been reported elsewhere [18].

The most intriguing property is switching voltage-time independence before threshold pulse width, which is quite different from any reported data in the literature [5, 8]. Nonlinear switching voltage-time relation is usually observed in traditional ionic systems. Such nonlinearity arises from a voltage induced temperature increase in a few-nanometer-thick region near electrode and an exponential increase in oxygen-vacancy mobility [5]. In this scenario, required switching voltage keeps changing as pulse width varies from ~second to ~nanosecond. However, such ionic migration related phenomenon is absent in nanometallic system, which confirms its electronic switching nature. In nanometallic RERAM, switching depends on whether external voltage can overcome energy barriers and consequently induce electron trapping or detrapping. Such process involves only electron tunneling and thus shows time independency. Of course, electron tunneling speed could determine the ultimate limit of switching speed, but that is far beyond nanosecond region and thus not an issue for current electronic devices.

Next, we discuss the "threshold pulse width (cliff)" phenomenon. Apparently, this is not likely an intrinsic property because of device size dependency. Required pulse voltage starts to change at longer pulses for a larger size while remaining unchanged for extreme small size. Such threshold phenomenon can be well understood if we consider the *RC* circuit effect. An equivalent circuit of the device is illustrated

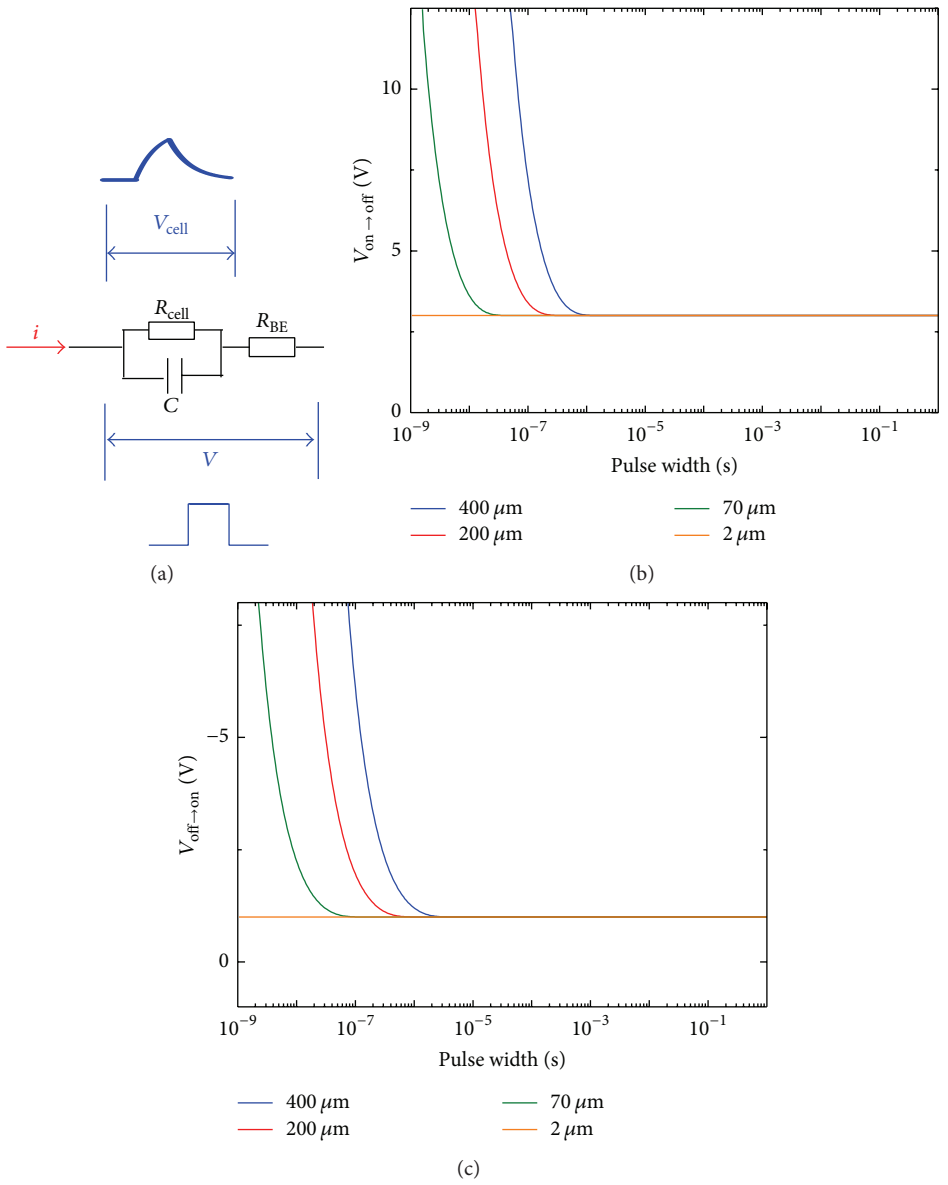

FIGURE 4: (a) Equivalent circuit: device structure composed of electrode resistor R_{BE} (mostly due to spreading resistance in bottom electrode) serially connected to a set of parallel cell resistance R_{cell} and cell capacitance C. Apparent voltage V is larger than the actual cell voltage V_{cell}. (b) Simulated on → off switching voltage *versus* pulse widths for various device sizes. (c) Simulated off → on switching voltage *versus* pulse widths for various device sizes.

in Figure 4(a), where a resistor R_{BE} is serially connected to $R/\!/C$ cell. The serial resistor R_{BE} can originate from bottom electrode resistance, interface resistance, or any parasitic line resistance. Intrinsic cell can be represented as an ideal RC parallel circuit. As an ideal square pulse is applied on the entire structure, cells cannot acquire voltage instantly because of capacitor charging effect. Rather, it experiences transient time roughly $\sim R_{BE}C$ to reach the steady state voltage, which is given by $V^*_{cell} = (R_{cell}/(R_{cell} + R_{BE}))V$. However, if the applied pulse is so short that it starts to disappear before capacitor achieving the designated voltage, then such $R/\!/C$ cell can never obtain its steady state V^*_{cell}. As a result, higher voltage V is required to compensate this RC-delay induced voltage inefficiency. An analytical solution for transient cell voltage can be derived from

$$i = \frac{V - V_{cell}}{R_{BE}} = \frac{V_{cell}}{R_{cell}} + C\frac{dV_{cell}}{dt}. \quad (1)$$

Assuming the square pulse starts from $t = 0$, the cell voltage can be expressed as

$$V_{cell} = \frac{R_{cell}}{R_{cell}+R_{BE}}\left[1 - \exp\left(-\frac{R_{cell} + R_{BE}}{CR_{cell}R_{BE}}t\right)\right] \times V. \quad (2)$$

RC-delay time is modified as $CR_{cell}R_{BE}/(R_{cell} + R_{BE})$, due to shunt effect of cell resistance, which has an upper

limit $R_{BE}C$ as cell resistance is infinitely high. Because cell capacitance is linear dependent on size following $C = \varepsilon d^2/\delta$ (ε: dielectric constant, d: cell lateral length, and δ: film thickness) while R_{BE} is independent of size, we can expect the delay time $\sim R_{BE}C$ to exhibit strong size dependence. By applying the above expression and assuming the intrinsic cell switching voltage is $V_{cell}^{on\to off} = 3$ V and $V_{cell}^{off\to on} = -1$ V (from DC switching data in Figure 2(a)) with further assumptions of $C(400\,\mu m) = 700$ pF, $R_{BE} = 800\,\Omega$, $R_{cell,HRS}(400\,\mu m) = 1\,M\Omega$, and $R_{cell,LRS} = 400\,\Omega$, we can obtain Figures 4(b) and 4(c) for on → off and off → on switching, respectively. Consistent with experimental data in Figure 3, larger sizes start to exhibit switching voltage increase at longer pulse width, while smaller sizes postpone such effect to a shorter pulse. For extremely small size ($2 \times 2\,\mu m^2$ or less), there is no obvious increase within nanosecond to second range, because delay time $\sim R_{BE}C = 800\,\Omega \times 18$ fF $= 15$ ps, way below nanosecond. Therefore, it suggests this "threshold" phenomenon is a purely circuit effect.

In fact, such switching voltage-time independence is universal in many nanometallic films. Other than Si_3N_4:Pt film, SiO_2:Pt and perovskite nanometallic film $LaAlO_3$:$LaNiO_3$ also exhibit similar independence as illustrated in [19, 20] (SiO_2:Pt) and [21] ($LaAlO_3$:$LaNiO_3$). In both cases, required switching voltage again rises up only as pulse widths are less than 100 ns, consistent with circuit induced *RC* delay time.

Before closing, we discuss the impact of this circuit effect on ever shrinking technology nodes. According to general capacitor theory, device capacitance scales down with device size, following $C \propto d^2$. Such relation is indeed beneficial in terms of extrinsic circuit delay. Although interconnect line resistance would increase as storage size builds up, it follows a weaker (linear) relation $R_l \propto N$, where $N \times N$ is memory size. To provide a rough estimation, we consider the state-of-the-art CMOS technology, for which the typical sheet resistance for metal conductor layers is 0.05 Ω/sq. For 1 Tbits ($10^6 \times 10^6$) memory, such interconnect line resistance reaches 0.05 Ω/sq $\times 10^6$ sq or 50 kΩ and a $100 \times 100\,nm^2$ cell capacitance is on the order of 0.1 fF (typically $C = 100$ pF for a $100 \times 100\,\mu m^2$ cell). Therefore, associated *RC* delay is as low as 5 ps, which would be trivial for a nanosecond memory device.

As for intrinsic switching time, we can conclude that it should be less than our measured lower limit 20 ns. Such bound is acquired from the best case ($2\,\mu m$ device) in Figure 3, which possesses the least capacitance and thus smallest *RC* time. It is currently difficult to make further conclusion regarding switching time because of experiment limit, but we believe intrinsic switching time is ultimately determined by electrons tunneling time within nanometer barrier, typically ~femtosecond. Such high speed is far beyond state-of-the-art electrical circuit limit (~picosecond) and thus not an issue for current electronic memory at all.

4. Conclusion

In conclusion, we have demonstrated and analyzed a switching-time independent electronic ReRAM. By shrinking the device dimension and thus its capacitance, switching voltage can maintain its intrinsic value within a wide range of 1 s to 20 ns and thus a low voltage yet ultra-fast device can be achieved. These results are applicable to other electronic ReRAM systems, which may shed light on future ultra-fast memory. Further advances in developing low voltage, fast switching materials may accelerate the adoption of highly integrated ReRAM in future generations of digital memory.

Competing Interests

The author declares having no competing interests.

References

[1] R. Waser, R. Dittmann, C. Staikov, and K. Szot, "Redox-based resistive switching memories-nanoionic mechanisms, prospects, and challenges," *Advanced Materials*, vol. 21, no. 25-26, pp. 2632–2663, 2009.

[2] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nature Nanotechnology*, vol. 8, no. 1, pp. 13–24, 2013.

[3] D. Ielmini, C. Cagli, and F. Nardi, "Resistance transition in metal oxides induced by electronic threshold switching," *Applied Physics Letters*, vol. 94, no. 6, Article ID 063511, 2009.

[4] S. Yu, Y. Wu, and H.-S. P. Wong, "Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory," *Applied Physics Letters*, vol. 98, no. 10, Article ID 103514, 2011.

[5] S. Menzel, M. Waters, A. Marchewka, U. Böttger, R. Dittmann, and R. Waser, "Origin of the ultra-nonlinear switching kinetics in oxide-based resistive switches," *Advanced Functional Materials*, vol. 21, no. 23, pp. 4487–4492, 2011.

[6] B. J. Choi, A. C. Torrezan, K. J. Norris et al., "Electrical performance and scalability of Pt dispersed SiO_2 nanometallic resistance switch," *Nano Letters*, vol. 13, no. 7, pp. 3213–3217, 2013.

[7] X. Yang, I. Tudosa, B. J. Choi, A. B. K. Chen, and I.-W. Chen, "Resolving voltage-time dilemma using an atomic-scale lever of subpicosecond electron-phonon interaction," *Nano Letters*, vol. 14, no. 9, pp. 5058–5067, 2014.

[8] S. B. Lee, A. Sangle, P. Lu et al., "Novel electroforming-free nanoscaffold memristor with very high uniformity, tunability, and density," *Advanced Materials*, vol. 26, no. 36, pp. 6284–6289, 2014.

[9] A. B. K. Chen, B. J. Choi, X. Yang, and I.-W. Chen, "A parallel circuit model for multi-state resistive-switching random access memory," *Advanced Functional Materials*, vol. 22, no. 3, pp. 546–554, 2012.

[10] X. Yang and I.-W. Chen, "Dynamic-load-enabled ultra-low power multiple-state RRAM devices," *Scientific Reports*, vol. 2, article 744, 2012.

[11] X. Yang, A. B. K. Chen, B. J. Choi, and I.-W. Chen, "Demonstration and modeling of multi-bit resistance random access memory," *Applied Physics Letters*, vol. 102, no. 4, Article ID 043502, 2013.

[12] X. Yang, Y. Lu, J. Lee, and I.-W. Chen, "Tuning resistance states by thickness control in an electroforming-free nanometallic complementary resistance random access memory," *Applied Physics Letters*, vol. 108, no. 1, Article ID 013506, 2016.

[13] A. Sawa, T. Fujii, M. Kawasaki, and Y. Tokura, "Interface resistance switching at a few nanometer thick perovskite manganite

active layers," *Applied Physics Letters*, vol. 88, no. 23, Article ID 232112, 2006.

[14] B. J. Choi, A. B. K. Chen, X. Yang, and I.-W. Chen, "Purely electronic switching with high uniformity, resistance tunability, and good retention in Pt-dispersed SiO_2 thin films for ReRAM," *Advanced Materials*, vol. 23, no. 33, pp. 3847–3852, 2011.

[15] X. L. Shao, L. W. Zhou, K. J. Yoon et al., "Electronic resistance switching in the Al/TiO_x/Al structure for forming-free and area-scalable memory," *Nanoscale*, vol. 7, no. 25, pp. 11063–11074, 2015.

[16] L. Wei, G. Q. Li, and W. F. Zhang, "Light-induced new memory states in electronic resistive switching of NiO/NSTO junction," *Journal of Physics D: Applied Physics*, vol. 49, no. 4, Article ID 045101, 2015.

[17] X. Yang, B. J. Choi, A. B. K. Chen, and I.-W. Chen, "Cause and prevention of moisture-induced degradation of resistance random access memory nanodevices," *ACS Nano*, vol. 7, no. 3, pp. 2302–2311, 2013.

[18] X. Yang, "Focus ion beam-induced mechanical stress switching in an ultra-fast resistive switching device," *Applied Physics A: Materials Science & Processing*, vol. 122, no. 6, article 587, 6 pages, 2016.

[19] X. Yang, *Resistance switching devices based on amorphous insulator-metal thin films [Ph.D. dissertation]*, University of Pennsylvania, 2014.

[20] A. B. K. Chen, *Size-dependent metal-insulator transition in Pt-dispersed SiO2 thin film: a candidate for future non-volatile memory [Ph.D. thesis]*, University of Pennsylvania, a candidate for future non-volatile memory, 2011, PhD dissertation.

[21] Y. Wang, *Alloy perovskite oxide thin film as resistance switching non-volatile memory [Ph.D. dissertation]*, University of Pennsylvania, 2009.