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Research Article

Carbon Nanotubes-Based Digitally Programmable Current Follower

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The physical constraints of ever-shrinking CMOS transistors are rapidly approaching atomistic and quantum mechanical limits. Therefore, research is now directed towards the development of nanoscale devices that could work efficiently in the sub-10 nm regime. This coupled with the fact that recent design trend for analog signal processing applications is moving towards current-mode circuits which offer lower voltage swings, higher bandwidth, and better signal linearity is the motivation for this work. A digitally controlled DVCC has been realized using CNFETs. This work exploited the CNFET's parameters like chirality, pitch, and numbers of CNTs to perform the digital control operation. The circuit has minimum number of transistors and can control the output current digitally. A similar CMOS circuit with 32 nm CMOS parameters was also simulated and compared. The result shows that CMOS-based circuit requires 418.6 μW while CNFET-based circuit consumes 352.1 μW only. Further, the proposed circuit is used to realize a CNFET-based instrumentation amplifier with digitally programmable gain. The amplifier has a CMRR of 100 dB and ICMR equal to 0.806 V. The 3 dB bandwidth of the amplifier is 11.78 GHz which is suitable for the applications like navigation, radar instrumentation, and high-frequency signal amplification and conditioning.

1. Introduction

CMOS technology is predominantly serving the electronics industry for the last 40 years. MOS device dimensions have already reached the nanometer regime. CMOS technology scaling suggests that this technology is nearing fundamental physical limits [1–3]. Therefore, researchers are looking for the emerging devices which can overcome the issues of CMOS. As the transistor size approaches sub-10 nm regime, short channel effects and source- (S-) drain (D) tunneling occur, posing a challenge in the further scaling of MOS [1, 4].

The carbon nanotube field effect transistor (CNFET) is one of the most promising devices among emerging technologies like Tunnel Field Effect Transistor (TFET), Single Electron Transistor (SET), and Nanowire Field Effect Transistor (NWFET) to extend the conventional silicon MOSFET technology. CNFETs exhibit similar functionality to their silicon MOSFET and are compatible with existing CMOS technology [5–9]. As the characteristics of a CNFET are superior to bulk CMOS, new design methodologies must be established. There has been substantial work going on for the development of the CNFET-based model for the performance estimation. CNFET has a potential to overcome the challenges of present CMOS technology. The performance results of CNFET-based circuits are good enough to overcome the bulk CMOS [5, 10]. The near ballistic transport properties and band structure of CNTs make them better channel materials for high-speed and low-power electronics. The CNFET has higher drive current, higher carrier mobility, higher transconductance, and better control over the channel [11].

The introduction of digital control to the current-mode circuit enhanced the functionality since last few years. The digital control also adds reconfigurability and enhances the performance of the circuit [12–15]. The transistors can be switched on/off by digital word inputs. Also, precise control of current gain is achieved using the digital control approach. A digital controlled CMOS voltage gain amplifier (VGA) was proposed which was used a digitally programmable current conveyor [12]. Additionally, CMOS-based digitally

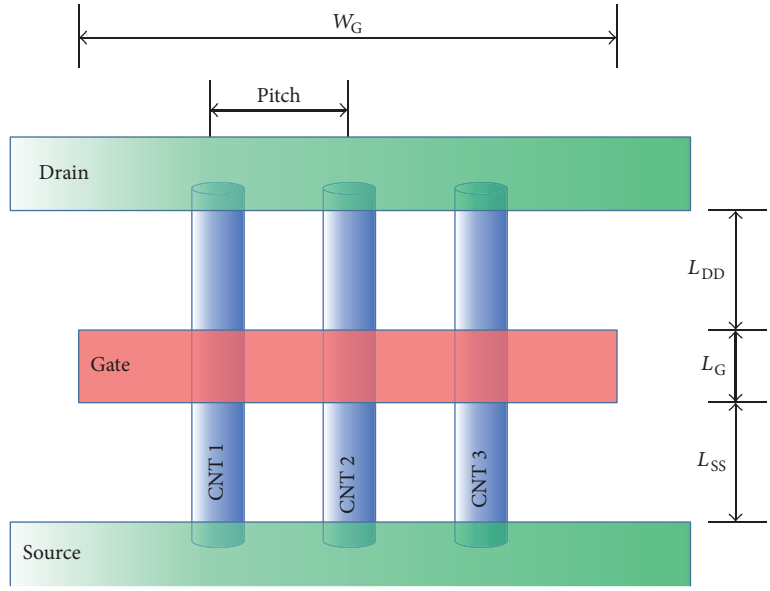

Figure 1: Top view of a CNFET with three CNTs.

programmable current conveyor II has been utilized to control the current of $Z+$ terminal [13]. In addition to this, the technique of [14] used current division cell (CDC) to realize the digitally programmable current follower (DP-CF). Moreover, a digitally controlled transconductor is realized with DDCC and R-2R ladder network [15]. This technique is novel but requires a large number of passive components. All these techniques use CMOS technology for the design of digital control block.

In this work, CNTs are utilized which have very high drive current, less scattering, and near ballistic transport of charge carriers [16]. The feature of the carbon nanotube is explored by which the drain current in a transistor is controlled by the number of CNTs in the channel. This property can be utilized to design a digitally controlled current conveyor. It enhances the operability and flexibility of the current conveyor block. The proposed method uses multiple CNTs to increase the drain current of the transistor. After that, this digital control approach is used to implement an instrumentation amplifier with programmable gain which can be useful in navigation and radar instrumentation systems.

This work is organized in the following order. A digitally programmable DVCC has been illustrated in Section 2. Section 3 deals with the realization of a programmable gain instrumentation amplifier. At last, Section 4 provides the conclusion.

2. Brief Overview of Carbon Nanotube-FET

The carbon nanotube (CNT) has been introduced as a key component for present nanoscale circuit design. Apart from their extensive use in chemistry, biotechnology, material science, and so on, CNFETs have also outperformed the conventional MOSFETs for high performance and low-power circuits, as carbon nanotube electronics offers higher current capability, higher transconductance, and ballistic operation in 1D structure [25, 26]. A simplified top view of CNFET with three-carbon nanotube is shown in Figure 1. Carbon nanotube field effect transistors (CNFETs) have semiconducting single-walled carbon nanotubes (CNTs) as a channel material and show enormous potential as extensions to the silicon MOSFETs.

The CNTs are classified into three types, based on the chiral vector (m, n). A CNT is known as zigzag, if $m = 0$ or $n = 0$. If $m \neq n$ and nonzero, CNT is said to be the chiral type, and if $m = n$, CNT is called armchair, as depicted in Figure 2.

The essential design parameters of carbon nanotube-FET are number of CNTs in transistor channel (N), internanotube space called pitch (S), and diameter of carbon nanotube (D_{CNT}). The gate length and width are illustrated as L_{gate} and W_{gate}, respectively [27, 28]. The CNT's diameter (D_{CNT}) and threshold voltage (V_{th}), the width of CNFET-based transistor (W), number of CNTs in channel (N), inter-CNT spacing (S), and energy gap ($\sum g$) are related by

$$\begin{aligned} D_{CNT} &= \frac{a\sqrt{n^2 + m^2 + nm}}{\pi}, \\ V_{th} &= \frac{aV_\pi}{qD_{CNT}\sqrt{3}}, \\ W &= (N-1) * S + D_{CNT}, \\ \sum g &= \frac{0.84\,\text{eV}}{D_{CNT}}. \end{aligned} \tag{1}$$

Here, terms m and n are the indices of chiral vector of graphene lattice and $a = 2.49$ Å (lattice constant). Also, q is electronic charge and $V_\pi = 3.033$ eV is the carbon π-π bond energy.

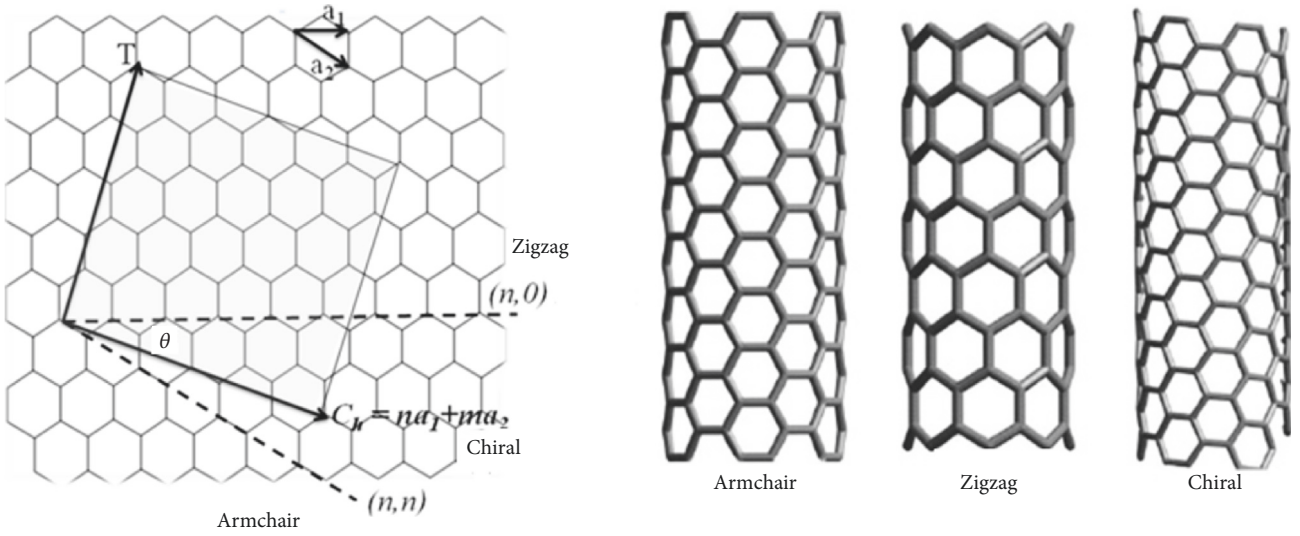

Figure 2: Illustration of chiral vector in a carbon nanotube.

There are some distinct features of CNFET which make it a promising candidate for high efficient electronics circuit design which are summarised as follows:

(1) It possesses high carrier mobility (10^3–10^4 cm^2/V-s) in CNTs which gives high on current (1 mA/μm).

(2) CNFET provides long scattering mean free path (approximately 1 μm) outcomes with lower delay and less heating. The elastic scattering means free paths in a CNT (1D structure) are long which results in a quasi-ballistic transport of charge carrier. Thus CNFET offers very high-speed switching.

(3) It has high thermal conductivity (1700–3000 W/mK) and chemical stability which results in high current density (approx. 10^{10} A/cm^2). The CNT can conduct heat nearly as well as Diamond or Sapphire.

(4) The band gap of CNFET is directly affected by its diameter. So the band gap can be tuned.

(5) The property of easy integration with high-K dielectric material leads to better gate electrostatics.

(6) Because of the miniaturized dimensions of the CNTs, the CNFET switches have lesser power than a conventional Si-based device.

(7) CNFET exhibits excellent matching of (complimentary) N- and P-type CNFETs with the equal sizes having same carrier mobility which gives similar drive currents. It is very beneficial in the prospects of transistor sizing of complex electronic circuits.

(8) As N-type and P-type CNFETs can be fabricated with the same size, this reduces the chip area in actual circuit implementation, whereas, in the case of MOSFET, the PMOS transistor is kept approximately three times wider than NMOS.

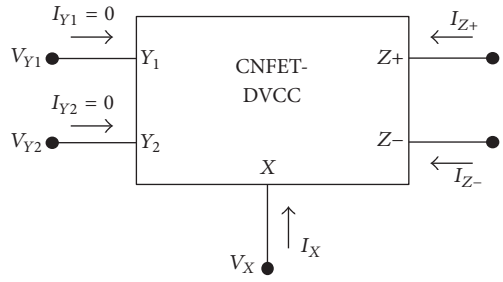

Figure 3: Circuit symbol of DVCC [17].

3. Digitally Programmable Differential Voltage Current Conveyor (DPDVCC) Using CNFET

The differential voltage current conveyor (DVCC) is proved to be a versatile active element for the realization of current-mode (CM) and voltage-mode (VM) circuits. Various applications like filters, oscillators, analog computation, and so on have been discussed [17, 21, 29–31]. The symbol of DVCC is depicted in Figure 3, and port relations are given in (2). In the proposed work, a CNFET-based differential voltage current conveyor has been used for digital control as shown in Figure 4.

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix}. \quad (2)$$

In the CMOS-based digital control techniques [12, 13, 18] the additional stages of transistors are added to Z terminal of the current conveyor to get the increased current with X terminal that can be controlled by the digital word. For getting current two times of I_X, the width of the transistors

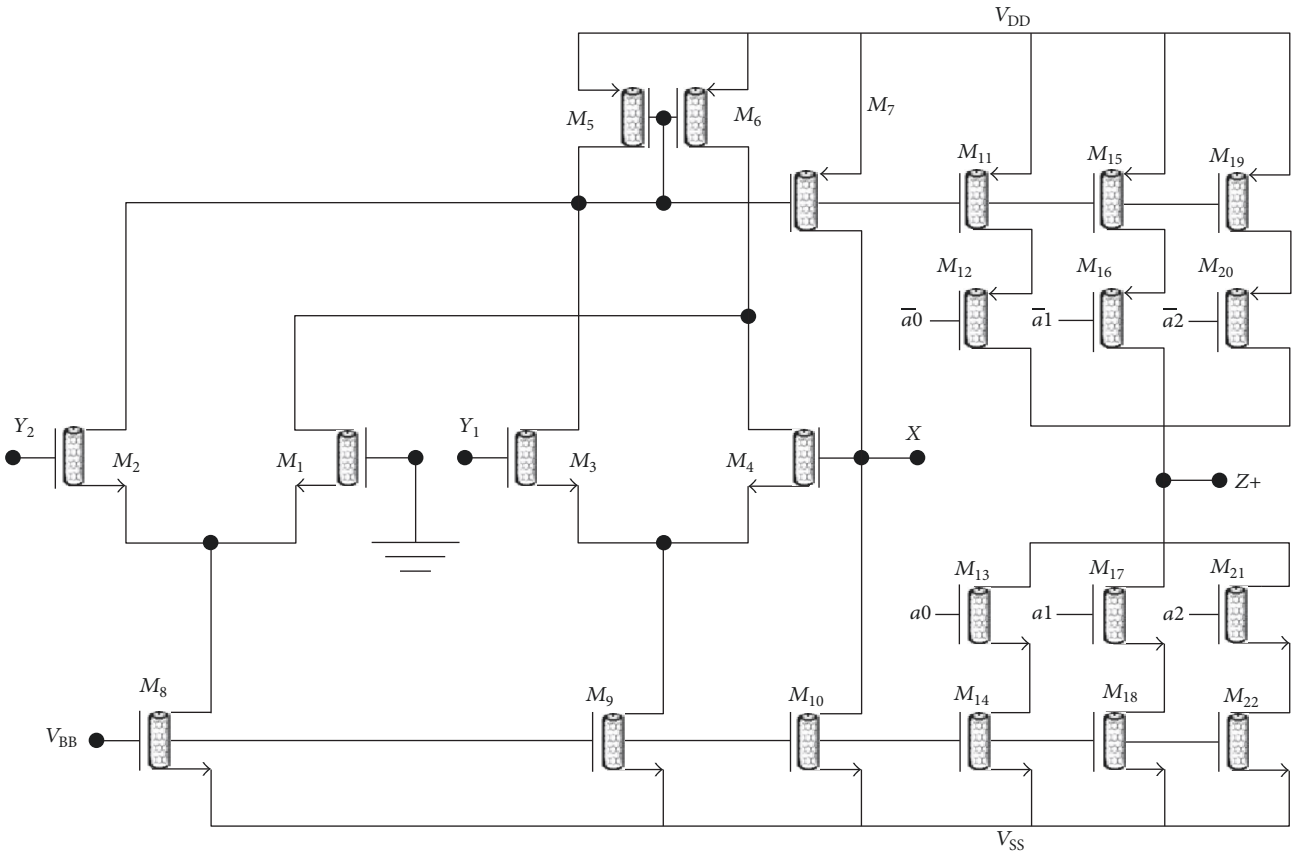

Figure 4: CNFET-based digitally programmable differential voltage current conveyor with only $Z+$ node.

is increased by two times, and for $4I_X$ current the width of transistors should be four times. It means that transistors must be of different sizes for a current conveyor. The designing of such kind of circuits could be complex for layout implementation. The transistors and passive components with minimum variability are always desirable. Regarding chip fabrication, the mask and layout designs of similar size transistors are comparatively easier than different sized transistors.

From the literature review, no earlier work is reported till date for digital control application using CNFET. So, Table 1 shows the comparison of proposed CNFET-based implementation with CMOS-based implementation for digital control application. It has been observed from Table 1 that the proposed circuit has lesser number of transistors compared to related existing work. Moreover, the proposed circuit is also simulated with CMOS 32 nm technology. The CMOS-based circuit has 418.6 μW power consumption whereas CNFET circuit consumes 352.1 μW. It reflects that CNFET-based implementation has better performance in terms of power than CMOS-based implementation.

The feature of the proposed circuit is to use the transistors of the same size for the active device, that is, DVCC. In CNFET transistor, drain current can be controlled by the number of CNTs in the channel. The width of CNFET could be constant by adjusting the number of tubes (N) and pitch (S) (see (3)). An n-channel CNFET has been simulated to plot

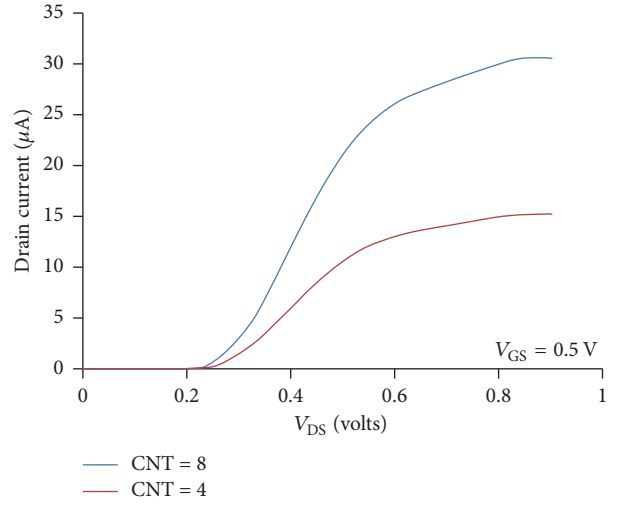

Figure 5: Dependence of drain current with number of CNTs of an n-channel CNFET.

the V-I curve with changing the number of CNTs. It is found that the drain current is raised double as the number of CNTs increased twice in the channel. For example, the drain current is measured as 15 μA for four CNTs in the channel and it is increased to 30 μA for eight CNTs for the same value of V_{GS} and V_{DS} as shown in Figure 5.

Table 1: Comparison of various digital control techniques for a 3-bit digital control word.

Reference	Device	Model	V_{DD}	Transistors	Aspect ratio
[18]	CCCII	0.25 μm CMOS	±5.0 V	44	Different
[13]	CCII	0.25 μm CMOS	±0.75 V	32	Different
[19]	FDCC	0.5 μm CMOS	±1.5 V	44	Different
[20]	DVCC	0.5 μm CMOS	±1.25 V	32	Different
This work	*DVCC*	*32 nm CNFET*	*±0.9 V*	*22*	*Constant*

Table 2: Dimensions of all transistors of Figure 4.

Transistor	Length (L)	Width (W)	Number of CNTs	Pitch
M_1–M_{14}	32 nm	226.5 nm	4	75 nm
M_{15}–M_{18}	32 nm	226.5 nm	8	32.14 nm
M_{19}–M_{22}	32 nm	226.5 nm	16	15 nm

It means we can double the current by changing the number of tubes in a carbon nanotube-FET. But, in the CMOS-based design, generally, the width of the transistor is increased to enhance the drain current for fixed V_{GS} and V_{DS}. But multifinger configurations can also increase the drain current without changing width. In this work, CNTs are utilized as the channel region of the transistor. In CNFET-based design width of the transistors can be kept constant by adjusting the pitch and number of CNTs. In Figure 4, transistors stage (M_1–M_{14}) has four CNTs. The width of transistors has been calculated as 226.5 nm as per (3) with consideration of pitch 75 nm for this stage.

Further, to double the current in next stage (M_{15}–M_{18}), number of CNTs should be double, that is, eight. The pitch of CNFET should be such that the width of CNFET will be 226.5 nm. To keep all transistors of same size, the pitch for the stage (M_{15}–M_{18}) has been calculated as 32.14 nm. Similarly, stage (M_{19}–M_{22}) contains sixteen CNTs, and the pitch has been calculated to be 15 nm, keeping the width of CNFET constant. The width of transistor stages (M_1–M_{14}), (M_{15}–M_{18}), and (M_{19}–M_{22}) has been calculated as (4), (5), and (6) respectively. Thus, in all the stages, widths of transistors are same. The dimensions of transistors used in Figure 4 are given in Table 2.

$$W = (N - 1) * S + D_{CNT}, \tag{3}$$

$$W = (4 - 1) * 75\,\text{nm} + 1.5\,\text{nm};$$
$$W = 226.6\,\text{nm}, \tag{4}$$

$$W = (8 - 1) * 32.14\,\text{nm} + 1.5\,\text{nm};$$
$$W = 226.6\,\text{nm}, \tag{5}$$

$$W = (16 - 1) * 15\,\text{nm} + 1.5\,\text{nm};$$
$$W = 226.6\,\text{nm}. \tag{6}$$

In this work, the carbon nanotubes (CNTs) in the channel of the transistor are used to increase the drain current of a CNFET. This feature is utilized for the digitally programmable current conveyor/follower. Thus drain current

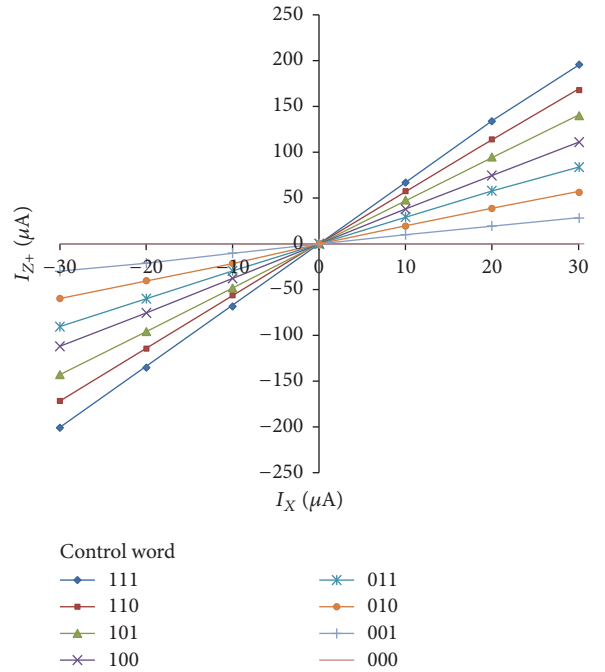

Figure 6: Transfer characteristic of digitally programmable DVCC with control word.

can be controlled by the number of CNTs for a digital control stage. Here, the control of drain current depends on the diameter and number of CNTs in a carbon nanotube-FET. The multifinger configuration MOSFET can also be used but it increases the overall transistor area. Transistors with multiple fingers have the disadvantage that the current direction is different for two neighboring fingers. For example, if for the first finger the source is to the left, the source for the second finger will be to the right. The properties of the transistor can change depending on the current direction. There should be careful efforts which are required to be exerted while trying to achieve good matching.

Further, DC and AC analysis of the proposed digitally programmable differential voltage current conveyor (DPDVCC) have been performed with SPICE simulation. The current transfer characteristic and frequency response of DPDVCC have been shown in Figures 6 and 7, respectively.

Moreover, voltage swing is also an important parameter for the performance assessment of the proposed active block. The voltage swing is the difference between maximum output voltage and minimum output voltage. The output voltage never exceeds these limits for given supply voltages V_{CC} and

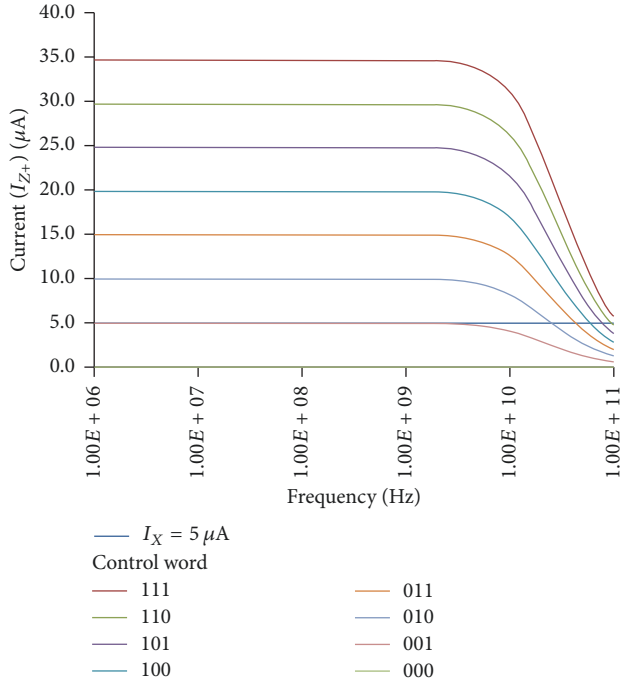

Figure 7: Frequency response of digitally programmable DVCC with control word.

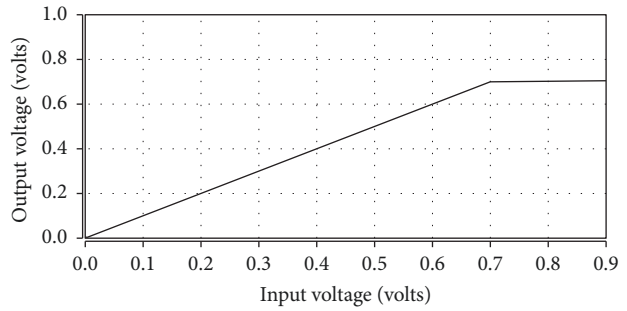

Figure 8: Illustration of output voltage swing.

V_{SS}. In the proposed circuit, the input voltage is applied from 0 to 0.9 V and the output voltage swing is obtained as 0 to 0.7 V as shown in Figure 8. Moreover, the voltage swing depicts how close the amplifier's output can be driven rail-to-rail under the defined operating conditions in which the amplifier can operate correctly. Also, the provision of voltage output swing is to find out the value of current where the amplifier is sinking or sourcing. The lesser the output short circuit current is, the nearer the amplifier will swing to the rail. The voltage output swing ability of an amplifier is dependent on the load current and output stage design of the amplifier.

The current (I_Z) has been digitally programmed by digital word (a_2, a_1, a_0). Table 3 illustrates the on/off state of the transistors (M_{12}–M_{13}, M_{16}–M_{17}, M_{20}–M_{21}) to understand the digital control operation.

It is imperative to describe the transistor sizing and mobility issue in CMOS and CNFET. While in CMOS, the transistor sizing is governed predominantly by the unequal mobility of the dominant carriers of the NMOS and PMOS transistors (leading to PMOS transistors turning out to be larger than the NMOS ones in a typical design), the CNFET technology alleviates this requirement of unequally sized transistors. This is attributed to the fact that the carrier mobility in the two types of CNFETs is equal. Second, from the layout and fabrication perspective, it is easier to design the mask and layout of the equal sized transistors. However, it is not necessary to keep transistors of the same width.

Table 3: Digital control bits in DPDVCC.

a_2	a_1	a_0 (n)	Transistors (on)	Transistors (off)	Current (I_Z+)
0	0	0	None	$M_{12,13,16,17,20,21}$	0
0	0	1	$M_{12,13}$	$M_{16,17,20,21}$	I_X
0	1	0	$M_{16,17}$	$M_{12,13,20,21}$	$2I_X$
0	1	1	$M_{12,13,16,17}$	$M_{20,21}$	$3I_X$
1	0	0	$M_{20,21}$	$M_{12,13,16,17}$	$4I_X$
1	0	1	$M_{12,13,20,21}$	$M_{16,17}$	$5I_X$
1	1	0	$M_{16,17,20,21}$	$M_{12,13}$	$6I_X$
1	1	1	$M_{12,13,16,17,20,21}$	None	$7I_X$

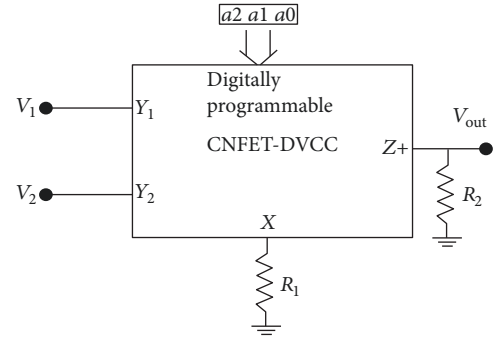

Figure 9: Instrumentation amplifier with programmable gain.

4. Instrumentation Amplifier Based on Digitally Programmable DVCC

A typical instrumentation amplifier is provided with differential input voltages, multiplies it with gain, and gives a single-ended output, suitable for use in measurement and test equipment [32, 33]. The basic circuit of instrumentation amplifier has been extensively configured using three Op-Amps, but here it is implemented by only one CNFET-based differential voltage current conveyor [21], which could work efficiently for voltage-mode as well as current-mode circuit applications.

The concept of digital controlling is used to program the gain of the instrumentation amplifier digitally. The proposed circuit of Figure 9 utilizes the digitally programmed DVCC (DPDVCC) to control the gain, instead of using resistors to control the gain of the amplifier as discussed [22–24]. The current I_Z+ of the DPDVCC circuit is responsible for this action because it is digitally programmed by transistors stage (M_{11}–M_{22}). The voltage transfer curve of the amplifier circuit

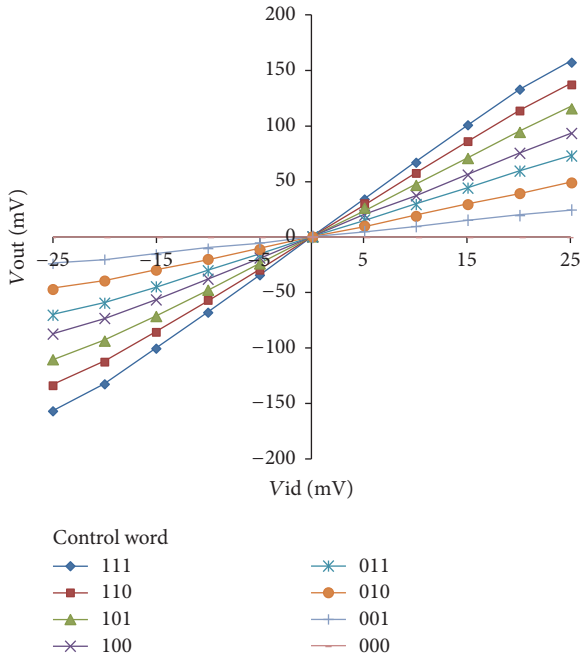

Figure 10: Transfer characteristic of instrumentation amplifier.

Table 4: Digital control bits for instrumentation amplifier.

a_2 a_1 a_0 (n)	000	001	010	011	100	101	110	111
Gain	0	1	2	3	4	5	6	7

is illustrated in Figure 10. The gain of the instrumentation amplifier is controlled by digital word (a_2 a_1 a_0) which has been depicted in Table 4.

$$V_{\text{out}} = n * (V_1 - V_2) \frac{R_2}{R_1}. \tag{7}$$

The performance of CNFET-based instrumentation amplifier is tested with HSPICE simulations keeping $R_1 = R_2 = 1\,\text{K}\Omega$ and control word (n) being varied (000–111). The output voltage of the instrumentation amplifier is calculated by relation (7). The frequency response of instrumentation amplifier is shown in Figure 11. A comparative study of current-mode instrumentation amplifiers with CMOS and CNFET (this work) is given in Table 5.

The 3 dB bandwidth of instrumentation amplifier is approximately 11.78 GHz. Figure 12 presents the 3 dB and unity gain bandwidth of the amplifier. The large bandwidth of the CNFET-based amplifier is mainly because the intrinsic capacitance of CNFET is less than MOSFET. Another reason behind higher bandwidth is the significant increase in the transconductance of CNFET as parallel CNTs improve the driving capability of the device. In the proposed circuit transistors use multiple CNTs in the channel region. Moreover, the 3 dB current and voltage bandwidths improve slightly with the increase in inter-CNT pitch, current per tube gets raised for the higher pitch. Further, in the application areas like navigation, radar instrumentation, and so on, the instruments operate simultaneously over different frequency bands within the 160 MHz to 18 GHz range. Therefore, there is a desire to have the higher bandwidth in such kind of applications. The proposed CNFET-based circuit has the very wide bandwidth to operate at these frequencies and thus is suitable for the above-mentioned application. The performance parameters like CMRR, ICMR, and unity gain bandwidth of the instrumentation amplifier have been measured using SPICE simulation and illustrated in Table 6. Further, the results show that it has 3 dB bandwidth up to 11.78 GHz as compared to 85 MHz reported in literature [21].

Moreover, the input common-mode range of the instrumentation amplifier is measured as 0.806 V and presented in Figure 13. The common-mode rejection ratio (CMRR) is also an important parameter which is calculated through SPICE simulation as given in Figure 14. The CMRR of the CNFET-based instrumentation amplifier is 100 dB. The higher the CMRR, the higher the ability of an IA to reject common-mode signals [33].

4.1. Nonideal Analysis of Instrumentation Amplifier. The output voltage of the instrumentation can be calculated by relation (7). The performance of the DVCC-based instrumentation amplifier (IA) differs from ideal behaviour because the voltage and current conveying actions are not exact, thus leading to degradation in performance in the DVCC-based IA. Therefore, to account for nonideal analysis, two parameters α and β are considered. The performance will be affected by considering nonideal analysis.

$$V_X = (V_1 - V_2). \tag{8}$$

The voltage of terminal X is expressed by (8) but, after the consideration of β, voltage V_X is written as (9). Further, current I_X is described in terms of input voltages (10). The current I_Z is depicted by (11) with the current gain α (X to Z terminal) and control word n. Finally, output voltage is expressed by (12).

$$V_X = (\beta_1 V_1 - \beta_2 V_2), \tag{9}$$

$$I_X = \frac{(\beta_1 V_1 - \beta_2 V_2)}{R_1}, \tag{10}$$

$$I_Z = n * \frac{\alpha(\beta_1 V_1 - \beta_2 V_2)}{R_1} \quad \text{as } I_Z+ = n * I_X, \tag{11}$$

$$V_{\text{out}} = n * \alpha(\beta_1 V_1 - \beta_2 V_2) \frac{R_2}{R_1}. \tag{12}$$

Here, β_1 and β_2 are the voltage transfer gains from input terminals Y_1 and Y_2, respectively, to the X terminal. α is the current transfer gain from X node to Z node [34]. Further, $\alpha = 1 - \epsilon_i$ and $\beta = 1 - \epsilon_j$, where ϵ_i and ϵ_j denote the current and voltage tracking errors of the DVCC. The transfer gains (α, β) deviate unity by the current and voltage tracking errors, which are quite small and technology dependent.

5. Conclusion

This paper presents a digitally programmable DVCC (DPDVCC) which is useful to control of the output current

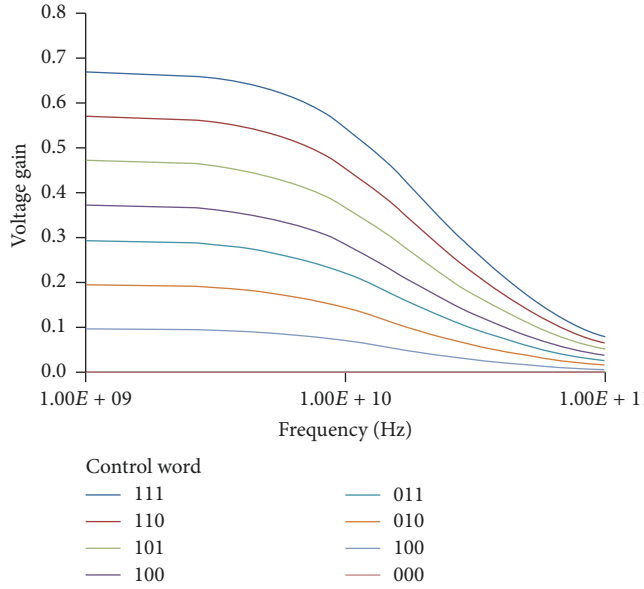

Figure 11: Frequency response of the instrumentation amplifier with digital word.

Table 5: Comparative study of current-mode instrumentation amplifiers.

Reference	Model	Device	V_{DD}	Transistors	Bandwidth
[21]	0.25 μm CMOS	DVCC	±1.5 V	32	85 MHz
[22]	0.35 μm CMOS	CCCII	±3.3 V	28	70 MHz
[23]	CMOS/BJT	CCII	–	26	2.97 MHz
[24]	CMOS/BJT	CCII	–	>26	1.2 MHz
This work	32 nm CNFET	DVCC	±0.9 V	22	11.78 GHz

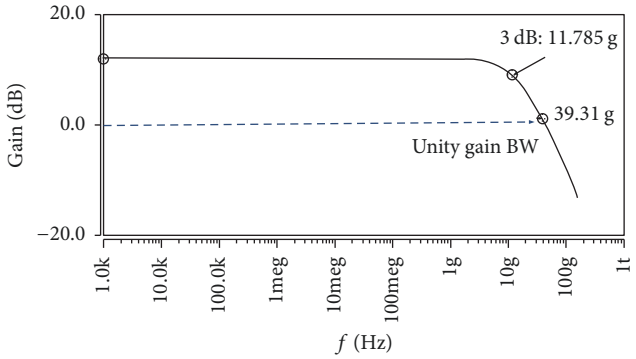

Figure 12: Representation of 3 dB and unity gain bandwidth of the amplifier.

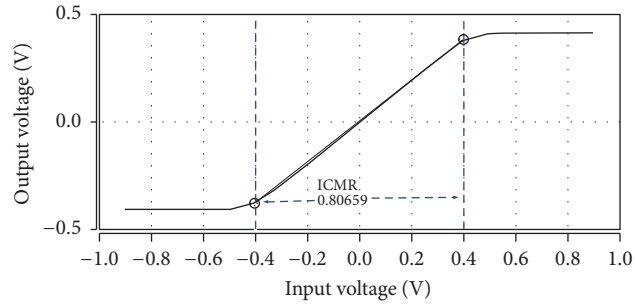

Figure 13: Input common-mode range of the amplifier.

Table 6: Performance parameters of the instrumentation amplifier.

Parameter	Value
ICMR	0.806 V
CMRR	100 dB
Unity gain BW	39.31 GHz
3 dB BW	11.78 GHz

digitally. The proposed CNFET-based circuit has equal sized and lesser transistors to realize the DVCC with binary bits control. Additionally, a wide-band instrumentation amplifier has been introduced whose gain can be controlled digitally as it utilizes the DVCC block with binary control for its design. The 3 dB bandwidth is observed as 11.78 GHz as compared to 85 MHz obtained by existing CMOS-based design. Extensive simulations are performed to study and verify all aspects of the circuits. The obtained results are quite good to be used in the futuristic CNFET-based circuit design.

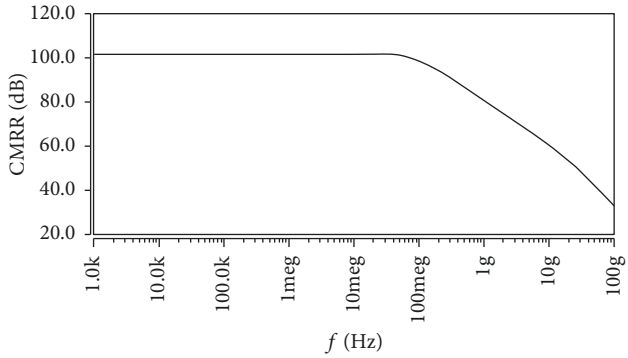

Figure 14: Illustrating CMRR versus frequency of the amplifier.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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