

## Review Article

# Fault Handling Methods and Comparison for Different DC Breaker Topologies and MMC Topologies of the HVDC System

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The HVDC system has many significant benefits and is widely used around the world. The protection of HVDC system is always an issue, which should be solved. This paper presents the working principle of different protection schemes. The advantages and disadvantages of these protection schemes are also introduced. In order to solve the HVDC fault, two protection strategies are proposed. One design focusses on the topologies of the HVDC breaker in the HVDC line, such as all-solid HVDC breaker, resonant HVDC breaker, and hybrid HVDC breaker. The other design is from the viewpoint of converter topology, which has two types. One type generates the counter-emf in arms, such as full bridge MMC, hybrid MMC, and clamp-double MMC. The other type cuts off the current path from the AC side to the DC side, which is also introduced in this paper. Some performances of these topologies are compared, such as switching time and efficiency.

## 1. Introduction

Recently, the HVDC system became of more concern because it can increase power efficiency compared to the traditional AC transmission. Conventional HVDC systems are equipped with current source converters (CSC), which use thyristors. In recent years, voltage source converters have become widely used and many promising topologies have been created and developed. Two-level and three-level VSCs have been installed since the 2000s, and the modular multilevel converters (MMC) [1, 2] have also been put to practical use since 2010. Compared with CSC, the VSC has advantages in control characteristics and reduction of ac filters.

However, compared to the AC system, there is no zero crossing of current in the transmission lines. When the fault occurs in the AC line, the mechanical switches can be opened at the time point of zero crossing of the AC current. The HVDC system does not have this kind of ability. In order to solve this problem and protect the HVDC system, many methods are proposed.

There are two main ways to protect the HVDC system. The first way uses different circuit breakers in the HVDC line in order to cut off the fault current. There are three types

of circuit typologies: all-solid HVDC breakers [3], resonant HVDC breakers [4], and hybrid HVDC breakers [5].

The second way of HVDC protection is from the viewpoint of converter topologies. It is well known that half bridge MMC has many advantages, but one main disadvantage is that it has no ability to cut off the fault current. Hence, many MMC submodule topologies are developed based on the half bridge MMC, such as full bridge SMs [6] and clamp-double SMs [7]. Because the modified SMs have more losses during normal operation, the hybrid MMC is considered [8]. This second method has two types. The first type is the topologies in [6–8]. These topologies can store rest energy in the capacitors in SMs and the arms build up the counter-emf; then the current is cut off. The second type is the topologies in [9, 10]. These topologies cut off the energy flow between AC and DC sides and the rest energy is consumed in the designed loop. Their structures are introduced in following section.

The performance of methods such as switching time and efficiency are also compared in this paper. According to the results, the new topology in [10] has good performance, which has lower loss than most topologies and short switching time.

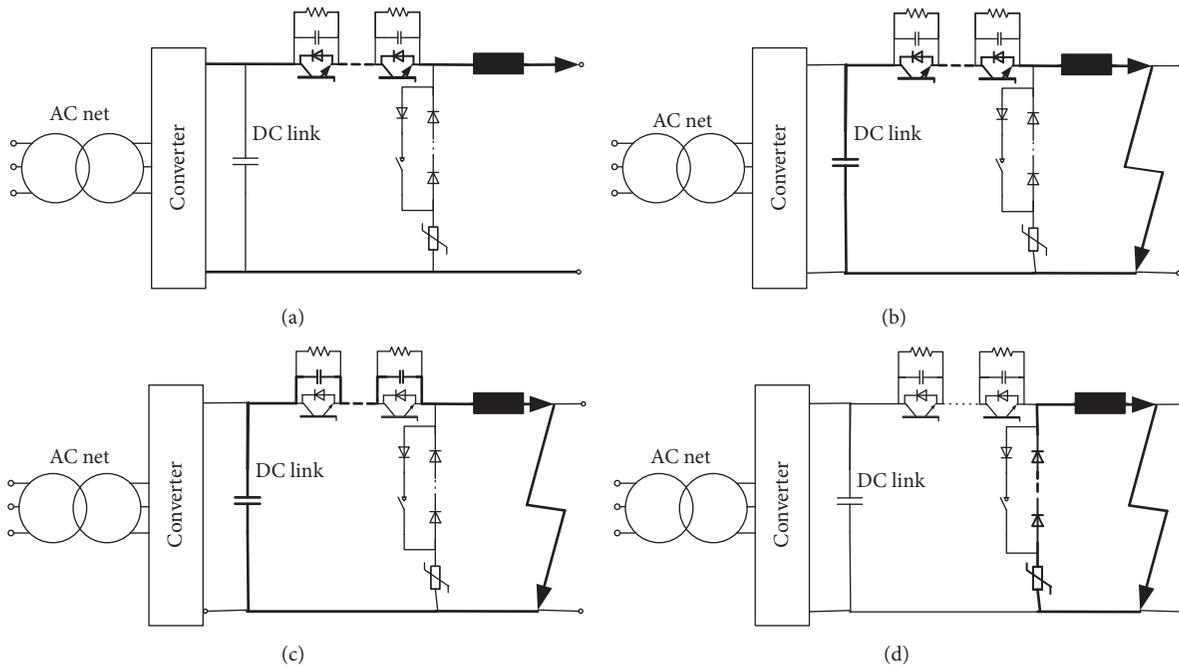


FIGURE 1: Structure and working principle of all-solid HVDC breaker (1st type). (a) Normal operation of all-solid HVDC. (b) Short circuit fault occurs. (c) The paralleled capacitor of each IGBT is charged through the loop. (d) The rest energy is consumed in the designed loop.

## 2. HVDC Breakers

This section introduces three types of HVDC breakers. For each type, there are several corresponding topologies. Advantages and disadvantages will be discussed. The performances will also be compared.

**2.1. All-Solid HVDC Breaker.** In [3], one kind of all-solid HVDC breaker is proposed, which is shown in Figure 1(a). In Figure 1(a) the sending end of the HVDC system is indicated and the IGBTs are connected in series in the HVDC line. When the fault current is detected Figure 1(b), all IGBTs are blocked. The paralleled capacitor of each IGBT is charged through the loop (Figure 1(c)), when the current of the HVDC breaker decays to zero, the rest energy will be consumed in the designed loop (Figure 1(d)).

Because the switching time of this HVDC breaker is very fast, almost equal to the switching time of IGBTs, the over current is low. During normal operation, all IGBTs in the HVDC line have conduction loss, so the total loss of this HVDC breaker is fairly large. The calculation will be shown later.

In [11], another kind of all-solid HVDC breaker is developed (Figure 2(a)), whose principle is different from the topology in Figure 1. As shown in Figure 2, the thyristors are connected in series in the HVDC line. After the fault, the C-L loop is triggered and the anticurrent is generated in the designed loop, Figure 2(b). When the current in thyristors is zero, all thyristors can be turned off (Figure 2(c)). At last, C will be charged again and the fault current can be cut off.

Compared to the first type, the switching of the HVDC breaker in [11] is slower, because the thyristors must be cut

off when the current decays to zero. However, during normal operation, the loss of thyristors is lower than IGBTs in the first type when the same number of devices is used in HVDC line.

**2.2. Resonant HVDC Breaker.** One kind of resonant HVDC breaker is proposed in [4], whose structure is shown in Figure 3. During normal operation, the DC current flows through the mechanical switches. When the fault current is detected, the vacuum switches receive a command to break. When the contacts in the vacuum switches start to separate, the current in one of the switches will commutate to its parallel diode and will flow through a plasma in another vacuum switch.

After a short delay (0.5 ms) [12], the thyristor of the current pulse generator is triggered and a current pulse flows through the pulse generator branch and the two external MOVs. The current in the vacuum switch still flows through the plasma and then reverses and the current commutates to its parallel diode at the created zero crossing. Both vacuum switches are turned off. After separation, the remaining energy of the line inductances must be absorbed. The input current will continue to flow to recharge the capacitor  $C_{PG}$  until the arrester  $VDR_{PG}$  becomes conductive.

Another kind of resonant HVDC breaker is developed in [13] (Figure 4). When the fault occurs (Figure 4(a)), the full bridge MMC submodule is triggered and an anticurrent is generated in the mechanical switch (Figure 4(b)). A current zero crossing is generated in order to open the mechanical switch. After the separation, the thyristor is conducted and the capacitor in the full bridge MMC submodule is charged again (Figure 4(c)). In fact, the FBSMs can be connected in series as shown in Figure 4(d), which means that the surge



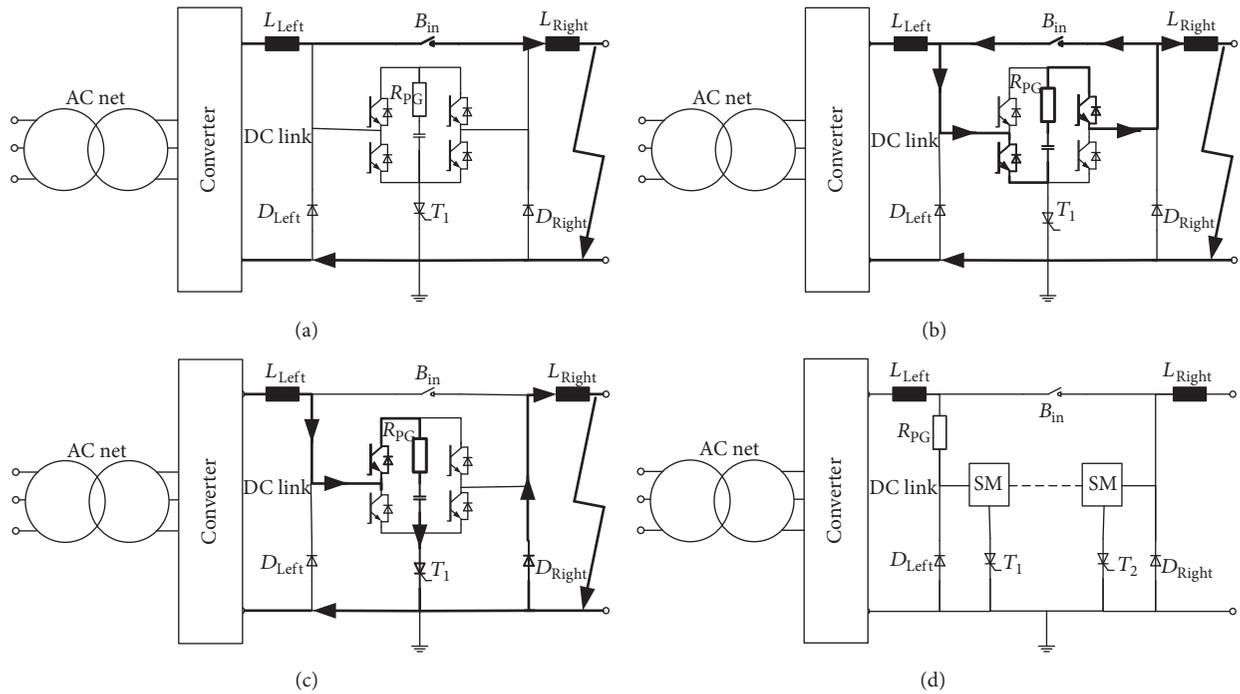


FIGURE 4: Structure of resonant HVDC breaker (2nd type). (a) The fault occurs. (b) The full bridge MMC submodule is triggered and an anticurrent is generated in the mechanical switch. (c) The mechanical switch is separated. The thyristor is conducted and the capacitor in the full bridge MMC submodule is charged again. (d) The FBSMs can be connected in series to change surge current.

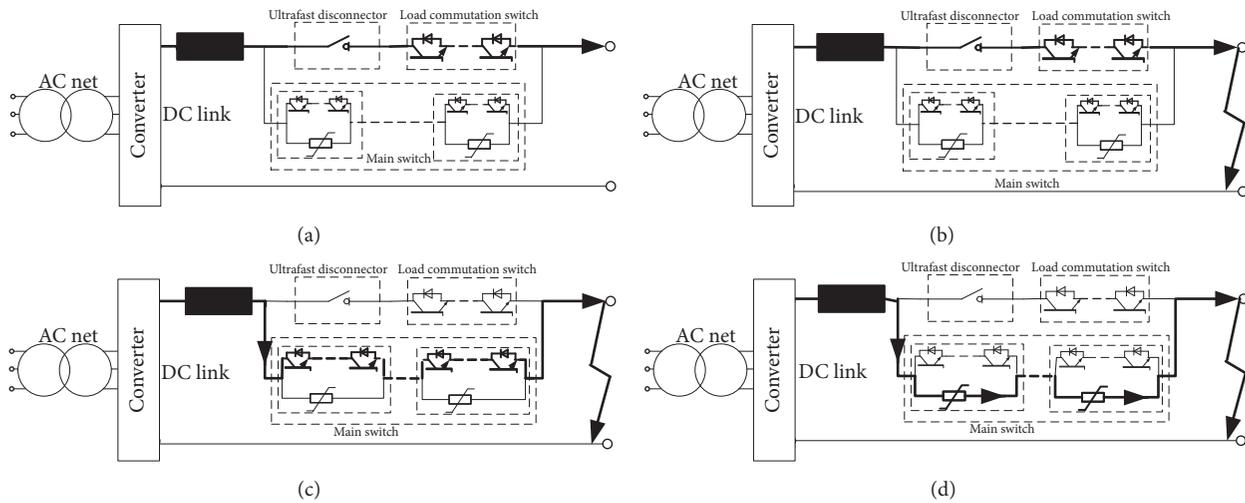


FIGURE 5: Structure and working principle of hybrid HVDC breaker. (a) Normal operation of hybrid HVDC breaker. (b) Short circuit fault occurs and LCS is blocked. (c) Fault current commutates to main switch and UFD is turned off. (d) IGBTs in main breaker are blocked and fault current commutates to arrestors' branch.

When the fault occurs, LCS is blocked and the fault current commutates to the IGBTs in the main switch (Figure 5(c)). If there is no current flowing through the UFD, it can be turned off. When UFD is separated, the LCS can be turned on.

The IGBTs in main switch can be turned off after the turning-off of UFD. The fault current will commutate to the arrestors of the main switch and the energy will be consumed by these arresters. At this point, the fault current can be cut off.

Compared to the all-solid HVDC breaker, the switching time of the hybrid HVDC is much slower because of the limitation of UFD.

The loss of the hybrid HVDC breaker is much lower than the all-solid HVDC breaker, but the number of IGBTs is almost the same because these IGBTs are needed to withstand the DC voltage in the end.

Compared to the resonant HVDC breaker, the hybrid HVDC breaker has longer switching time and higher loss,

TABLE 1: Number of semiconductor devices in different HVDC breaker topologies.

	All-solid HVDC breaker		Resonant HVDC breaker		Hybrid HVDC breaker
	1st type	2nd type	1st type	2nd type	
IGBTs	300	0	0	1200	300
Diodes	300	600	1200	600	0
Thyristor	0	600	300	600	0

because the hybrid HVDC breaker in [5] uses the high voltage UFD, whose opening time is longer than medium voltage vacuum tubes. For hybrid HVDC breaker, there is no plasma during the whole process, which means that the mechanical part of it has less stress than vacuum tubes in the resonant HVDC breaker.

The over current of this hybrid HVDC breaker depends on the switching time of UFD (2 ms). For large over current, the IGBTs in main breaker should be designed specifically. The cost of IGBTs is higher than it is for others.

**2.4. Comparison of HVDC Breakers.** In order to compare different HVDC breakers, the parameters of the HVDC system should be the same. It is assumed that the DC voltage is 300 kV, the rate DC current is 1200 A, and the DC reactor is 100 mH.

According to the structure of HVDC breakers, the needed semiconductor devices are summarized in the Table 1. It is assumed that each semiconductor device withstands 2 kV in different topologies in order to make the comparison of loss and efficiency. Because the HVDC breaker should be equipped in the sending end and receiving end, the number of devices should be doubled.

The number of semiconductor devices in Table 1 is rough, because some devices can be ignored. For example, the number of IGBTs in the load commutation switch is very low. According to [5], a matrix of  $3 \times 3$  IGBT positions for each current direction is chosen, which has little effect on the calculation result.

For all topologies, the IGBTs are chosen as FZ1200R45KL3B5 (4500 V, 1200 A), the diodes are chosen as DZI070N28K (2800 V, 1070 A), and the thyristors are chosen as T1930N32TOF VT (3200 V, 2180 A).

The operation loss of each HVDC breaker topology can also be calculated according to the datasheets of semiconductors. The results are shown in Table 2. The total loss of HVDC breakers in sending end and receiving end should be added together.

The over current of the HVDC breaker depends on the switching time of the HVDC breaker. According to the parameters of the HVDC system, the rise of the fault current is about 3 kA/ms. It is assumed that if the fault current increases by 20%, the fault current is detected. For the all-solid HVDC breaker, the turn-off time of IGBTs is about 1.7  $\mu$ s, and the incremental current after the detection is about 5 A, which can be ignored.

For resonant HVDC breakers, the switching time of medium voltage vacuum tubes is 0.5 ms and the increment of the current is about 1500 A. The maximum over current is about 3900 A. The semiconductor devices in resonant

TABLE 2: Conduction loss of different HVDC breakers topologies.

Topologies of different HVDC breakers	Estimated power loss
All-solid HVDC breaker	
1st type	990 kW (0.28%)
2nd type	268 kW (0.07%)
Resonant HVDC breaker	
1st type	0
2nd type	0
Hybrid HVDC breaker	12 kW (0.003%)

HVDCs can withstand this current for short duration and they do not need to cut off this current.

For the hybrid HVDC breaker, the switching time of UFD is 2 ms, so the over current could be about 7500 A, which means that the IGBTs in the main switch must have the ability to cut off this high over current. They should be designed specially.

According to the calculation and summary above, each type of HVDC breaker has advantages and disadvantages. From the view point of economy, the all-solid HVDC breaker has an extremely large hardware cost and cost of semiconductor loss.

The resonant HVDC breaker solves the problem of cost of semiconductor loss, but the second type has too large a hardware cost, which could never be considered for the usage of the HVDC system. The first type of resonant HVDC breakers has an appropriate cost of hardware, but as mentioned above, the serial connected vacuum tubes cannot have equal voltage after the separation. The technical problem needs to be solved first before the application.

The hybrid HVDC breaker also has an appropriate cost of hardware and semiconductor loss. According to [5], the fault can be cleared within 5 ms, but the over current is too large for normal IGBT to be turned off because of the large switching time of UFD, so the special IGBTs must be used; the extra cost cannot be ignored.

### 3. Modified MMC Topologies

This section introduces the modified MMC topologies, which have ability to cut off the fault current. The hardware cost and efficiency are also calculated. The modified MMC topologies have two types. The first type generates the counter-emf in arms and there is no current from AC side. The second type cuts off the current path from the AC side to the DC side.

**3.1. First Type.** The full bridge MMC submodule (FBSM) is the first modified MMC topology, which has the ability to cut

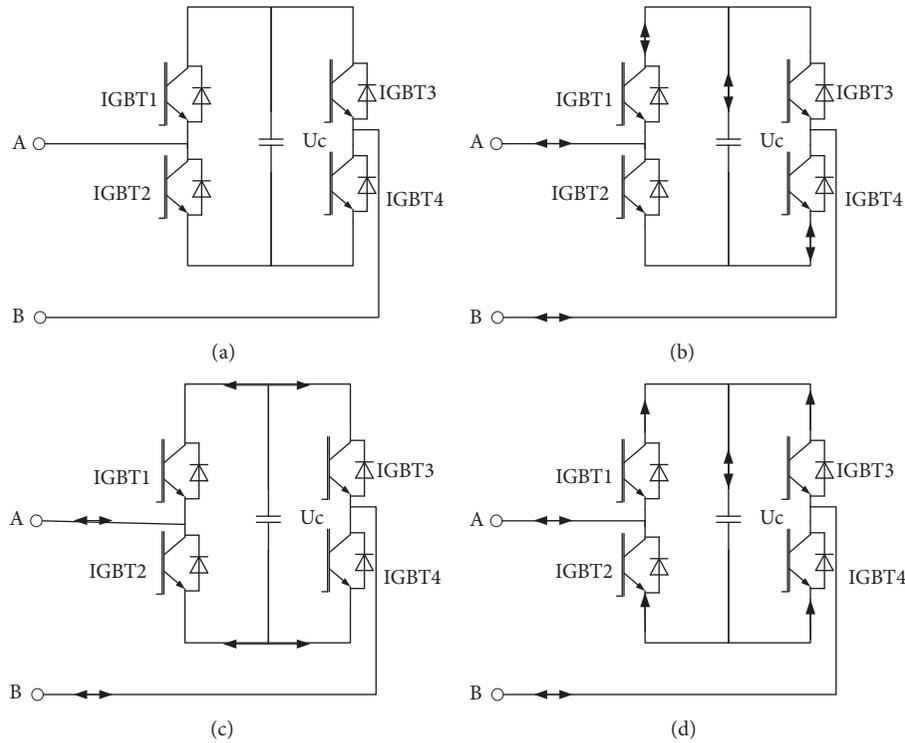


FIGURE 6: Structure and working process of FBSM. (a) Structure of FBSM. (b) FBSM is inserted. (c) FBSM is bypassed. (d) All IGBTs are blocked.

off the fault current. The structure and working principle of FBSM are shown in Figure 6.

During normal operation, if the FBSMs are inserted, the current flows through IGBT1 and IGBT4 (Figure 6(b)). If the FBSM is bypassed, the current flows through IGBT1 and IGBT3 or IGBT2 and IGBT4 (Figure 6(c)). When the fault occurs, all IGBTs in the FBSM are blocked. The current can just flow through IGBT1 and IGBT4 or IGBT2 and IGBT3 to charge the capacitor of the submodule until the counter-emf of arms is built up and the current is cut off (Figure 6(d)).

The structure and working principle of clamp-double SMs are shown in Figure 7. Each cell can be considered as two half bridge cells in series connection, with the additional semiconductors (IGBT5) kept in the on-state and diodes (diode 1 and diode 2) kept in the off-state during normal operation [12].

During normal operation, when both capacitors are inserted, the current flows through IGBT1 and IGBT4 (Figure 7(a)). When one of the capacitors is inserted, if IGBT1 and IGBT3 are turned on, the C1 is inserted; if IGBT2 and IGBT4 are turned on, the C2 is inserted (Figure 7(b)). If IGBT2 and IGBT3 are on-state, the SM is bypassed (Figure 7(c)). When the fault occurs, all IGBTs in the SM are blocked. If the current flows from A to B, the equivalent circuit is that two capacitors are connected in series and charged. If the current flows from B to A, the equivalent circuit is that two capacitors are connected in parallel and charged (Figure 7(d)). Then the counter-emf is built up and the fault current can be cut off.

Another kind of topology is the hybrid MMC, which consists of FBSMs and HBSMs. The number of each kind of SM

should be decided by hardware cost, cost of semiconductor loss, and fault ride through capability [14]. According to [14], in order to cut off the fault current, the blocking voltage must be at least equal to the AC phase-to-phase peak voltage. However, to reduce the fault current in an appropriate time, higher voltage ratings are needed. Hence, a scenario with a blocking voltage  $V_b = 1.2 \cdot V_{DC}$  is considered. To ensure this blocking voltage rating a minimum amount of full bridge cells  $n_{FB,min}$  is required in each MMC arm [14]:

$$n_{FB,min} = \frac{V_b}{2V_C} = \frac{0.6 \cdot V_{DC}}{V_C}. \quad (1)$$

$V_{DC}$  is the DC voltage of system;  $V_C$  is the voltage of SMs;  $V_b$  is blocking voltage.

For example, if the HVDC voltage is 300 kV, the SM voltage is 2 kV and the modulation index is 1. The number of FBSMs is 90 and the number of HBSMs is 60. In this case, the hybrid MMC has the ability of fault current blocking. The structure of the hybrid MMC is shown in Figure 8.

**3.2. Second Type.** The second type of MMC based topology can cut off the energy path from the AC side to the DC side, which is a relatively new method to protect the HVDC system. The first new method uses an extra IGBT in the submodule. The structure is shown in Figure 9 [9].

Generally, the pole-to-ground dc-link fault is more likely than the pole-to-pole dc-link fault. However, the pole-to-pole fault is more critical in the symmetrical monopole HVDC configuration, since the pole-to-ground fault may merely

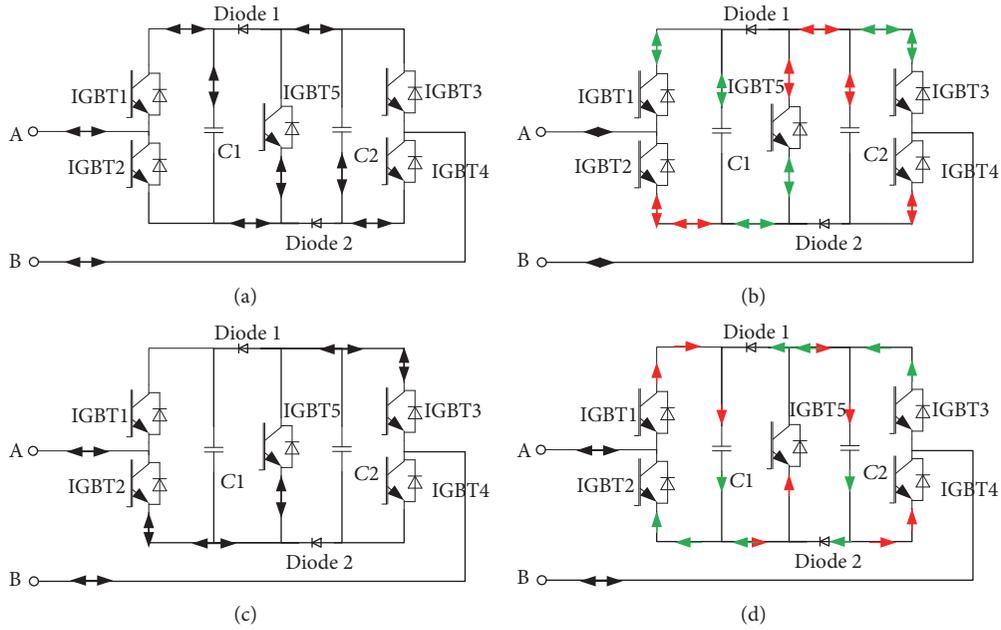


FIGURE 7: Structure and working process of clamp-double MMC. (a) Both capacitors are inserted. (b) One of the capacitors is inserted. (c) SM is bypassed. (d) All IGBTs are blocked.

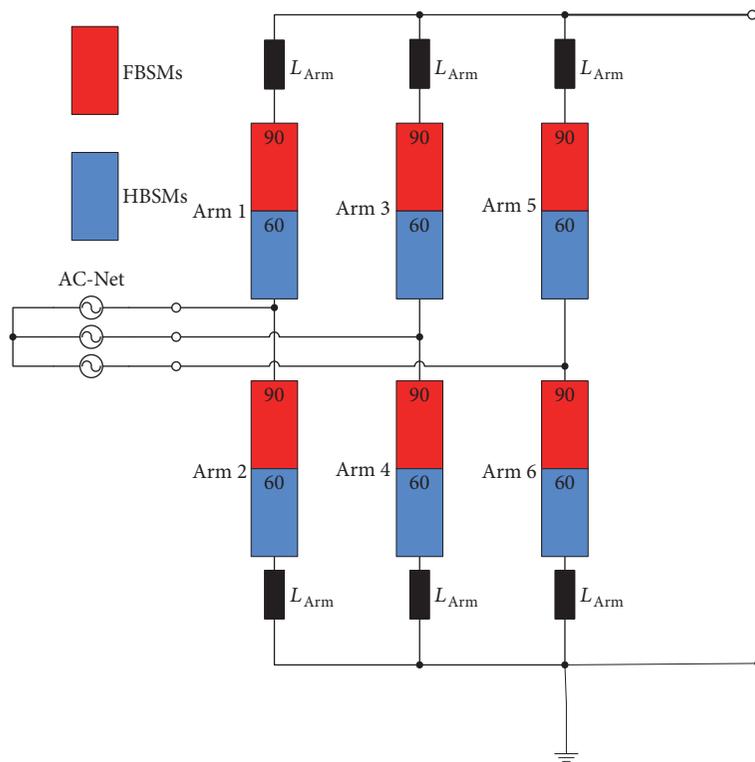


FIGURE 8: Structure of hybrid MMC ( $V_{DC} = 300$  kV,  $V_C = 2$  kV,  $M = 1$ ).

result in the overvoltage of one monopole. In other typical HVDC configurations, such as the asymmetrical monopole configuration and the bipolar configuration, the pole-to-ground fault is actually the same type as the pole-to-pole fault in the symmetrical monopole configuration [15]. Therefore,

the pole-to-pole dc-link fault in the symmetrical monopole configuration is the most representative dc-link fault and becomes the major concern in this part.

In Figure 9, there are a number of  $k$  SMs with extra IGBTs and there are a number of  $j$  SMs without extra IGBTs in each

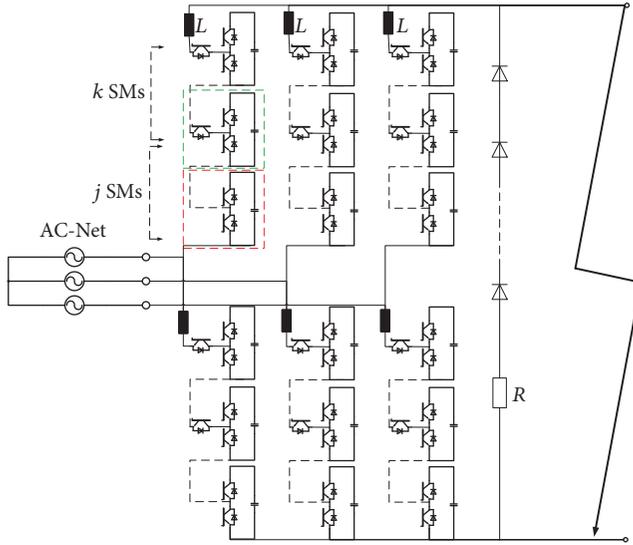


FIGURE 9: Structure of the first new topology.

arm. According to [9], in order to protect the extra IGBT, a snubber circuit is connected in parallel with this IGBT in the SM.

During normal operation, the extra IGBT in each SM is on-state. If the fault occurs, all IGBTs are blocked, including the extra IGBTs, so the current from the AC side to the DC side is cut off. The rest energy in the HVDC line will be consumed in the designed loop and the rest energy in arms will be stored in the snubber circuit in each SM with extra IGBT.

In order to ensure that the extra IGBTs can withstand the high voltage after the blocking, according to [9], the number of SMs with extra IGBTs should be determined as follows:

$$k > 0.39N. \quad (2)$$

$k$  is Number of SMs with extra IGBT in each arm;  $N$  is Number of SMs in each arm.

If the HVDC voltage is 300 kV, the SM voltage is 2 kV and the modulation index is one.  $N$  is equal to 150 and the minimum needed SM with extra IGBTs is 59.

The second new method is introduced in [10]. According to [10], the terminal of each HBSM is connected with a pair of anticonnected thyristors, which is shown in Figure 10. The structure of this new topology is shown in Figure 11.

During normal operation, these thyristors are off-state and the SMs work just like normal HBSMs. IGBT1s and IGBT2s are turned on.

The fault occurs at time  $t_1$  and after the short circuit fault is detected at time  $t_2$ , the thyristors in each submodule are turned on. The IGBT1s are all turned off at time  $t_3$  and the fault current flows through Arrester 1. At time  $t_4$  the current in the UFD decays to zero and the UFD can be turned off. After the switching time of the UFD, the IGBT2s in the freewheeling diodes are all turned off at time  $t_6$ ; the fault current in the DC line is commutated to the Arrester 2. The DC fault current will decay much faster after the IGBT2s are

TABLE 3: Parameters of HVDC system.

DC voltage of system $V_{DC}$	300 kV
DC current of system $I_{DC}$	1200 A
Number of cells per arm $n$	150
Power $P$	360 MW
AC line voltage $\hat{V}_{AC}$	150 kV
AC line current $\hat{I}_{AC}$	1600 A
AC grid frequency $f_N$	50 Hz
Angle between arm current and voltage $\varphi_i$	0
Voltage of each SMs $V_c$	2 kV
Modulation frequency $f_M$	50 kHz

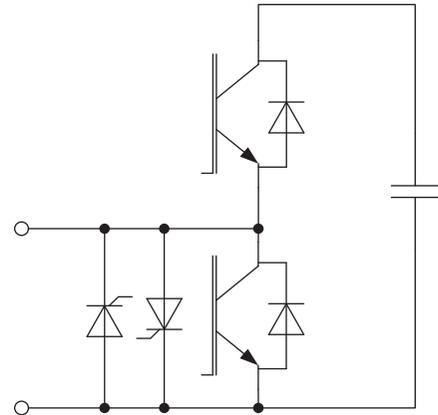


FIGURE 10: Topology of submodule of second method.

turned off. At time  $t_7$ , the DC fault decays to zero. The details are illustrated by current diagram in Figure 12.

In order to prove this new topology, the simulation results are shown in Figure 13, which is finished by SIMULINK. The parameters of the simulation are shown in Table 3.

As shown in Figure 13, when the fault distance  $L_{sc}$  increases, the decay time of fault current in HVDC line  $I_{DC,II}$  will also increase. However, the decay time of fault current  $I_{DC,I}$  in UFD will always be limited in a short period, which means that the UFD can be always opened in a short time. AC side and DC side can be separated quickly. The separation time is not affected by fault distance.

**3.3. Comparison of Different MMC Based Topologies.** In this section, different topologies are compared. The power loss and efficiency are considered. In order for different topologies to be compared, they should work in the same condition. Some important parameters are shown in Table 3.

The IGBTs, diodes, and thyristors are used in all topologies with the same models, which are the same as models in HVDC breakers (FZ1200R45KL3B5, DZ1070N28K, and T1930N32TOF VT).

For half bridge module multilevel converter (HB-MMC) and full bridge module multilevel converter (FB MMC), there are 150 SMs in each arm, so there are 900 SMs in the converter. If the inverter side and rectifier side are considered, the number of SMs should be doubled.

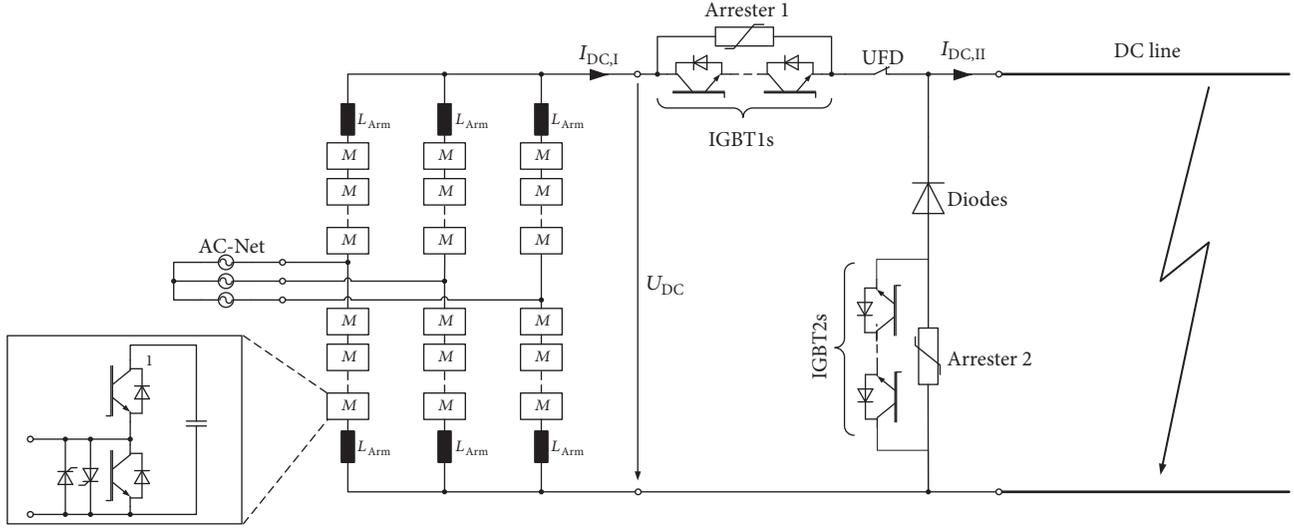


FIGURE 11: Structure of the second new topology.

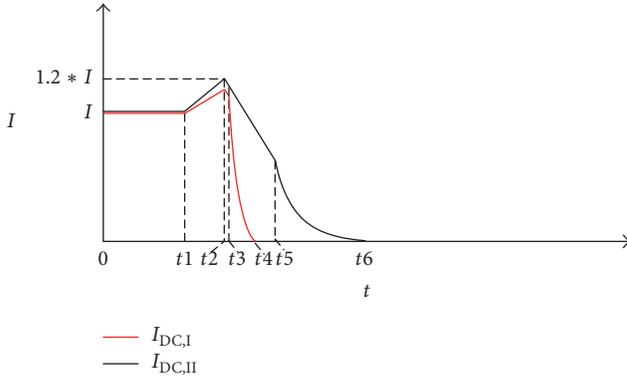


FIGURE 12: The diagram of DC current in the UFD and DC line in the modified HVDC breaker. ( $t_1$ : short circuit occurs;  $t_2$ : short circuit is detected, all thyristors are turned on, and MMC are blocked;  $t_3$ : IGBTs in the DC line are turned off;  $I_{DC,I}$  decrease faster;  $t_4$ : current in the UFD decays to zero;  $t_5$ : IGBT2s in the diodes branch are all turned off;  $t_6$ : current in the DC line decays to zero).

For clamp-double MMC (CD-MMC), one submodule is equivalent to two HBSMs. Therefore, there are 75 SMs in each arm.

For hybrid MMC (HY-MMC), as mentioned above, there are 90 HBSMs and 60 FBSMs in each arm.

The first new topology also has 150 SMs in each arm, but the extra semiconductor devices should be considered. There are 59 SMs that have extra IGBTs and 91 normal SMs in each arm.

The second new topology needs thyristors for each SM. It also needs extra IGBTs to withstand the voltage of arresters. The clamped voltages of Arrester 1 and Arrester 2 are set to be 10 kV. If each IGBT can withstand 2 kV, five IGBTs are needed for each arrester. The number of semiconductor devices in different topologies is summarized in Table 4.

The semiconductor loss can be calculated by the method in [16]. In [16] the average conduction loss and switching loss

TABLE 4: Number of semiconductors in different MMC topologies.

	IGBTs	Diodes	Thyristors
HB-MMC	3600	0	0
FB-MMC	7200	0	0
CD-MMC	4500	1800	0
HY-MMC	5760	0	0
1st new MMC	4308	300	0
2nd new MMC	3620	300	3600

of a half bridge cell are calculated. Based on the parameters in Table 3, the average loss of a half bridge cell is calculated, which is shown in Figure 14.

The conduction loss and switching loss of upper IGBT and diode are  $P_{ct1}$ ,  $P_{cd1}$ ,  $P_{st1}$ , and  $P_{sd1}$ . The conduction loss and switching loss of lower IGBT and diode are  $P_{ct2}$ ,  $P_{cd2}$ ,  $P_{st2}$ , and  $P_{sd2}$ . According to this result, the total loss of one converter can be calculated. With the same method, the loss of FBSM can also be attained, which is shown in Figure 15.

The conduction loss and switching loss from IGBT1 to IGBT4 in Figure 6 are indicated in Figure 14. The loss of IGBT1 is the same as IGBT4 and the loss of IGBT2 is the same as IGBT3. According to the result, the total loss of FB MMC can be calculated.

For the clamp-double MMC, if the modulation method is the same as HB-MMC, the conduction loss and switching loss of IGBTs should be the same; the extra loss is generated by the conduction loss of IGBT5 (Figure 7). The first new MMC has the same case, because the SMs with extra IGBTs also generate conduction loss during normal operation. The conduction loss of this kind of extra IGBTs and diodes can be calculated by the following equations [16]:

$$P_{ct} = \frac{1}{2\pi} \int_0^{2\pi} V_{CE}(i_{Arm,n}) \cdot i_{Arm,n} d\omega t, \quad (3)$$

$$P_{cd} = \frac{1}{2\pi} \int_0^{2\pi} V_F(i_{Arm,p}) \cdot i_{Arm,p} d\omega t, \quad (4)$$

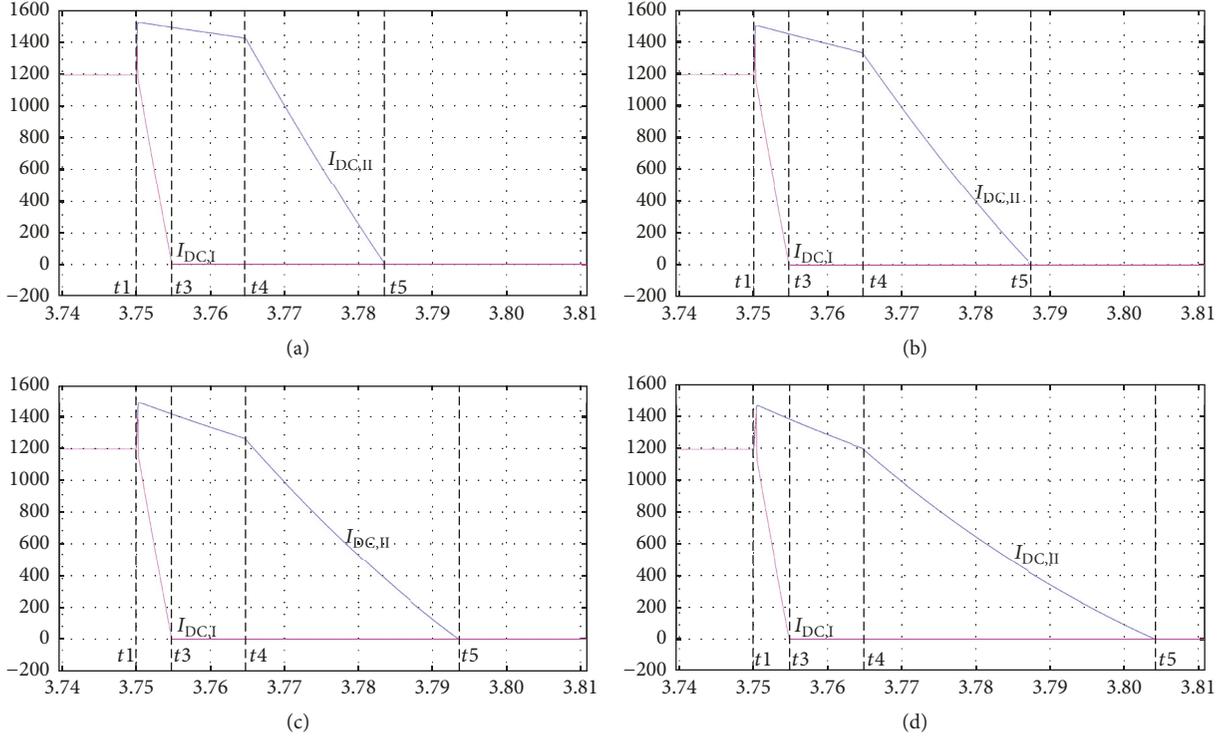


FIGURE 13: Decay time of the fault current in HVDC line with different fault location (second new topology). (a)  $L_{sc} = 20$  km,  $t_1 = 0$  s,  $t_3 = 4$  ms, and  $t_5 = 75$  ms. (b)  $L_{sc} = 50$  km,  $t_1 = 0$  s,  $t_3 = 4$  ms, and  $t_5 = 37$  ms. (c)  $L_{sc} = 100$  km,  $t_1 = 0$  s,  $t_3 = 4$  ms, and  $t_5 = 44$  ms. (d)  $L_{sc} = 200$  km,  $t_1 = 0$  s,  $t_3 = 4$  ms, and  $t_5 = 55$  ms.

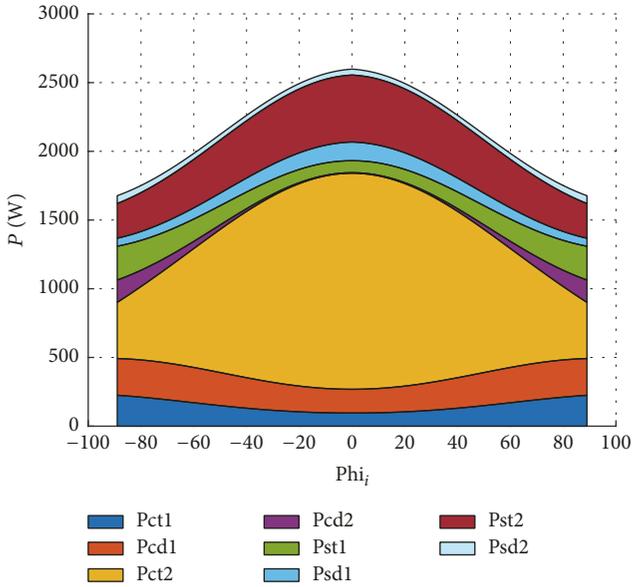


FIGURE 14: Average loss of devices in one cell in HB-MMC.

$$i_{Arm,p} = \begin{cases} i_{Arm} & \text{if } i_{Arm} > 0 \\ 0 & \text{else,} \end{cases} \quad (5)$$

$$i_{Arm,n} = \begin{cases} i_{Arm} & \text{if } i_{Arm} < 0 \\ 0 & \text{else.} \end{cases} \quad (6)$$

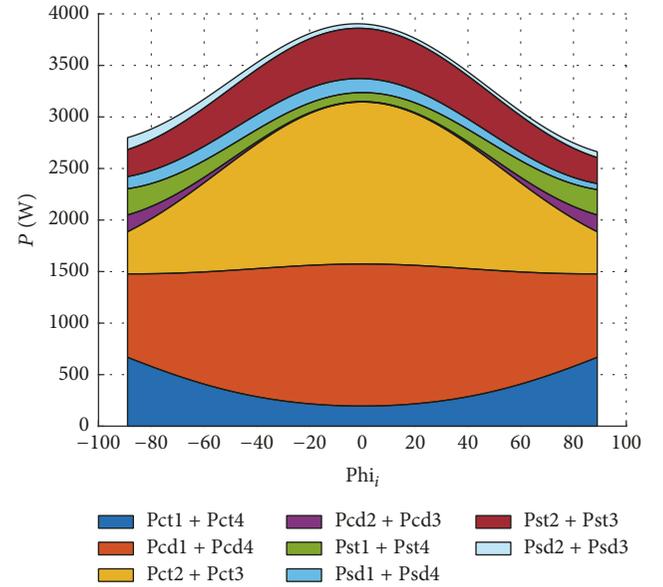


FIGURE 15: Average loss of devices in one cell in FB MMC.

$V_{CE}$  and  $V_F$  can be attained from equations as follows:

$$y = (a + b \cdot x^c) \cdot d. \quad (7)$$

The coefficients are shown in Table 5.

The conduction loss of one extra IGBT is shown in Figure 16.

TABLE 5: Coefficient for Equation (3).

$x$	$y$	$a$	$b$	$c$	$d$
$i_C$	$V_{CE}$	1 V	0.025 V	0.69	1
$i_F$	$V_F$	0.7 V	0.026 V	0.62	1

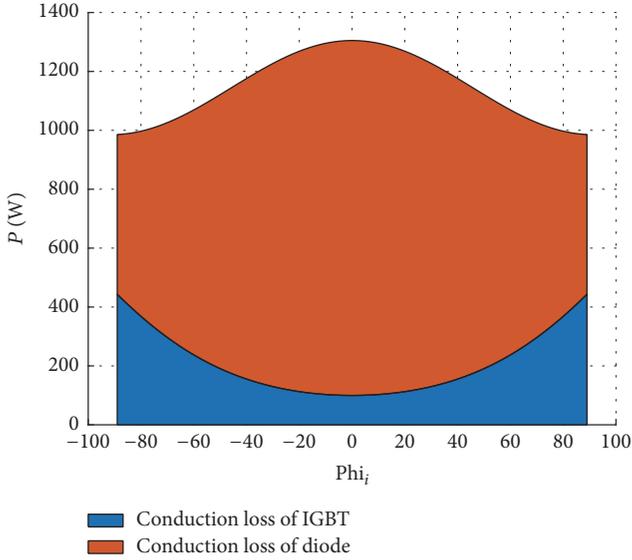


FIGURE 16: Average loss of extra IGBT and diode per cell.

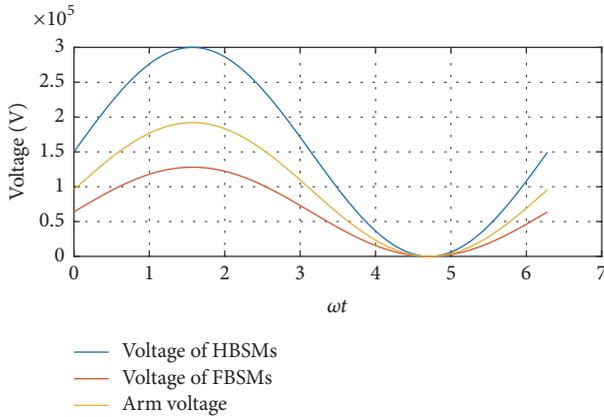


FIGURE 17: Voltage of HBSMs and FBSMs in one arm.

The loss of the hybrid MMC can also be attained with the method in [16]. Because the modulation index is one, the FBSMs can just output zero or  $V_c$ . In order to calculate the loss of FBSMs and HBSMs, the voltage of HBSMs and FBSMs should be attained first, which is shown in the voltage diagram in Figure 17. As mentioned above, the number of HBSMs is 60 and the number of FBSMs is 90.

The loss of one arm in the hybrid MMC is shown in Figure 18, which includes 60 HBSMs and 90 FBSMs.

For the second new topology, there is no extra loss during normal operation. The loss is generated by IGBTs in the HVDC line, which can be easily calculated.

According to the calculation above, the efficiency of different MMC topologies can be summarized and the final

TABLE 6: Power loss and efficiency of different topologies.

	Power loss (kW)	Efficiency
HB-MMC	4676.4	98.70%
FB-MMC	7025.4	98.05%
CD-MMC	5850.9	98.37%
HY-MMC	6488.4	98.19%
1st new MMC	5600.3	98.44%
2nd new MMC	4710.0	98.69%

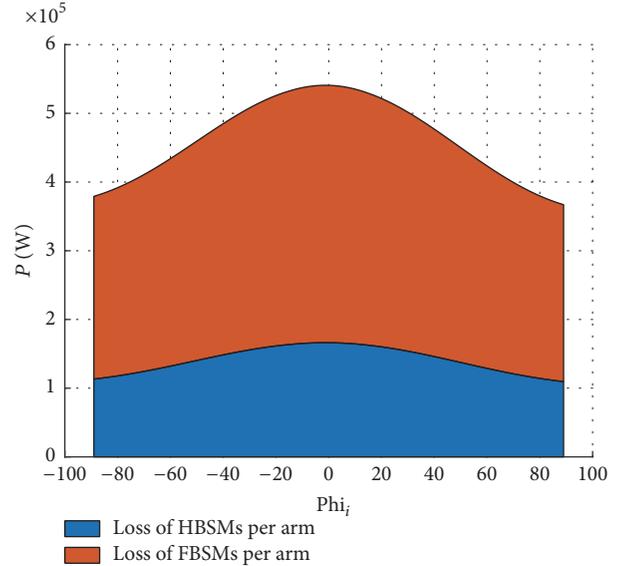


FIGURE 18: Loss of all HBSMs and FBSMs per arm in hybrid MMC.

result is shown in Table 6. The inverter and rectifier sides are both considered, so the power loss should be doubled. It is assumed that the angle between arm current and arm voltage is zero.

The power loss of the second new method has extraordinarily low power loss compared to other MMC topologies. In the long term, the second new MMC has more advantages than other topologies.

The power loss of different HVDC breaker and modified MMC topologies are shown in Tables 2 and 6. It is assumed that the different HVDC breakers are equipped for the HB-MMC; the total loss and the efficiency of both main methods can be compared; the results are shown in Figure 19.

#### 4. Conclusion

In this paper, different HVDC fault handling methods are discussed and compared. It is assumed that the HVDC breakers are used for half bridge MMC. According to the final results, most HVDC breakers with HB-MMC have less power loss than modified MMC topologies, because the HVDC breakers are independent from the converter, and the modified MMC topologies have to change the structure of each submodule, whose amount is extremely large in each converter; even the all-solid HVDC breaker has lower power loss than some

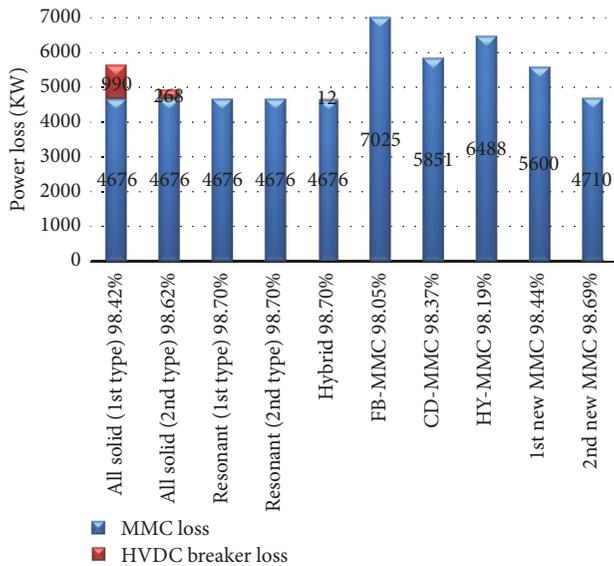


FIGURE 19: Total loss and efficiency of different HVDC and modified MMC.

modified MMC. However, the modified MMC topologies can overcome most disadvantages of HVDC breakers and some modified MMC topologies have extra functions. For example, the full bridge MMC and hybrid MMC can realize over modulation. The selection of the fault handling method should not just depend on the economy; sometimes the fault handling method and the converter should be considered together.

## Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

## References

- [1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proceedings of the 2003 IEEE Bologna PowerTech Conference*, pp. 272–277, Italy, June 2003.
- [2] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC '08)*, pp. 174–179, IEEE, Rhodes, Greece, June 2008.
- [3] K. Sano and M. Takasaki, "A surgeless solid-state DC circuit breaker for voltage-source-converter-based HVDC systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2690–2699, 2014.
- [4] Y. Wang and R. Marquardt, "A fast switching, scalable DC-Breaker for meshed HVDC super-grids," in *Proceedings of the Int. Exhibition and Conf. for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*, 2014.
- [5] J. Häfner and B. Jacobson, "Proactive Hybrid HVDC Breakers—A key innovation for reliable HVDC grids," in *The electric power system of the future - Integrating supergrids*

and microgrids International Symposium in Bologna, Bologna, Italy, 2011.

- [6] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385–394, 2015.
- [7] R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-bus-applications," in *Proceedings of the 2010 International Power Electronics Conference - ECCE Asia -, IPEC 2010*, pp. 502–507, Japan, June 2010.
- [8] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1137–1146, 2014.
- [9] T. H. Nguyen and D.-C. Lee, "Protection of the MMCs of HVDC transmission systems against DC short-circuit faults," *Journal of Power Electronics*, vol. 17, no. 1, Article ID JPE 17-1-24, pp. 242–252, 2017.
- [10] X. Jiang and M.-M. Bakran, "A new protection scheme for HVDC circuit based on MMC topology with controllable fault current," in *Proceedings of the 18th European Conference on Power Electronics and Applications, EPE 2016 ECCE Europe*, Germany, September 2016.
- [11] J.-Y. Kim, S.-S. Choi, and I.-D. Kim, "A new reclosing and re-breaking DC thyristor circuit breaker for DC distribution applications," *Journal of Power Electronics*, vol. 17, no. 1, Article ID JPE 17-1-27, pp. 272–281, 2017.
- [12] S. Norrga, X. Li, and L. Angquist, "Converter topologies for HVDC grids," in *Proceedings of the 2014 IEEE International Energy Conference, ENERGYCON 2014*, pp. 1554–1561, Croatia, May 2014.
- [13] J. Krishnan, H. Gueldner, K. Handt, and S. Nielebock, "A modular bi-directional hybrid circuit breaker for medium and high voltage DC networks," in *Proceedings of the 18th European Conference on Power Electronics and Applications, EPE 2016 ECCE Europe*, Germany, September 2016.
- [14] V. Hofmann and M.-M. Bakran, "Optimized design of a hybrid-MMC and evaluation of different MMC topologies," in *Proceedings of the 18th European Conference on Power Electronics and Applications, EPE 2016 ECCE Europe*, Germany, September 2016.
- [15] International Electrotechnical Commission, "High-voltage direct current (HVDC) transmission using voltage sourced converters (VSC)," IEC TR-62543, 2011.
- [16] A. Schoen, A. Birkel, and M.-M. Bakran, "Modulation and Losses of Modular Multilevel Converters for HVDC Applications," in *PCIM Europe*, vol. 22, Nuremberg, Germany, 2014.



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