Hindawi Publishing Corporation
Advances in Condensed Matter Physics
Volume 2011, Article ID 258731, 8 pages
doi:10.1155/2011/258731

Research Article

From Coherent States in Adjacent Graphene Layers toward Low-Power Logic Circuits

Leonard F. Register, Dipanjan Basu, and Dharmendar Reddy

Department of Electrical and Computer Engineering, Microelectronics Research Center, The University of Texas at Austin, 10100 Burnet Road, Building 160, Austin, TX, 78758, USA

Correspondence should be addressed to Leonard F. Register, register@mer.utexas.edu

Received 31 May 2010; Accepted 19 August 2010

Academic Editor: Emanuel Tutuc

Colleagues and we recently proposed a new type of transistor, a Bilayer PseudoSpin Field Effect Transistor (BiSFET), based on many-body coherent states in coupled electron and hole layers in graphene. Here we review the basic BiSFET device concept and ongoing efforts to determine how such a device, which would be far from a drop-in replacement for MOSFETs in CMOS logic, could be used for low-power logic operation, and to model the effects of engineerable device parameters on the formation and gating of interlayer coherent state.

1. Introduction

The greatest roadblock to continued logic scaling is power consumption. Circuit heating can limit device density and clock frequencies beyond intrinsic device limits. Mobile device performance is limited by battery use. And it has been estimated that 7% of power consumption in the United States is already integrated circuit related [1]. Complementary metal-oxide semiconductor (CMOS) logic employing electron/n-channel and hole/p-channel metal-oxide field effect transistors (MOSFETs) has been the standard for many years. However, basic physics rather than technological limits now portend an "end of the roadmap"—referring in part to the International Technology Roadmap for Semiconductors (ITRSs) [2]—for CMOS scaling in the not too distant future. Specifically, thermionic emission of charge carriers over the gated channel barrier between the source and drain combined with the need for rapid switching appears to limit minimum supply voltages to 0.5 to 0.7 V at room temperature, and associated switching energies to a few aJ [2]. Of course, with this limit defined by thermionic emission, lower voltage and power operation would be possible at colder temperatures. However, for most conventional applications, logic or otherwise, a proposal for below room-temperature operation is a nonstarter. This need for continued scaling beyond the end of the roadmap for CMOS is motivating various efforts to produce transistors based on alternative switching mechanisms.

Of relevance to the subject of this special issue, colleagues and we recently proposed a new type of transistor, a Bilayer PseudoSpin Field Effect Transistor (BiSFET), based on many-body coherent states in coupled electron/n and hole/p type graphene layers [3]. Normally one does not associate coherent many-body states with room temperature. However, as a consequence of a synergy of graphene properties—a single atomic layer thick with nearly perfect electron-hole symmetry in the band structure, a low density of states and zero band gap—it has recently been predicted that this condensate might occur above room temperature in otherwise weakly coupled and oppositely charged graphene double/bilayer systems [4]. Under appropriate conditions, the predicted temperature for coherence could extend to slightly above $0.1E_F/k_B$ where E_F is the magnitude of the Fermi energy relative to the Dirac point [4], which translates to $n \approx p \approx 5\times10^{12}/\text{cm}^2$ in graphene for many-body-induced coherence above 300 K [3]. Single layer graphene sheets have been gated up to densities in excess of $10^{13}/\text{cm}^2$ [5]. The BiSFET represents one attempt to explore the applicability of

this novel predicted behavior for graphene bilayers to achieve device functionality.

In the following we review the basic BiSFET device concept (Section 2) [3], how such a device, which would be far from a drop-in replacement for MOSFETs in CMOS logic, could be used for low power logic operation (Section 3) [3, 6, 7], and ongoing work to examine the effects of engineerable device parameters on formation and "gating" of interlayer coherence (Section 4) [8].

2. The BiSFET Device Concept

A schematic of a BiSFET intended to represent only the essential device elements is shown Figure 1(a). A *p*-type and an *n*-type layer of graphene are separated by a dielectric tunnel barrier (or perhaps are just misaligned in order to limit the bare charge carrier transport/tunneling between layers, but the effects of such misalignment on the interlayer coherence has not yet been well explored). The region for coherence could be defined, for example, by increased carrier concentrations consistent with the introductory remarks, or by variation of the separation between the two layers or variation in the dielectric material as will be discussed. As illustrated, each graphene layer has a metallic contact and is electrostatically coupled to a gate electrode through a gate dielectric. Much like for a Josephson junction, the current flow between the layers is expected to be limited by the peak/critical interlayer current beyond which the coherence would collapse. Below the critical current and associated critical interlayer voltage, the layers would be essentially shorted together via the many-body-enhanced interlayer current flow, with current flow limited by the leads; beyond this voltage, current would drop toward the single particle tunneling limit. The required carrier densities could perhaps be induced under zero gate bias by use of differing work functions for the gates, or ferroelectric oxides as dielectrics, and/or back-gating. Applied gate voltage signals are intended only to balance or slightly unbalance the charge concentrations between layers to increase or degrade the interlayer coherence, and, thus, increase or decrease the interlayer critical current. Note that in many cases a switchable input signal to only one gate is required, leaving a good deal of flexibility in what constitutes the other "gate."

Preliminary estimates for the critical current and associated voltage are provided in [3]. Perhaps the most important results are two qualitative predictions: first, the critical current and associated voltage should depend on engineerable device parameters, allowing them to be designed subject to technological constraints; second, the critical voltage can be small compared to $k_BT/q \approx 26\,\text{mV}$ at room temperature allowing potentially very low voltage operation. Qualitatively expected *I*-*V* characteristics are illustrated in Figure 1(b).

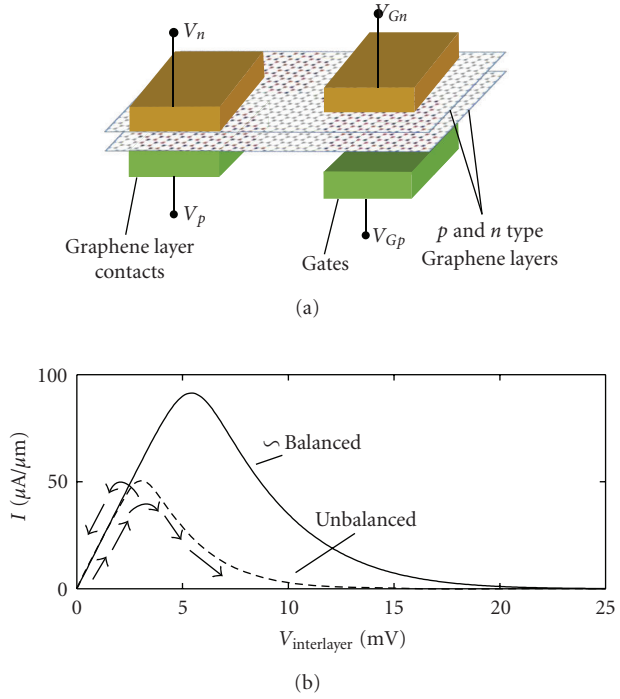

Figure 1: (a) Schematic illustration of BiSFET (with dielectrics not shown for clarity). (b) Qualitative estimation of interlayer current versus interlayer voltage for balanced and unbalanced charged distributions, consistent with the BiSFET model used in Section 2 as required for specificity. Arrows in (b) illustrate inverter operation as discussed in Section 3.

3. BiSFET Logic

Without an experimental realization of a BiSFET or even experimental evidence for formation of the condensate in adjacent layers of graphene at the time of writing, it might seem that exploring logic based on BiSFETs is a case of "putting the cart before the horse." However, such circuit level work helps measure the potential payoff of continuing device work, and informs that work through identification of critical device physics and technological challenges.

We also note that the *I*-*V* characteristics of Figure 1(b) are similar in some respect to those of resonant tunneling diodes, which have long been considered for logic applications. Indeed, the clocked biasing of the logic gates as discussed here has much in common with proposals for gated resonant tunneling diodes (RTDs), for example, [9, 10]. However, there are fundamental differences between how BiSFETs and gated RTDs operate, which are relevant to circuit design as well. For example, critical for low voltage circuit design, peak conductivity for a BiSFET would be intrinsically centered about a 0 V interlayer potential, with, again, critical voltages being small compared to k_BT/q. In an RTD, peak conductivity is associated with resonant band alignment, which may or may not occur under zero bias across the diode as defined not only by design but by device-to-device variances during fabrication, and is broadened by the thermal carrier distributions on either side of the junction in conventional RTD designs.

For the purposes of SPICE-based circuit simulation, we model the BiSFET as shown in Figure 2. To provide the required specificity for SPICE-based circuit simulation, the qualitative *I*-*V* behavior illustrated in Figure 1(b) has been

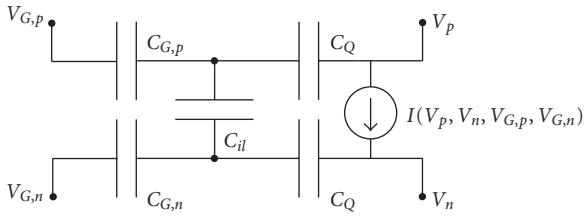

FIGURE 2: Circuit model of BiSFET used for SPICE simulation. $V_p - V_n$ is the interlayer voltage, and $V_{G,p}$ and $V_{G,n}$ are the gate voltages. $C_{G,p}$, $C_{G,n}$, and C_{il} are parallel plate capacitances between the p-type graphene layer and its gate, between the n-type graphene layer and its gate, and between the n and p graphene layers, respectively. C_Q are the quantum capacitances associated with the density of states of the individual graphene layers, and I is the interlayer current of all four applied voltages.

approximated via the smoothed current versus interlayer voltage relation,

$$I = G_o\left(V_p - V_n\right)\left[1 + \left(\frac{(V_p - V_n)/V_{\max}}{\exp\left(1 - \left|V_p - V_n\right|/V_{\max}\right)}\right)^4\right]^{-1/4}, \tag{1}$$

with gate dependent $V_{\max}$,

$$V_{\max} = V_{\max,o}\exp\left[-\frac{10\left|\Delta p - \Delta n\right|}{n+p}\right], \tag{2}$$

where G_o represents the ballistic Landauer-Büttiker limit of conductance, and Δn and Δp are the variations in charge densities with all four terminal voltages consistent with the model of Figure 2. There remains much work to be done on the device side to better quantify this behavior. However, we note that the actual form of the decay in the negative differential resistance (NDR) regime of (1), $I \approx G_o V_{\max}\exp(1 - |V_p - V_n|/V_{\max})$, is not critical to logic gates operation or power consumption [6]. Also, for specificity, for all the simulations presented below, the following model parameter values have been used in accordance with the calculations in [3]. All gate lengths have been chosen to be $L = 10$ nm. Unless otherwise specified, the gate/channel widths for BiSFETs shown in the circuits here are $W = 20$ nm for a W/L ratio of 2; larger specified values of W/L below indicate wider gates. Again for specificity, effective oxide thicknesses (EOTs) of 1 nm are assumed for gate and interlayer dielectrics corresponding to $C_g = C_{il} = 3.5 \times 10^{-6}$ F/cm^2, but this choice does not imply the use of the same oxides. To the contrary, the gate dialectics should be more insulating, while the interlayer dielectric should allow some single/bare electron tunneling which is necessary to allow the many-body-enhanced interlayer current on which the BiSFET relies [3, 8]. The nominal carrier densities in graphene layers were taken to be $p_o \approx n_o \approx 5 \times 10^{12}$ cm^{-2} which should theoretically allow room-temperature operation as discussed in Section 2. These densities could be provided by, for example, opposing gate work-functions of approximately ± 1 eV, respectively, or by one ± 1 eV gate work function and an opposing fixed back-gate bias.

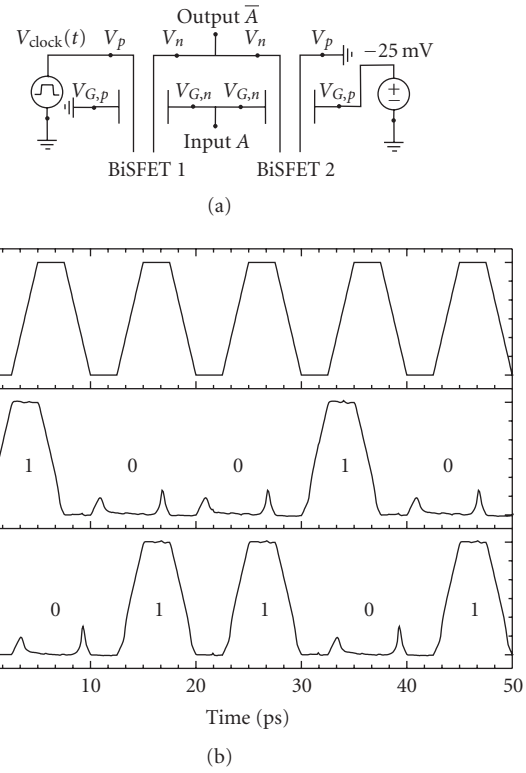

FIGURE 3: (a) BiSFET-based inverter layout and (b) clock signal, illustrated input voltage signal string (from a preceding inverter), and inverted output signal obtained using the SPICE circuit simulator.

Because of the substantial qualitative differences between BiSFET behavior and that of MOSFETs—that is, current decay rather than saturation with increased interlayer voltage, and perhaps weak dependence on gate voltage by comparison—entirely different ways of implementing Boolean logic are required using BiSFETs. The simplest of logic elements, an inverter, can be realized in a complementary layout as shown in Figure 3(a) where we have used a symbolic representation for the BiSFET. The unswitched "back-gate" voltages represent changes in work-functions, modulation doping, or actual back-gate voltages that produce an equivalent charge imbalance. Although this circuit appears similar to a CMOS inverter, the operation is notably different, with a clocked power supply $V_{\text{clock}}(t)$ [3, 6], as in, for example, [9]. $V_{\text{clock}}(t)$ is used because changing the input signal/voltage with a fixed power supply has no effect on the output signal. Instead, $V_{\text{clock}}(t)$ must be raised after the input signal is set for proper logic functionality. As illustrated via the arrows in Figure 1(b), as the clock voltage increases, it is split essentially equally between the two devices until the current reaches the peak allowed for the device with the smaller peak/critical current. Beyond that point the current can only decrease, forcing the voltage drop across the device with the larger critical current back toward zero while that for the device with the smaller critical current increases into the NDR region. With a 0 mV input signal and -25 mV on V_{Gp2}, BiSFET 2 will have a charge imbalance and the associated lower critical current, causing the output

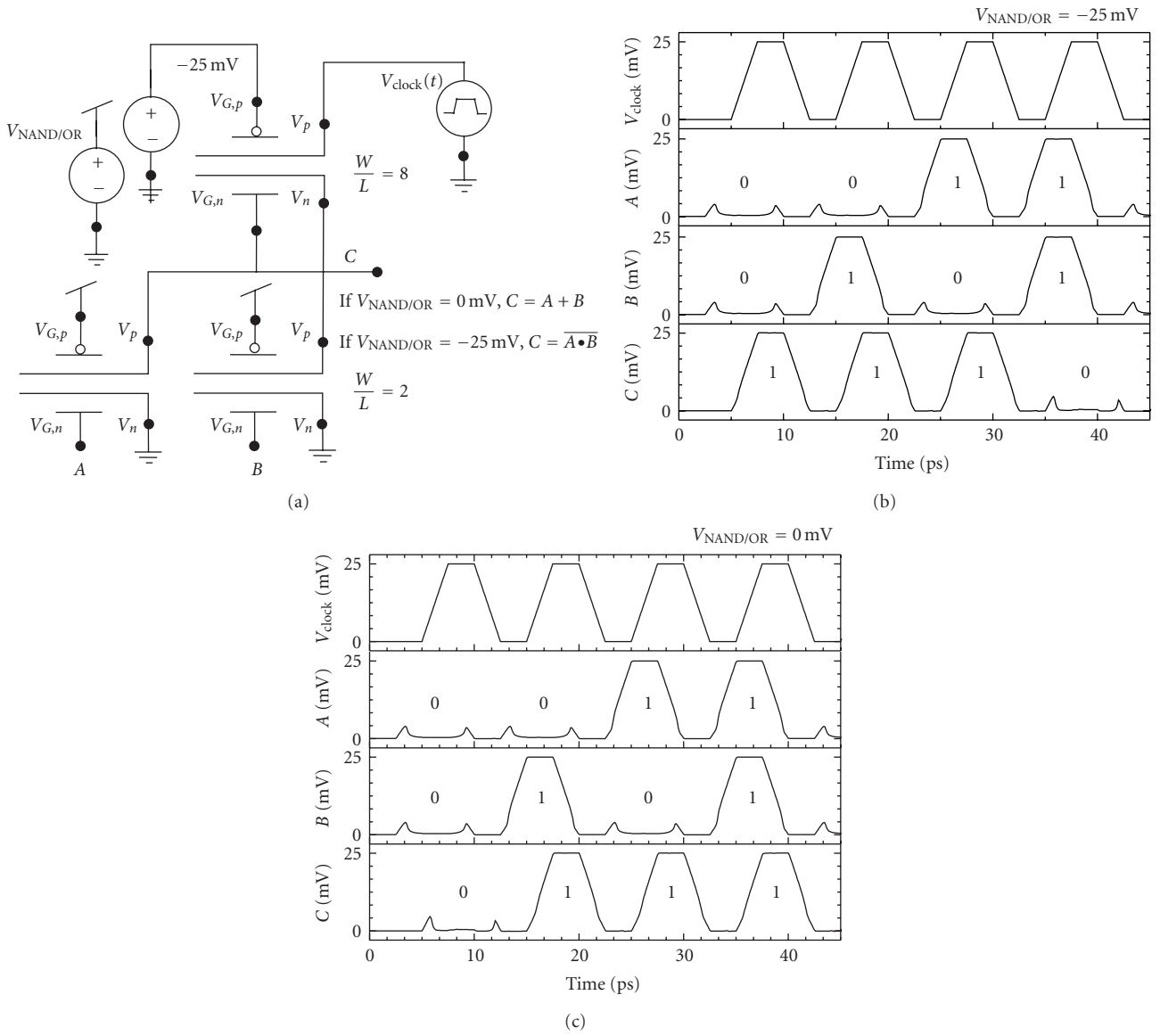

Figure 4: (a) A programmable NAND/OR Gate and SPICE simulation results of (b) NAND and (c) OR gate operation at 100 GHz.

signal to closely follow $V_{\text{clock}}(t)$, that is, to go high. With the input voltage high, +25 mV, however, the charge in BiSFET 2 is balanced and that in BiSFET 1 is unbalanced, $V_{\text{clock}}(t)$ is dropped predominantly across BiSFET 1, and the output signal remains low. Similarly, removing the input signal will have no effect on the output while the clock signal remains high; each gate also serves much like a latch.

Figure 3(b) shows the SPICE-simulated response for such an inverter. The clock signal is pulsed with a frequency of 100 GHz and peak clock voltage of 25 mV. A four-inverter output load was considered. The clock signal is delayed relative to the input signal by the 2.5 ps rise time, allowing the latter to be set before the inverter is clocked. Both input and output signals were subject to a fan-in and fan-out of four inverters, respectively. The average energy consumed per clock cycle per BiSFET was ∼0.01 aJ = 10 zJ. For comparison, the switching energy for current MOSFETs is ∼100 aJ, and 2020 "end of the roadmap" CMOS will have a switching energy on the scale of 5 aJ [2]. The drastic energy reductions are largely a function of the reduced operating voltage for this many-body-coherence-mediated switching mechanism that may be possible, where energies scale as the square of voltage, of course. However, these estimates are rough and do not consider the parasitic power losses of delivering the clock signal to each BiSFET. And, each BiSFET is switched on each clock cycle, for an effective activity factor of unity for an active clock.

Other logic gates such as NAND, NOR, OR, and XOR (exclusive OR) gates, and memory elements have also been implemented and verified by SPICE simulations [6, 7], as per the example of the potentially programmable NAND/OR gate of Figure 4. The average energy consumed per switching

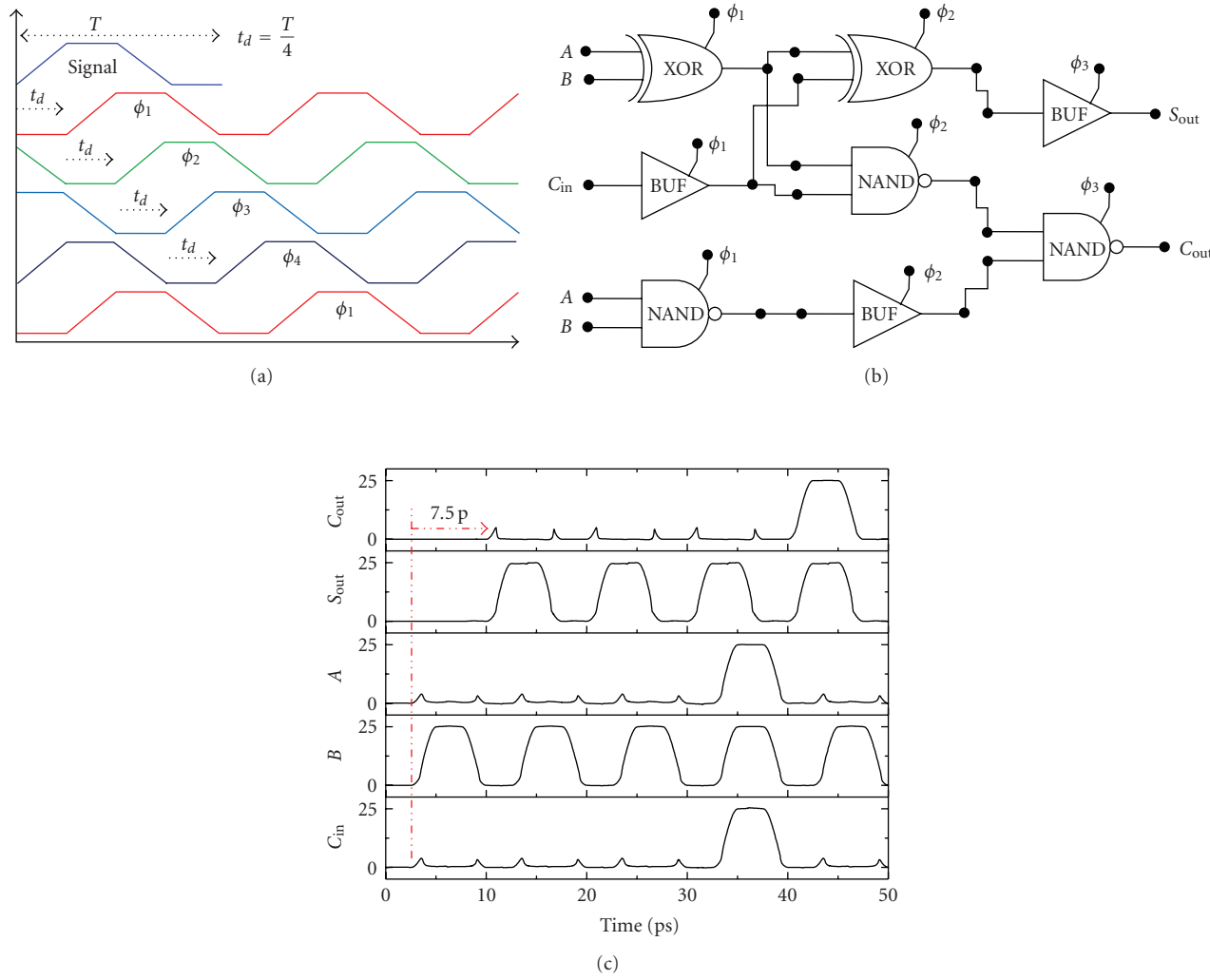

FIGURE 5: (a) Illustration of a four-phase clocking scheme, (b) a 1-bit full adder, and (c) inputs and sum (S) and carry (C) outputs with the delay between input and output shown.

operation per gate (not per BiSFET) was ~30 zJ for both the NAND and OR gates, respectively. We have also considered multistage circuits using a four-phase clock signal, as in [10], such as the adder of Figure 5 [7]. Note that although each gate in series requires a quarter-period delay in processing the signal, the inputs can be released once the output for each gate is set, and new inputs can be processed each clock cycle no matter how many subsequent gates there are in series.

4. Achieving and Gating Interlayer Coherence

To take a direct look at the many-body-interaction-induced interlayer coherence, we use a π-band tight-bond model of the graphene layers, treat the many-body interaction via a Fock approximation as within the original work predicting possible room-temperature coherence [4], and neglect any bare/single particle coupling here although it is ultimately required to support the critical current. The interlayer coherence is therefore driven entirely by the exchange interactions between the top (T) and bottom (B) layers,

$$V_F(\mathbf{R}_T, \mathbf{R}_B) = \frac{-e^2}{4\pi\varepsilon_0\varepsilon_r\sqrt{(\Delta R)^2 + d^2}} \times \sum_{\alpha,\mathbf{k},s} n_{\alpha,\mathbf{k},s}\phi_{\alpha,\mathbf{k},s}(\mathbf{R}_T)\phi^*_{\alpha,\mathbf{k},s}(\mathbf{R}_B). \quad (3)$$

Here, $\mathbf{R}_T$ and $\mathbf{R}_B$ are the 2D in-plane vectors for the atoms in the top and bottom graphene layers, respectively. $\Delta R = |\mathbf{R}_T - \mathbf{R}_B|$ is the magnitude of the in-plane component of the separation between the atoms, and d is the separation between the two layers, and the $\phi_{\alpha,\mathbf{k},s}(\mathbf{R})$ are the self-consistently calculated single particle Bloch functions subject to the Fock interaction, where α labels the band, $\mathbf{k}$ the wavevector, and s the spin state.

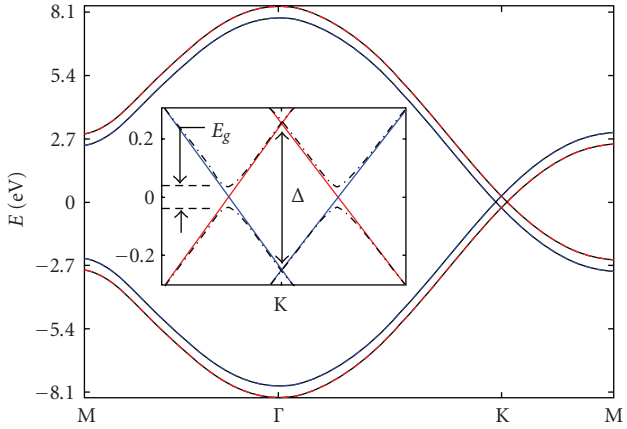

FIGURE 6: Energy bands of two graphene layers separated by 1.0 nm of SiO_2 (ε_r = 3.9), having layer potentials of $-\Delta/2$ (top layer—blue) and $+\Delta/2$ (bottom layer—red) in the uncoupled state (solid lines) along the high-symmetry directions in the Brillouin zone (shown above). Δ = 0.5 eV. Phase coherence between layers creates a correlated, lower energy state (black dash-dotted lines). The inset magnifies the low energy-spectrum, revealing a band gap E_g of 74 meV at 0 K for balanced top and bottom layer charge distributions with E_F located within the band gap.

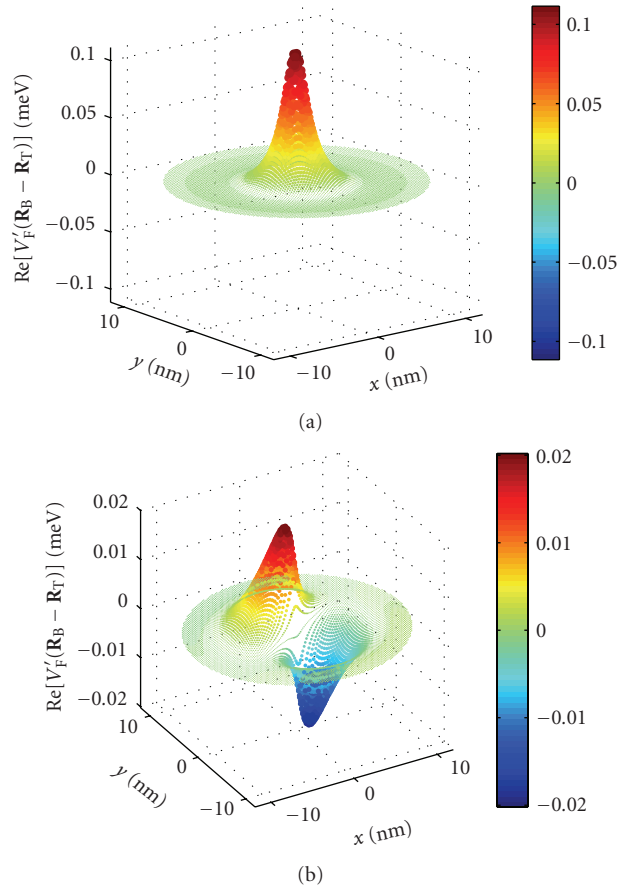

FIGURE 7: (a) Real part of $V'_F(\mathbf{R}_T,\mathbf{R}_B)$ for A_T-A_B coupling obtained by dividing $V_F(\mathbf{R}_T,\mathbf{R}_B)$ by $\exp[i\mathbf{k}_D \cdot (\mathbf{R}_T - \mathbf{R}_B)]$, as a function of $\mathbf{R}_T - \mathbf{R}_B$ for Δ = 0.5 eV, d = 1 nm, ε_r = 3.9, and balanced charge distributions at 0 K. The imaginary part essentially vanishes. $V'_F(\mathbf{R}_T,\mathbf{R}_B)$ for B_T-B_B is essentially identical except for a 180° degree phase shift. (b) Real part of $V'_F(\mathbf{R}_T, \mathbf{R}_B)$ for A_T-B_B coupling obtained under the same conditions. The imaginary part is rotated by 90°. $V'_F(\mathbf{R}_T,\mathbf{R}_B)$ for B_T-A_B coupling is essentially the complex conjugate of $V'_F(\mathbf{R}_T, \mathbf{R}_B)$ for A_T-B_B coupling.

Of course, self-consistent solutions can be obtained simply by setting the interlayer exchange interactions to zero. This solution corresponds to an uncorrelated/incoherent state with electrons isolated in one layer or the other. However, a self-consistent solution that yields a nonzero value of the interlayer exchange potential and eigenfunctions that overlap both layers is what we are after. Coherence results in a gap in the energy spectrum of the two-layer system near the points at which the conduction band of the top layer and the valence band of the lower would otherwise cross. For balanced charge distributions in the two layers (overall charge neutrality) the Fermi level falls within the center of the gap, energy is gained due to gap formation, and the coherent state becomes energetically favorable. This band splitting for such a correlated state (0 K temperature, balanced charge distributions of 6×10^{12} cm^{-2} corresponding to an interlayer potential splitting Δ of 0.5 eV, interlayer spacing of 1 nm, and dielectric permittivity ε_r = 3.9 of SiO_2) is illustrated in Figure 6, where the energy bands are plotted along the high-symmetry directions.

Figure 7 shows corresponding 0 K solutions for the self-consistent nonlocal Fock potential of (3). Note that the result depends greatly on which of the two atoms in the primitive unit cell of each layer are considered. Physically, the alignment (not the coupling) was Bernal-like for this particular simulation, but the result is essentially the same for a hexagonal-like alignment because the separation between the graphene layers is much greater than the nearest neighbor atomic separation within layers. Also note that, beyond being nonlocal within the plane of the layers, the coupling is neither Bernal-like nor hexagonal-like, but rather takes on an antihexagonal nature, at least in the absence of bare coupling. As further detailed in [8], along with initial efforts to consider the consequences for the critical interlayer current, this antihexagonal pattern of coupling is optimal for coupling the chiral valence band and conduction band electron states of the individual graphene layers to each other, states which have opposite relative phases between the two atomic sublattices for any given wavevector $\mathbf{k}$.

The need is for room-temperature coherence, however. As temperature increases, states below the condensate band gap begin to empty, and states above the condensate band gap begin to fill whose contributions to the condensate is of same magnitude but opposite sign to their counterparts below, breaking down the condensate, as again detailed in [8]. Figure 8(a) illustrates the resulting temperature dependence of the condensate for three different dielectric permittivities, exhibiting a universal behavior when normalized to the 0 K band gap. Thus, along with other considerations [4], obtaining a room-temperature condensate translates to finding a 0 K band gap greater than at least approximately $4k_BT$

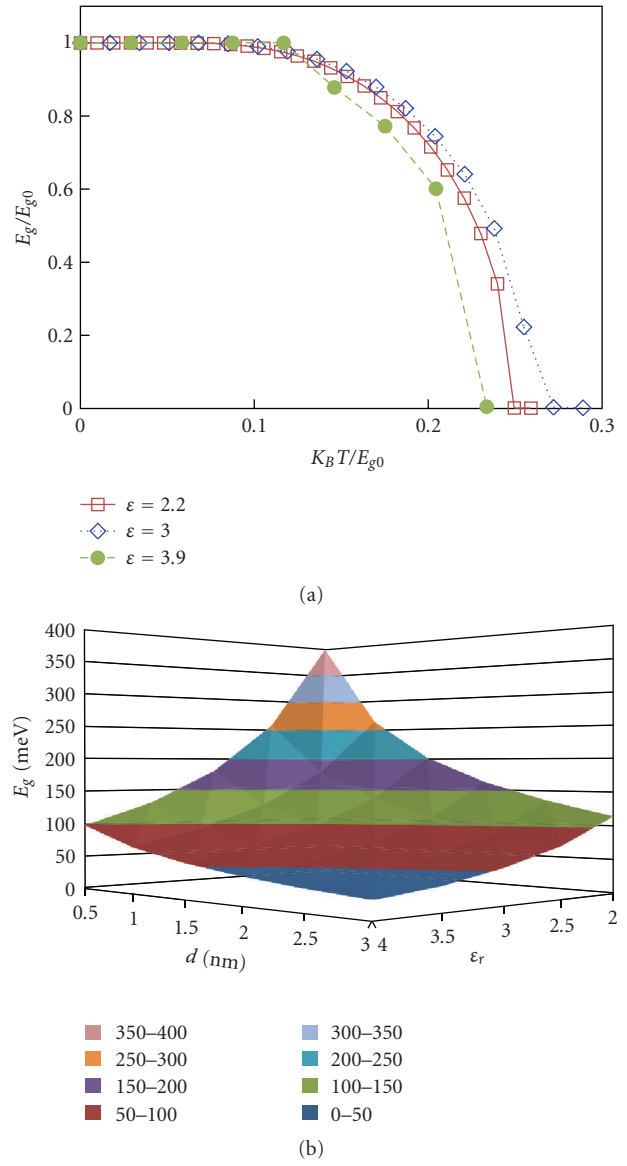

Figure 8: (a) Temperature dependence of the band gap for three different dielectric constants normalized to the 0 K band gap in each case, with $\Delta = 0.5$ eV, $d = 1$ nm, and balanced charge distributions. (b) 0 K band gap as a function of interlayer separation d and dielectric relative permittivity ε_r.

$\approx$ 100 meV. The 0 K band gap for various combinations of layer separation and displacement are shown in Figure 8(b). Among other things, it becomes clear that low-permittivity dielectrics are preferable, in contrast to the needs of CMOS devices (or to dielectrics encountered in III–V quantum well systems).

Finally, Figure 9 provides an example of degradation of the condensate with charge imbalance. In this case at least, the initial sensitivity is actually less than that of (2) used in SPICE simulations. This should not be that qualitatively critical, however, as the circuits are bistable and essentially any difference in critical currents should be sufficient to control the switching. On the other hand, with a bit more

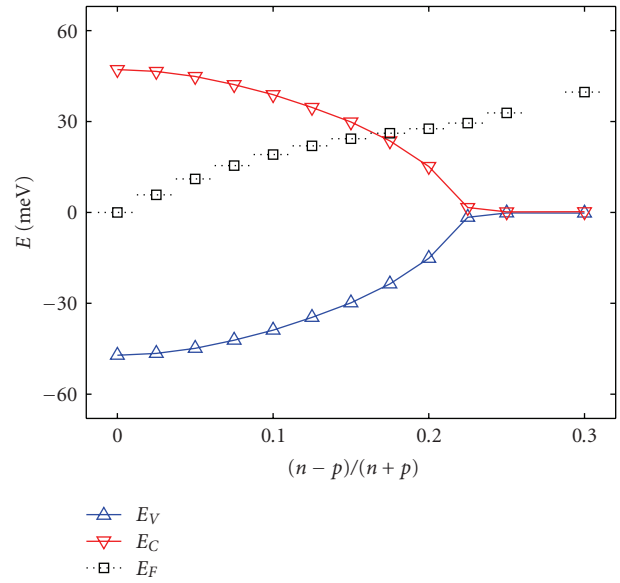

Figure 9: Energy band edges for the coherent state and Fermi level as a function of carrier imbalance between top layer electron density and bottom layer hole density, for graphene bilayers separated by 1 nm at 300 K with $\varepsilon_r = 3.0$ and $\Delta = 0.5$ eV.

charge imbalance, the coherence appears to completely collapse, for reasons detailed in [8], and more conventional logic may become possible.

5. Conclusion

We have reviewed ongoing efforts on the theory side to translate possible room-temperature many-body-induced interlayer coherence in graphene bilayers into a "beyond CMOS" switch, a Bilayer PseudoSpin Field Effect Transistor or BiSFET. The BiSFET is, however, currently only a concept based on novel predicted physics in a novel material system. And we recognize the limitations of theory, and the technological challenges to realization of BiSFETs even if theory holds. There are certainly no guarantees that such a device based on room-temperature many-body-mediated coherence between graphene layers can ever be realized. However, we believe that the potential benefits of ultra-low power logic well justify the efforts, theoretical as here as well as experimental, to more fully explore the possibility.

Acknowledgments

This work was supported through the NRI SWAN Center by the Semiconductor Research Corporation and the Texas Emerging Technology Fund, and by the U.S. Army Research Office.

References

[1] C. Hu, D. Chou, P. Patel, and A. Bowonder, "Green transistor—a V_{DD} scaling path for future low power ICs," in *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA '08)*, pp. 14–15, April 2008.

[2] International Technology Roadmap for Semiconductors, http://www.itrs.net/.
[3] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (BiSFET): a proposed new logic device," *IEEE Electron Device Letters*, vol. 30, no. 2, pp. 158–160, 2009.
[4] H. Min, R. Bistritzer, J.-J. Su, and A. H. MacDonald, "Room-temperature superfluidity in graphene bilayers," *Physical Review B*, vol. 78, no. 12, Article ID 121401, 2008.
[5] P. Avouris, Z. Chen, and V. Perebeinos, "Carbon-based electronics," *Nature Nanotechnology*, vol. 2, no. 10, pp. 605–615, 2007.
[6] D. Reddy, L. F. Register, E. Tutuc, and S. K. Banerjee, "Bilayer pseudospin field-effect transistor: applications to Boolean logic," *IEEE Transactions on Electron Devices*, vol. 57, no. 4, pp. 755–764, 2010.
[7] D. Reddy, L. F. Register, E. Tutuc, G. D. Carpenter, A. H. MacDonald, and S. K. Banerjee, "Bilayer pseudospin field effect transistor for beyond CMOS logic," INC6 Grenoble, France, May 2010.
[8] D. Basu, L. F. Register, D. Reddy, A. H. MacDonald, and S. K. Banerjee, "Tight-binding study of electron-hole pair condensation in graphene bilayers: gate control and system-parameter dependence," *Physical Review B*, vol. 82, Article ID 075409, 9 pages, 2010.
[9] T. Akeyoshi, K. Maezawa, and T. Mizutani, "Weighted sum threshold logic operation of MOBILE (monostable-bistable transition logic element) using resonant-tunneling transistors," *IEEE Electron Device Letters*, vol. 14, no. 10, pp. 475–477, 1993.
[10] C. Pacha, P. Gloesekötter, K. Goser, U. Auer, W. Prost, and F.-J. Tegude, "Resonant tunneling transistors for threshold logic circuit applications," in *Proceedings of the 9th IEEE Great Lakes Symposium on VLSI*, pp. 344–345, IEEE Computer Society Press, Ann Arbor, Mich, USA, 1999.