

Research Article

Structural and Electrical Characteristics of Metal-Ferroelectric $\text{Pb}_{1.1}(\text{Zr}_{0.40}\text{Ti}_{0.60})\text{O}_3$ -Insulator (ZnO)-Silicon Capacitors for Nonvolatile Applications

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In this work metal-ferroelectric-insulator-semiconductor (MFIS) thin-film structures using $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3$ (PZT) as the ferroelectric layer and zinc oxide (ZnO) as the insulator layer were fabricated on n-type (100) Si substrate. $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3$ and ZnO thin films were prepared on Si by the sol-gel route and thermal deposition method, respectively. On the optimized PZT (140 nm) and ZnO (40 nm) films were examined by scanning electron microscope (SEM). From AFM data the root mean square (r.m.s.) roughness of the film surface is 13.11 nm. The leakage current density of ZnO/n-Si (MIS) structure was as low as $1.8 \times 10^{-8} \text{ A/cm}^2$ at 2.5 V. The capacitance versus voltage (C-V) characteristics of the annealed ZnO/Si (MIS) diode indicated the good interface properties and no hysteresis was observed. Au/PZT (140 nm)/ZnO (40 nm)/Si (100) leakage-current density was about $5.7 \times 10^{-8} \text{ A/cm}^2$ at positive bias voltage of 3 V. The large memory window width in C-V (capacitance-voltage) curve of Au/PZT/ZnO/Si capacitor was about 2.9 V under $\pm 12 \text{ V}$ which thus possibly enables nonvolatile applications. The memory window as a function of temperature was also discussed.

1. Introduction

Ferroelectric materials such as $\text{Pb}(\text{ZrTi})\text{O}_3$ (PZT) have been extensively studied for dynamic random access memory (DRAM) and nonvolatile memory applications [1, 2]. In particular, the ferroelectric field-effect transistors (ferroelectric FETs), in which the gate with metal/ferroelectric/semiconductor (MFS) structure is controlled by the spontaneous polarization of ferroelectric materials, are expected to be one of the leading candidates for future nonvolatile memory devices [3], because of their fast switching speed, nonvolatility, tolerance against radiation, and high integrated density. In order to realize ferroelectric FETs, preparation of ferroelectric/Si structures with a sharp interface is essential. However, it is very difficult to deposit the ferroelectric PZT films directly on silicon substrates without interfacial reaction [4], because Pb is highly reactive with Si and easily diffuses into the Si substrates. Therefore, an insulating buffer layer preventing interdiffusion of Si and Pb is necessary for PZT

film deposition on Si substrates. Thus many kinds of buffer layer such as Y_2O_3 [5], CeO_2 [6], YMnO_3 [7], SrTiO_3 [8], PbO [9], HfO_2 [10], Si_3N_4 [11], and TiO_2 [12] films have been proposed to avoid the diffusion at the interface between ferroelectric materials and Si substrates. But it was found that devices with these buffer layers have large current drops due to the high density of crystalline defects or carrier traps existing in the interface of Si and buffer. Rajangam Ilangovan et al. used Al_2O_3 - HfO_2 buffer layer with SBT ferroelectric layer to improve the electrical properties [13, 14]. So selecting a suitable buffer layer and corresponding processing conditions is still essential to improve the performance of ferroelectric memory devices. In this work, we have introduced ZnO which is used as a buffer layer between the ferroelectric thin film and Si because it has relatively high dielectric constant. In order to show that the PZT-ZnO-based MFIS structure is suitable for nonvolatile memory FETs with large memory window, the electrical and structural properties of the MFIS structure at a relatively low

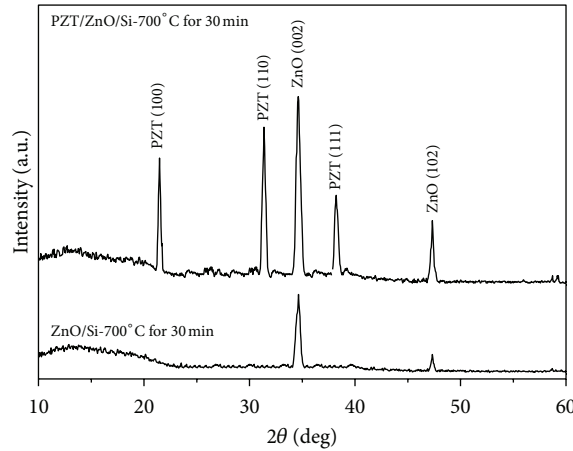


FIGURE 1: XRD patterns of the $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3/\text{ZnO}/\text{n-Si}$ and $\text{ZnO}/\text{n-Si}$ thin films.

processing temperature of 700°C were investigated and the fabricated capacitor (MFIS) performance has been evaluated with varying annealing process.

2. Experiment

The ZnO films were deposited on n-type Si substrates using ZnO powder (purity > 99.999%, produced by Merck Ltd.) by thermal evaporation process (HIND HI VAC Model no. 12 A4D Vacuum Coating Unit) and the maintained chamber pressure was approximately 10^{-5} torr. During evaporation, the substrates were kept 15 mm above the source material. The as-deposited ZnO films were annealed in air using conventional tubular furnace at 700°C for 30 min. The $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3$ films were deposited on ZnO/n-type Si (100) substrates by sol-gel route. The starting materials were lead acetate trihydrate ($\text{Pb}(\text{CH}_3\text{COO})_2 \cdot 3\text{H}_2\text{O}$, 99.5% Loba chemicals), titanium (IV) isopropoxide ($\text{Ti}(\text{O}^i\text{Pr})_4$, 99% Merck), and zirconium acetylacetonate ($\text{ZrC}_{20}\text{H}_{28}\text{O}_8$, 99.8% Merck). 2-methoxyethanol and acetic acid were used as a solvent and chemical modifier, respectively. The concentration of PZT precursor solution was 0.4 M. Excess of lead acetate (10%) was added to the solution to compensate the loss of lead during the thermal treatment. PZT thin films were prepared by spin coating at the speed of 3000 rpm for 20 seconds. After depositing by spin coating, the gel films were pyrolyzed in air at 300°C for 10 min to remove solvent and other organics. These processes were repeated for several times to achieve desired film thickness. Finally, the $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3$ thin film postannealed at 600°C and 700°C for 30 min in air. The thickness of the PZT films was 140 nm. For measurements of electrical properties, gold was used as a top electrode on $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3/\text{ZnO}/\text{Si}$ structures by a vacuum evaporation method at room temperature through a shadow mask, and the area was 0.2 mm^2 . Silver paste was used as a bottom electrode of silicon side of PZT/ZnO/Si structure.

Crystalline properties of PZT/ZnO/n-Si (100) were examined by powder X-ray diffraction (XRD) analysis with

Cu-K α radiation (Model XPERT-PRO). Microstructure and morphology of the thin film samples were observed using scanning electronic microscope (SEM, Hitachi Model S-3000H) and atomic force microscope (AFM). The Capacitance-Voltage (C-V) characteristics of the MIS and MFIS structure were measured by using an impedance analyzer (HP4194A) at 1 MHz with a small signal voltage of 200 mV. The sweep rate of the bias voltage was 0.2 V/s. Leakage current density (J-V) measurements were done using Keithley 6517 electrometer.

3. Results and Discussions

Figure 1 shows the XRD patterns of the ZnO and PZT/ZnO thin films on n-type Si substrate. The ZnO has the hexagonal structure and preferred orientation of (0002) direction in the out-of-plane direction after annealing at 700°C for 30 min. The crystalline quantity of ZnO thin films can be evaluated by the full width half maximum (FWHM) of (0002) peak at $2\theta = 34.59$. The sol-gel derived PZT thin films on ZnO/Si structure were annealed at 700°C for 30 min. All PZT films on the ZnO/Si film exhibited polycrystalline growth. No undesirable peak of pyrochlore phase appears in the XRD patterns of PZT films annealed at 700°C , which implies that PZT films are well crystallized with perovskite structure with preferred orientation of (111) peak at $2\theta = 38.20$.

Figure 2 shows the SEM images of the surface and cross-section of the PZT/ZnO/Si structure thin films. Figure 2(a) shows that the films have the dense and crack-free surface. Figure 2(b) shows that the average film thickness of the PZT and ZnO was 140 nm and 40 nm, respectively. The PZT was deposited by spin coating; the layer smoothness depends on the rotation of substrate. The layer structure (fracture) may be due to lesser substrate rotation (2000 rotation per minute). The surface would have been smooth if the rpm is high (nearly 3000 rpm).

Figure 3(a) shows the AFM images of $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3/\text{ZnO}$ films on Si substrates annealed at 700°C for 30 min.

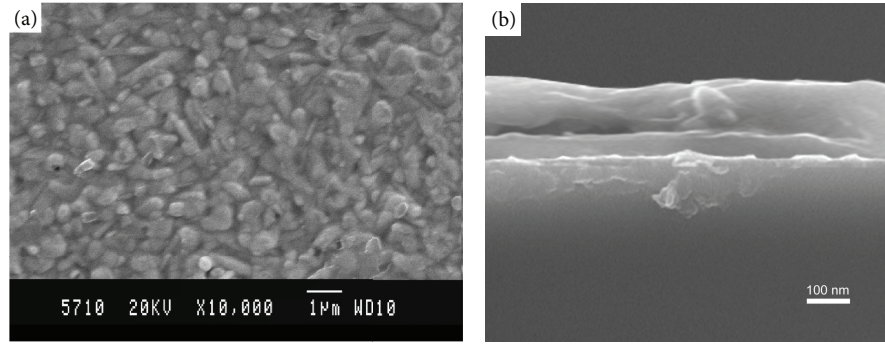


FIGURE 2: SEM images of the (a) surface and (b) cross-section view of PZT/ZnO/Si thin films.

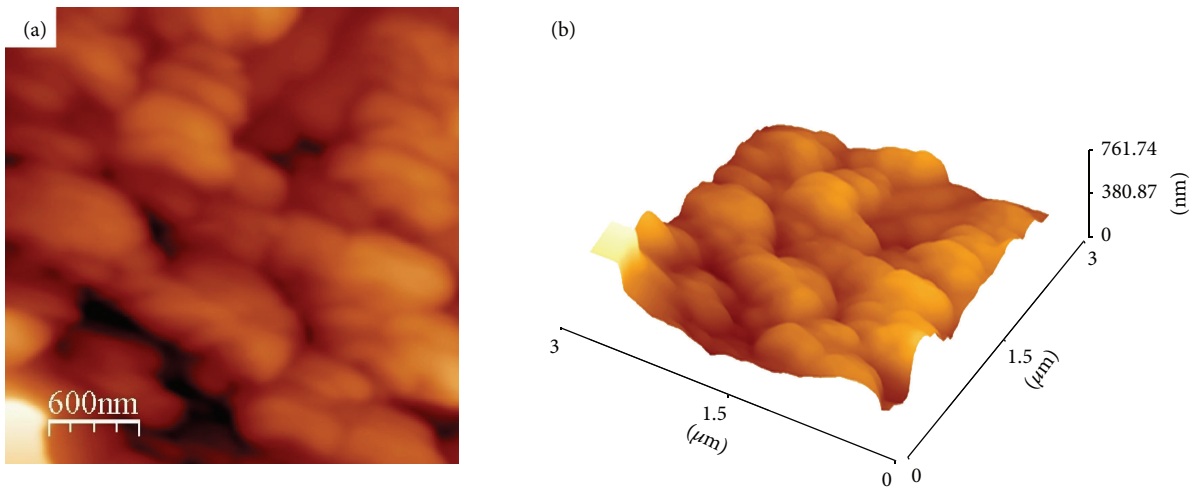


FIGURE 3: AFM images of $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3/\text{ZnO}$ films on Si substrate annealed at 700°C for 30 min.

The root mean square (r.m.s.) roughness of the film surface is 13.11 nm and observed well-defined grain growth of PZT/ZnO structure. As can be seen from Figure 3(b), after nucleation, circular rosettes grow at right corner of the film along perpendicular direction to the substrate [15].

Figure 4(a) shows a typical C-V characteristic at room temperature for an Au/ZnO/Si (MIS) diode measured at 1 MHz with a small signal voltage of 200 mV, and the sweep rate of the bias voltage was 0.2 V/s. The C-V curve clearly shows the region of accumulation, depletion, and inversion. The accumulation region capacitance is read to be approximately 440 pF. The width of the loop is 0.2 V, which shows that ZnO layer served as a good buffer layer and there is no apparent threshold hysteresis in the C-V curve. In order to improve the performance of the MFIS FET, one of the important points is that the ZnO buffer insulating layer should have small leakage current and a high dielectric constant. Figure 4(b) shows J-V characteristics of Au/ZnO/Si (MIS) structure annealed at 700°C for 30 min, which was measured with a voltage step of 0.3 V and delay time of 8 sec. The current density at 2.5 V is about $1.8 \times 10^{-8} \text{ A/cm}^2$ under positive bias of 6 V, which indicates that the insulating

property of the deposited ZnO film layer of MFIS structure is relatively good for memory device applications.

Figure 5(a) shows typical curves of the 1 MHz C-V characteristics for the Au/ $\text{Pb}_{1.1}\text{Zr}_{0.40}\text{Ti}_{0.60}\text{O}_3/\text{ZnO}/\text{Si}$ capacitor. The measurements were performed at room temperature. The maximum capacitances were measured at different gate voltages, with a sweep rate at the bias voltage of 0.2 V/s. The counterclockwise C-V hysteresis loop, indicated by the arrows in the figure, is observed. In our C-V experimental results, the memory window of the Au/PZT/ZnO/n-Si (100) capacitor increased as the gate voltage increases [16]. The width of the loop increased from 0.5 V to 2.9 V with increasing the applied voltage from ± 4 to ± 12 V, respectively. Further increasing the bias voltage up to ± 14 V the memory window decreased (Figures 5(a) and 5(b)). This is due to the charge injection into the ZnO because much higher electric field is applied to the ZnO layer. This memory window satisfies the practical application of nondestructive read-out (NDRO) ferroelectric random access memories (FRAMs) operation.

Figure 6 exhibits counterclockwise C-V curves of Au/PZT/ZnO/n-Si (MFIS) structures, which were annealed at varying temperatures. The values of memory window

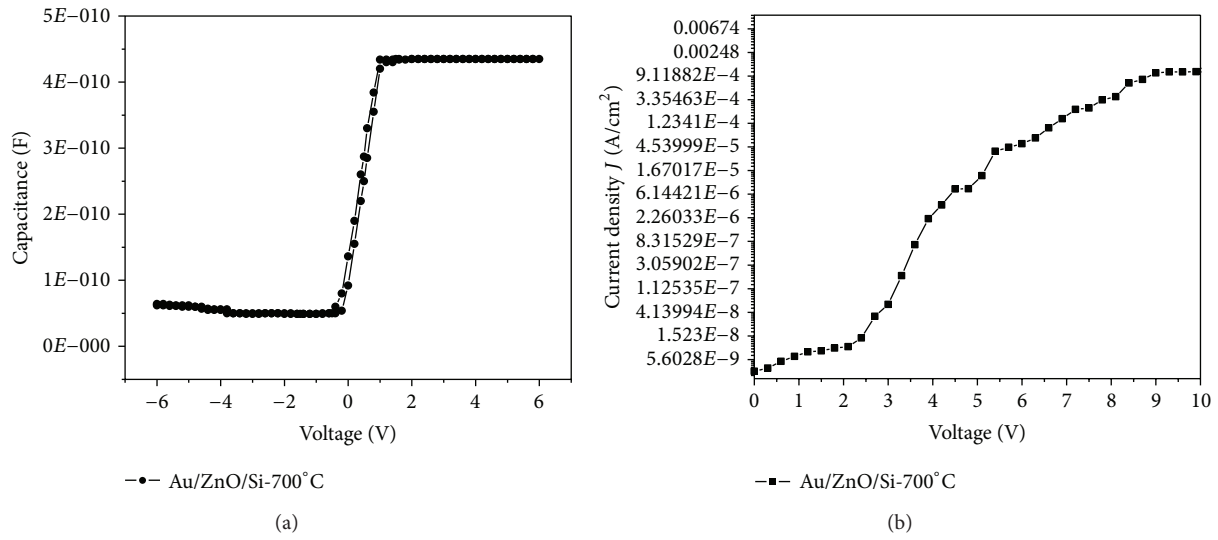


FIGURE 4: (a) C-V and (b) J-V characteristics of Au/ZnO/Si (100) (MIS) diodes annealed at 700°C for 30 min.

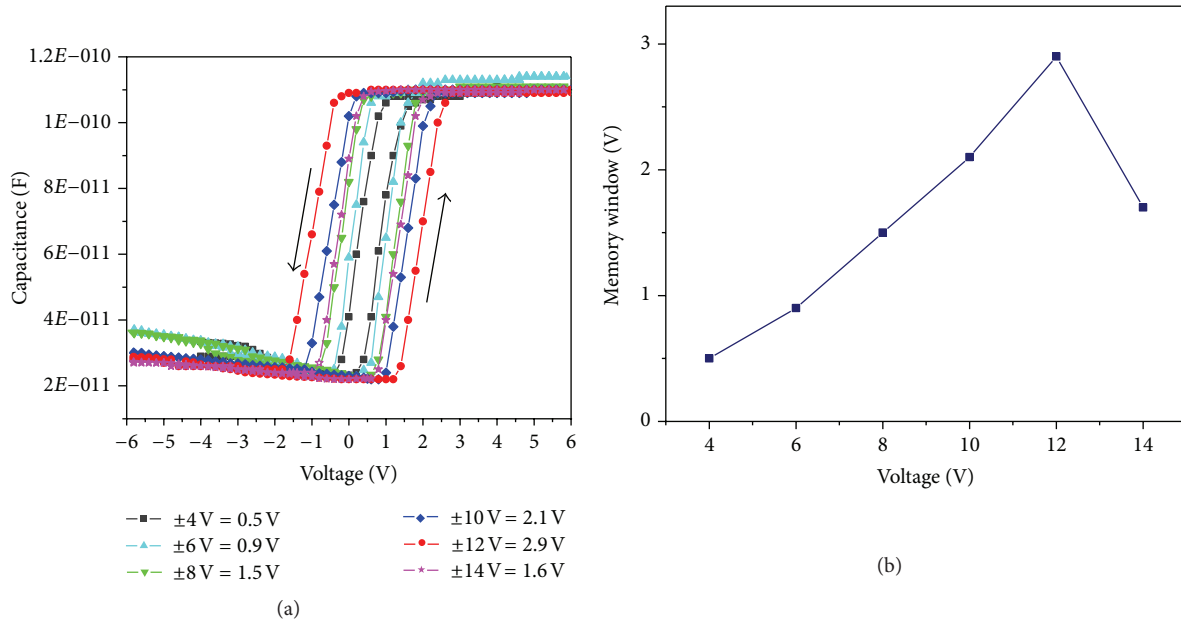


FIGURE 5: (a) C-V curves and (b) the memory window of the Au/PZT/ZnO/Si (MFIS) structure.

width were about 1.7 V and 2.9 V for the annealing temperature 600°C and 700°C, respectively. The hysteresis characteristics are considered due to the ferroelectric property of the PZT film. This result indicated that the annealing of the PZT film at 600°C is insufficient for the crystallization of the PZT film [17], and on the other hand there was no lead loss at 700°C.

Leakage current density is one of the important parameters for device application. Figure 7 exhibits J-V characteristics of Au/PZT/ZnO/n-Si (MFIS) structure at 700°C only,

which was measured with a voltage step of 0.3 V and delay time of 0.8 sec. As can be seen from Figure 7, the leakage-current density of MFIS capacitors is about 5.7×10^{-8} A/cm² at positive applied voltage 3 V. The leakage current densities are relatively low at positive voltage 3 V, compared to Masrurah and Toda [18], and the voltage dependence of the leakage current densities is low. The experimental results indicate that the PZT/ZnO-based MFIS heterostructures are suitable for nonvolatile ferroelectric memory applications especially for low power dissipation operation in the devices.

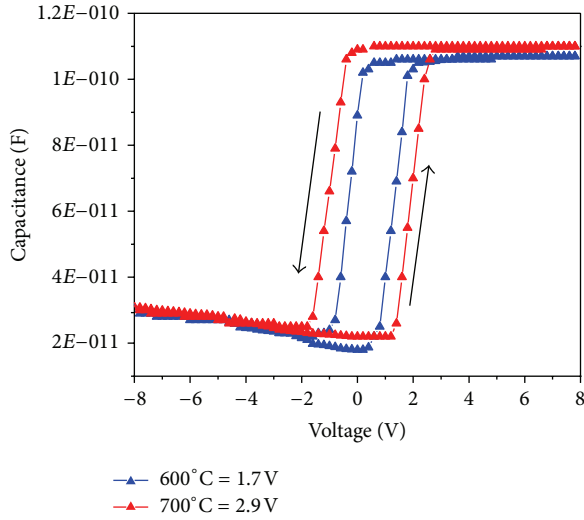


FIGURE 6: C-V characteristics for Au/Pb_{1.1}Zr_{0.40}Ti_{0.60}O₃/ZnO/Si capacitors at various annealing temperature.

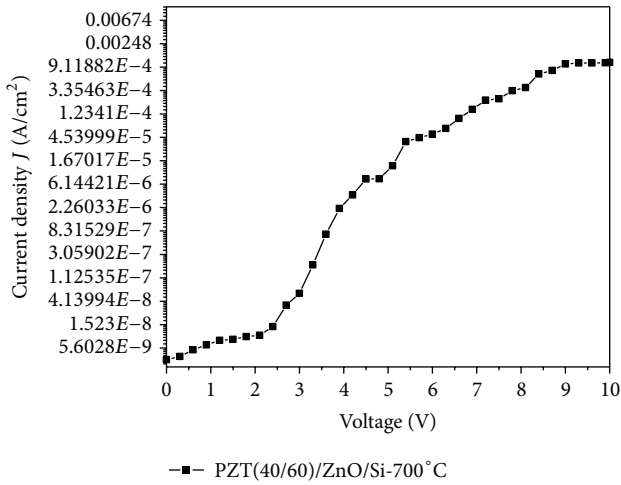


FIGURE 7: Leakage current density (J-V) characteristic of Au/PZT/ZnO/n-Si capacitor.

4. Conclusion

PZT (MFIS) capacitors have been successfully fabricated using ZnO buffer layer. The C-V curve of Au/ZnO/Si (MIS) clearly shows the region of accumulation, depletion, and inversion. There is no threshold hysteresis observed, and the leakage current is very low. Au/PZT/ZnO/Si Leakage-current density was about 5.7×10^{-8} A/cm² at positive bias voltage of 3 V. In the capacitance-voltage (C-V) characteristics of Au/Pb_{1.1}Zr_{0.40}Ti_{0.60}O₃/ZnO/n-Si (100) structures, a hysteresis loop with counterclockwise trace was observed, and the memory window was about 2.9 V. This result suggests that PZT/ZnO/Si capacitor is suitable for nonvolatile memory FETs with large memory window in low voltage, low power dissipation operation. In future, PZT/ZnO interface should be further studied to exploit potential advantages arising

from the direct integration of ferroelectric materials on semiconductors.

Conflict of Interests

The authors declare that they have no conflict of interests.

Acknowledgment

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