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Research Article

Analysis of Low Dimensional Nanoscaled Inversion-Mode InGaAs MOSFETs for Next-Generation Electrical and Photonic Applications

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The electrical characteristics of $In_{0.53}Ga_{0.47}As$ MOSFET grown with Si interface passivation layer (IPL) and high k gate oxide HfO_2 layer have been investigated in detail. The influences of Si IPL thickness, gate oxide HfO_2 thickness, the doping depth, and concentration of source and drain layer on output and transfer characteristics of the MOSFET at fixed gate or drain voltages have been individually simulated and analyzed. The determination of the above parameters is suggested based on their effect on maximum drain current, leakage current, saturated voltage, and so forth. It is found that the channel length decreases with the increase of the maximum drain current and leakage current simultaneously. Short channel effects start to appear when the channel length is less than 0.9 μm and experience sudden sharp increases which make device performance degrade and reach their operating limits when the channel length is further lessened down to 0.5 μm. The results demonstrate the usefulness of short channel simulations for designs and optimization of next-generation electrical and photonic devices.

1. Introduction

$In_{0.53}Ga_{0.47}As$ alloys with higher electron mobility are ideal channel materials to implement metal-oxide-semiconductor filed effect transistors (MOSFETs) [1, 2]. $In_{0.53}Ga_{0.47}As$ is believed to be easier to obtain unpinned surface Fermi level and thus can potentially provide better transistor performances compared to other III-V materials. At present, low dimensional nanoscaled III-V semiconductor MOSFETs have received particular attention for their potential applications in photodetectors and solar cells [3–10]. As MOSFET scaling approaches physical and technical limits, various specific gate oxides and passivation techniques have been developed to further increase the device performance of $In_{0.53}Ga_{0.47}As$ MOSFETs. Among them, silicon interface passivation layer (IPL) technique has been successfully employed where silicon IPL acts as a barrier layer to prevent reactions between oxygen and $In_{0.53}Ga_{0.47}As$ layer [11]. The bonds between oxygen and Ga atoms which are closely associated with interface states are replaced by Ga-Si and As-Si bonds during the growth of silicon interface layer [12]. Another functional layer, Ga_2O_3, Al_2O_3, or HfO_2, is also usually deposited as gate oxide in MOSFET structures to improve drain currents [13]. High performance $In_{0.53}Ga_{0.47}As$ MOSFET with silicon IPL and HfO_2 gate oxide has been demonstrated experimentally. However, quantitative analysis of device behavior of this kind of MOSFET is still further needed.

In this paper, the electrical characteristics of nanoscaled $In_{0.53}Ga_{0.47}As$ MOSFET grown with Si IPL and high k gate oxide HfO_2 layer are investigated. The effects of various parameters, such as thickness of Si IPL and HfO_2 layers and thickness and doping concentration of drain and source areas, on drain current and I_{off} are systematically analyzed. Changes of threshold voltage, subthreshold characteristics

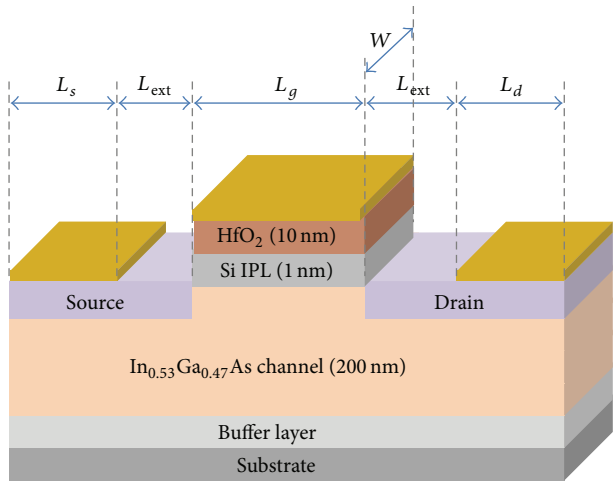

FIGURE 1: Schematic device structure of $In_{0.53}Ga_{0.47}As$ MOSFET.

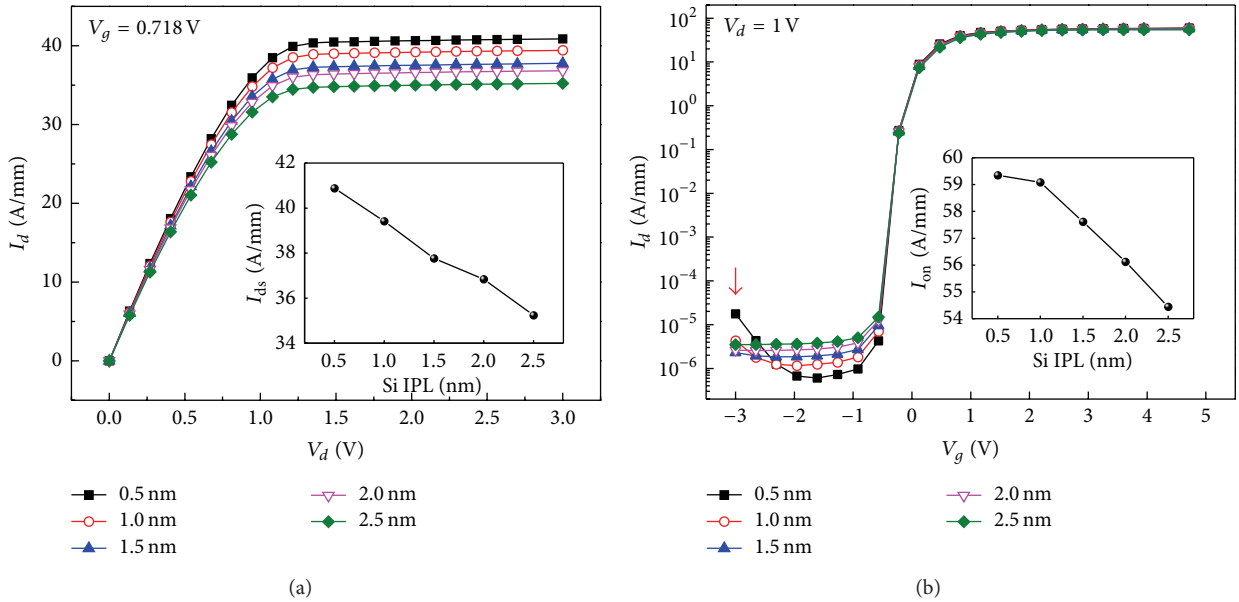

FIGURE 2: Si IPL thickness dependence on output (a) and transfer (b) characteristics.

translation, and saturation region due to short-channel effect caused by decrease of $In_{0.53}Ga_{0.47}As$ channel length are also investigated.

2. Method and Device Structure

Schematic device structure of the $In_{0.53}Ga_{0.47}As$ MOSFET is shown in Figure 1. The thickness of unintentionally doped $In_{0.53}Ga_{0.47}As$ channel layer, silicon IPL, and HfO_2 gate oxide layer is 200 nm, 1 nm, and 10 nm, respectively. All the lengths of gate L_g, source L_s, and drain L_d are equal to 5 μm. The extended length L_{ext} between source and drain contacts is 10 μm. The doping concentration in source and drain areas is $5 \times 10^{18}/cm^3$. The transverse width of this MOSFET W is 600 μm. Physical models applied in our simulation include drift-diffusion equation, band gap narrowing (OldSlotboom), doping-dependent degradation and high field saturation for mobility, Fowler-Nordheim tunneling model for gate leakage current, and Shockley-Read-Hall (SRH) recombination models [14].

3. Results and Discussion

Figure 2 shows output and transfer characteristics with a thickness of Si IPL varying from 0.5 nm to 2.5 nm at a fixed gate or drain voltage. Maximum drain current, I_{ds}, increases linearly with the decrease of thickness of Si IPL as shown in the first inset. This increase can be accounted for by the increase of electric field strength under gate electrode with decrease of thickness of Si IPL, which subsequently raises the electron concentration induced in $In_{0.53}Ga_{0.47}As$ channels. The interpretation can also explain the increase of power-up

current I_{on} and leakage current I_{off} with decrease of thickness of Si IPL in the transfer characteristics curves in the second inset. Simultaneously, the effect of Si IPL as a barrier layer between oxygen and $In_{0.53}Ga_{0.47}As$ layers may be diminished by the decrease of its thickness. The significant increases of I_{off} when the gate voltages V_g approach larger negative voltages, as the arrow indicates, are attributed to the depletion in the drain area close to gate electrode in $In_{0.53}Ga_{0.47}As$ channels, which increases tunneling probability of carriers between drain and gate electrode [15]. Therefore, the determination of thickness of Si IPL should be a result of compromise between drain currents and role of a barrier layer. A value between 1.0 nm and 1.5 nm is suggested to be set for the thickness of Si IPL based on above simulation results.

Figure 3 shows output and transfer characteristics with a thickness of gate oxide HfO_2 layer varying from 5 nm to 25 nm at a fixed gate or drain voltage. Due to the variation of electric field strength under gate electrode, maximum drain current I_{ds} and power-up current I_{on} increase with decrease of thickness of HfO_2 layer. Stronger I_{ds} and I_{on} are beneficial to improving device performance of $In_{0.53}Ga_{0.47}As$ MOSFETs. Leakage current I_{off} also exhibits sharp increase with decrease of thickness of HfO_2 layer as explained in Figure 2, especially when the thickness is reduced to 5 nm. This occurrence is not desired to improve device performance. Based on these results, an ideal value of thickness of HfO_2 layer should be kept larger than 10 nm.

Figure 4 shows influences of doping depth of source and drain layer on output and transfer characteristics at a fixed gate or drain voltage. The decrease of doping depth of source and drain layers leads to a decrease of maximum drain current I_{ds} and an increase of turn-on voltage V_{on}. The former decrease is negative for device development, whereas the latter increase is desired for it is helpful to enlarge the linear operation zone of $In_{0.53}Ga_{0.47}As$ MOSFETs. Different from the aforementioned effects of Si IPL thickness and HfO_2 thickness, the doping depth of source/drain layer has obvious influence on I_{on} instead of I_{off}. I_{on} increases quickly with increase of doping depth. Therefore, a larger doping depth in source and drain layers is preferred for improving device performance. However, increase of doping depth is restricted by the geometrical sizes of $In_{0.53}Ga_{0.47}As$ MOSFETs themselves.

Figure 5 shows influences of doping concentration of source and drain layer on output and transfer characteristics at a fixed gate or drain voltage. The increase of doping concentration produces a desired increase of maximum drain current I_{ds} and an undesired decrease of turn-on voltage V_{on}. As a result for balance between I_{ds} and V_{on}, a middle-value doping concentration is preferred in practice. When the doping concentration increases ten times from $5 \times 10^{18}/cm^3$ to $5 \times 10^{19}/cm^3$, I_{ds} only increases about 40%, indicating that impurity scattering which inhibits electrical current increasing begins to dominate [16]. Here, the doping concentration of source/drain layer also has obvious influence on I_{on} instead of I_{off} as previous doping depth.

Figure 6 shows influences of channel length on output and transfer characteristics at a fixed gate or drain voltage.

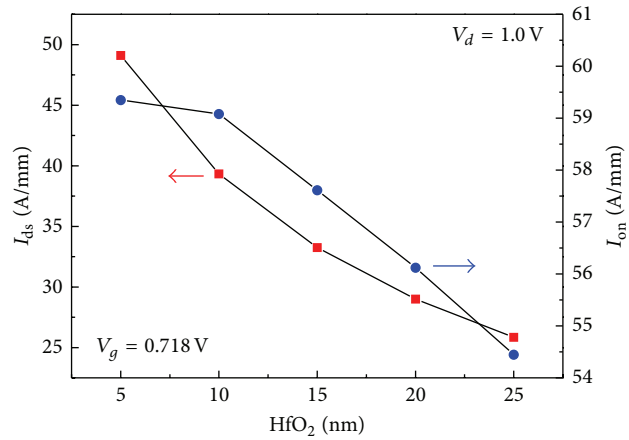

Figure 3: Gate oxide HfO_2 thickness dependence on output and transfer characteristics.

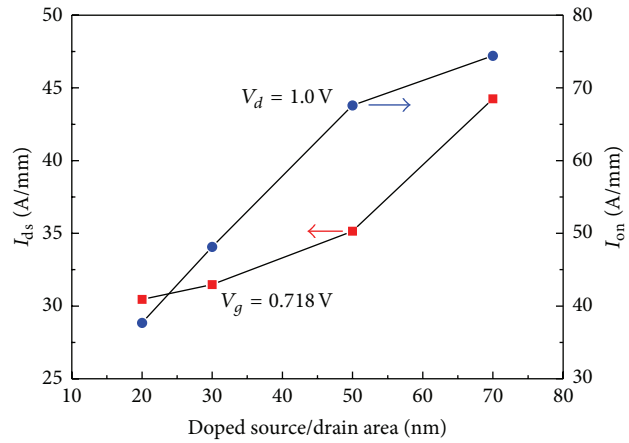

Figure 4: Source/drain layer doping depth dependence on output and transfer characteristics.

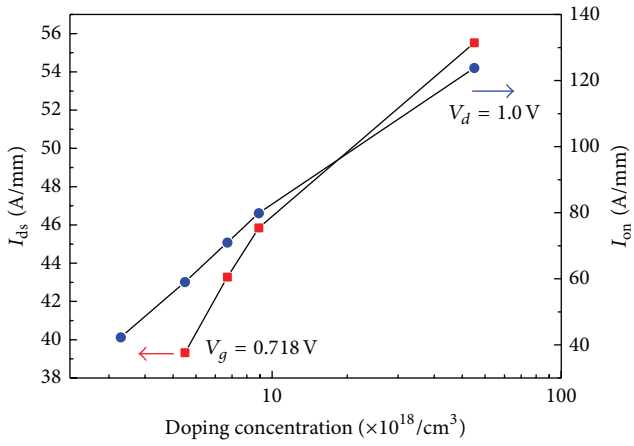

Figure 5: Source/drain layer doping concentration dependence on output and transfer characteristics.

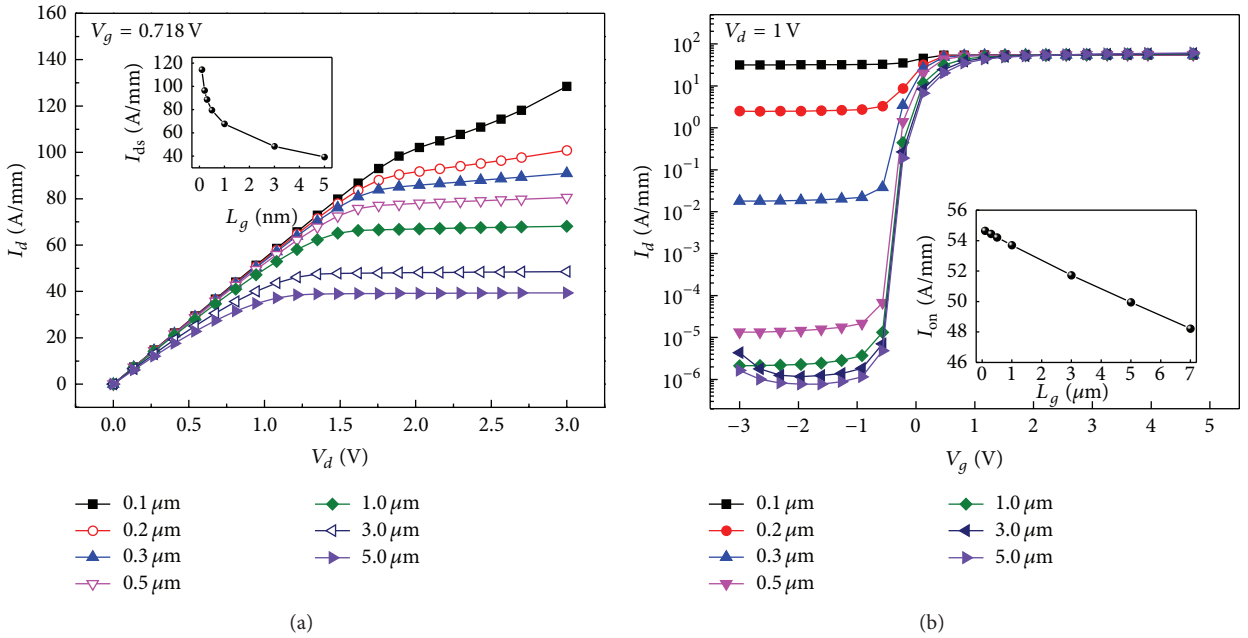

FIGURE 6: Channel length dependence on output (a) and transfer (b) characteristics.

Saturated drain current I_{ds} and saturated voltage V_s both increase with the decrease of channel length. The appearance of saturated drain current is a result of unvaried pinch-off voltage at the point where the potential drop across the oxide at the drain terminal is equal to threshold voltage V_T. When the channel length is further lessened down from 0.5 μm to 0.1 μm, the depletion region at the drain terminal extends laterally into the channel, reducing the effective channel length and causing the drain current to be no more saturated. This is the so-called channel length modulation that drain currents begin to move upward with increase of drain voltage when the channel length is substantially shortened as Figure 6(a) illustrates. Meanwhile, the reduction of channel length causes the drain terminate to be closer to source terminate, producing an obvious increase of leakage current I_{off} and weaker effect of gate electrode on drain currents, as Figure 6(b) shows. Power-up current I_{on} shows a linear relationship with channel length. This is consistent with previous reports [14].

Figure 7 shows influences of channel length on threshold voltage V_T and subthreshold characteristics ∇V_T at a fixed drain voltage. A transverse shift of subthreshold characteristics ∇V_T is observed for different channel lengths, an important feature of drain induced barrier lowing (DIBL) effect. The DIBL effect is a result of increase of injected electrons from source area to channel induced by lowering of potential barrier height between drain and source electrodes when the channel length is lessened [17]. The shift of subthreshold characteristics ∇V_T starts to become most obvious and the device performance degrades quickly when the channel length is lessened down to a critical value of 0.5 μm, much bigger than that of Si-based npn MOSFETs [18, 19]. In the InGaAs-based MOSFETs, the channel layer InGaAs is unintentionally doped whereas the channel layer in Si-based devices is p-type doped,

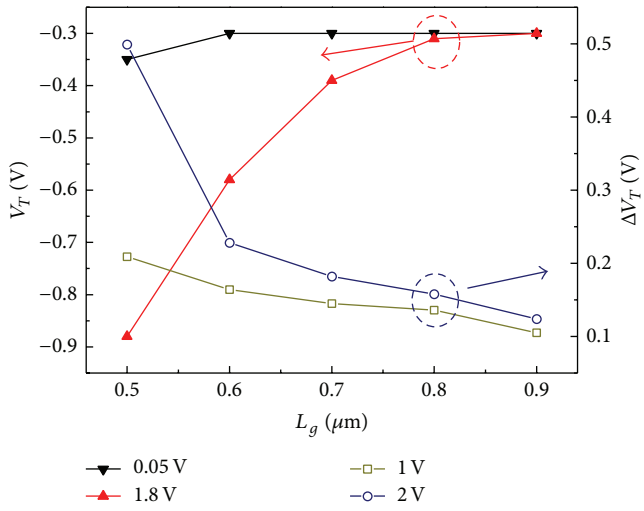

FIGURE 7: Channel length dependence on threshold voltage and shift of subthreshold characteristics.

which will induce less Fermi energy difference between drain and source electrodes. Then the corresponding potential barrier height in the InGaAs MOSFETs is comparatively smaller than that of Si-based MOSFETs [20–22]. This is the physical mechanism where DIBL effect is much obvious in the InGaAs MOSFETs. Threshold voltage V_T experiences a similar sudden decrease when the channel length is lessened down to the same value of 0.5 μm. These results mean that the InGaAs MOSFETs start to show short channel effect at a value of 0.9 μm of channel length and reach their operating limits when the channel length is further lessened down to 0.5 μm.

4. Conclusion

In conclusion, the electrical characteristics of $In_{0.53}Ga_{0.47}As$ MOSFET grown with Si IPL and high k gate oxide HfO_2 layer have been investigated in detail. The decrease of Si IPL thickness and gate oxide HfO_2 thickness is beneficial to improving device performance by increasing the maximum drain current. However, rather small Si IPL thickness and gate oxide HfO_2 thickness result in sharp increase of leakage current and device performance degradation. The increase of source and drain layer doping depth brings about larger maximum drain current and almost has little negative influence on saturated voltage and leakage current. Unfortunately, increase of doping depth is limited by the geometrical size of MOSFETs themselves. The increase of source and drain layer doping concentration also has dual influences. On the one hand, it helps to improve the maximum drain current. On the other hand, it produces a lowered saturated voltage and smaller device linear operating limits. The decrease of channel length increases the maximum drain current and leakage current simultaneously. Short channel effects start to appear when the channel length is lessened down to about 0.9 μm and experience sudden sharp increases which make device performance degrade and reach their operating limits when the channel length is further lessened down to 0.5 μm.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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