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Research Article

Transformation of Holes Emission Paths under Negative Bias Temperature Stress in Deeply Scaled pMOSFETs

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We examine the impact of negative bias temperature (NBT) stress on the fluctuations in I_D and I_G for deeply scaled pMOSFETs and find that the relative high NBT stress triggers I_G-RTN and I_D-step. Through the analysis of the field dependence of emission constant and the carrier separation measurement, it is found that under the relative high NBT stress some traps keep charged state for very long time, as observing step-like behaviors in I_D, while other traps emit charged holes to the gate side through TAT process, which originate both I_D-step and ID-RTN.

1. Introduction

Negative bias temperature instability (NBTI) degradation is one of the most important reliability issues in modern complementary metal-oxide-semiconductor (CMOS) technologies [1–7]. Recently, much attention has been paid to NBTS generated oxide traps, which could significantly increase the failure probability in deeply scaled pMOSFETs. Furthermore, these traps are currently considered to not only cause the V_{th} degradation but also increase the gate leakage current (I_G) [8–10]. However, someone considers the I_G fluctuations are probably not to be explained as the results of NBT induced switching traps [11–13]. Tsujikawa reported that the observed transient I_G and I_D signal simultaneously in small size pMOS devices are not linked directly with each other [11]. Wagner et al. [12] pointed out that the increases of I_G fluctuation are probably caused by the beginning of oxide breakdown which should not be explained as the results of NBT induced switching trap while Gao et al. [14] have reported that I_G increases only when part of the switching hole traps transform to the permanent bulk traps with increasing NBT stress or stressing time. To date, the impact of negative bias temperature stress condition on I_D and I_G fluctuation has not been systematically evaluated yet.

In this paper, we examine the impact of stress on the I_G-RTN and I_D-RTN for deeply scaled pMOSFETs, using carrier separation measurement to identify the type of I_G-RTN. The characteristic of time constants and amplitude in RTN under the various stress regions is investigated and a trap-assisted tunneling model through NBT stress-induced switching traps is proposed to explain the mechanism of I_G-RTN. The results illustrate that, under the relative high NBT stress, at least some of the holes are discharged from the traps to the gate side.

2. Experiment

Plasma nitric oxide (PNO) pMOSFETs used in this study were fabricated with a standard CMOS process technology. The devices size ($L \times W$) is 30 nm × 70 nm and dielectric thickness is about 2.6 nm. And the I_D-V_G curve of this device is shown in the inset of Figure 1. The measurements were conducted using a Keithley 4200 semiconductor characterization

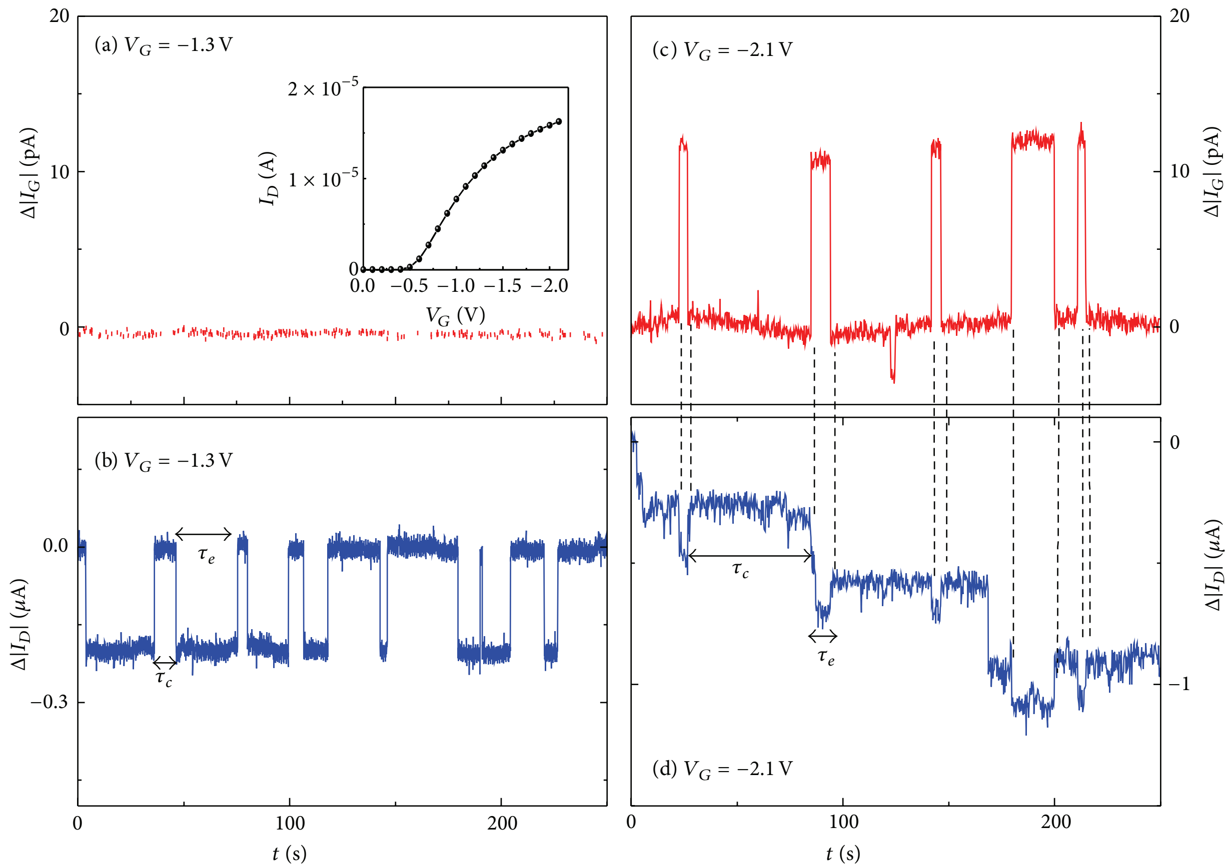

FIGURE 1: The time trace of I_G and I_D fluctuation under the gate voltage V_G of −1.3 V and −1.9 V with V_{DS} of 50 mV. The inset shows the I_D-V_G curve of the experimental device.

system and a Cascade Summit 12000 probe station with a built-in temperature controller.

3. Result and Discussion

Figure 1 shows the time traces of I_G and I_D monitored simultaneously under the relative low ($V_G = -1.3$ V, $E_{ox} = 3.1$ MV/cm) and high ($V_G = -2.1$ V, $E_{ox} = 6.2$ MV/cm) NBT with V_{DS} of 50 mV at room temperature stress for pMOSFETs. I_D-RTN is clearly detected in both cases, which should be contributed by the traps in the gate oxide layer. But there are two major differences between the two stress conditions. One is that the higher stress voltage triggers I_G-RTN, which has the strong reverse correlation with I_D-RTN; for example, the low drain current RTN level corresponds to the high gate current RTN level. The correlation suggests that I_G-RTN and I_D-RTN share the same traps induced by NBT stress, or a trapped hole results in the simultaneous increase in I_G and decrease in I_D under the relatively high NBT stress condition.

By using the carrier separation measurement as shown in Figure 2, the drain and source electrodes were connected together and the gate electrode was biased under the stress condition [15–17]. In that case, the I_G current could be divided into hole (source/drain) part and electron (substrate) part. The hole current, electron current, and I_G components could be monitored simultaneously with the stress time. We could find several RTN fluctuations in the traces of I_{Hole} and I_G and no obvious RTN fluctuations in the $I_{electron}$ trace as shown in Figure 3. Moreover, it could be seen that the RTN fluctuations in the traces of I_{Hole} have almost same amplitude

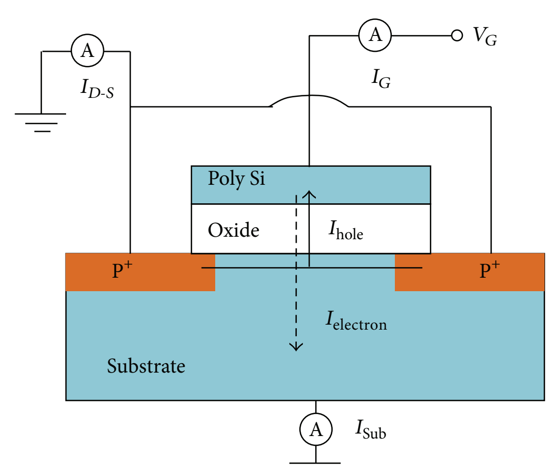

FIGURE 2: Configuration of the circuit diagram in carrier separation measurements. The gate electrode is biased for the stress condition, and drain and source electrodes are connected together.

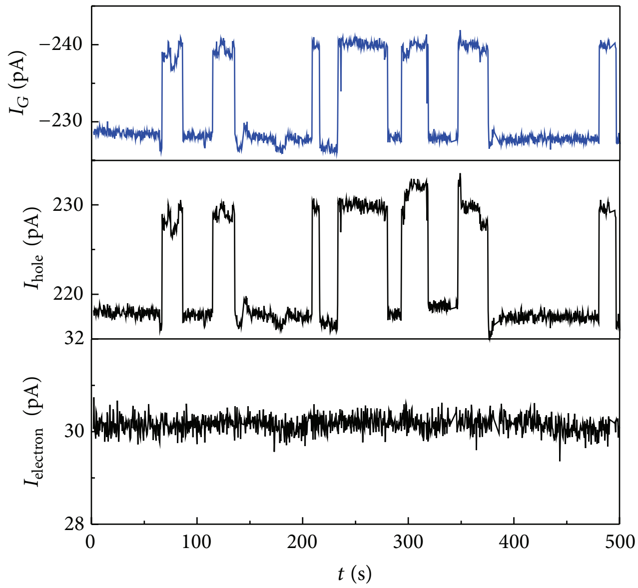

Figure 3: The time traces of gate current, electron current, and hole current under NBT stress (−1.9 V) at $T = 320$ K by using carrier separation technique.

and synchronize with that in the I_G trace. Therefore, holes are the major contributors to I_G-RTN. To conclude, the switching hole trap generated in high NBT stress could induce a larger amount of hole from channel to gate.

Another major difference for the two stress conditions is the electrical behaviors of I_D-RTN. Figure 4 shows the field dependence of the average value of capture time (τ_c) and emission time (τ_e) for the I_D-RTN within the gate voltage of (−1.0 V∼ −1.3 V) and (−1.8 V∼ −2.1 V). The average values of τ_c and τ_e are obtained from the exponential distribution of the single τ_c and τ_e. As shown in Figure 4(a), for the low stress range, τ_c and τ_e are found to exponentially decrease and increase with V_G, respectively. As shown in Figure 4(b), for the high stress range, τ_e keeps weakly dependent with the field even though τ_c exhibits similar behaviours as these observed in the low stress. The strong field dependence of both τ_c and τ_e in I_D-RTN under low stress could be explained by the extended nonradiative multiphonon (eNMP) theory [18–22]. In this theory, when the negative gate bias is applied for pMOSFETs, the switching trap states can be created from Si-Si precursors in the oxide state by capturing a hole via a multiphonon emission (MPE) process [18, 20]. The increase of the gate field results in a lower MPE barrier. The latter enhances the charge transfer reaction, leading to the dramatic reduction of hole capture time, which could be described as follows [23–25]:

$$\tau\left(\Delta E_B, F_{\mathrm{OX}}, F_C\right) = \tau_0 \cdot \exp\left(\frac{\Delta E_B}{KT}\right) \cdot \exp\left(-\frac{F_{\mathrm{ox}}^2}{F_c^2}\right). \quad (1)$$

Here ΔE_B is the multiphonon emission (MPE) barrier for hole capture, F_{ox} is the applied field in the oxide layer, and F_c is the characteristic field in MPFAT process. The red solid lines in Figure 4(a) present the fitting results with F_c being about 2.5 MV/cm which is analogous to that measured in NBTI [20, 26]. On the other hand, increasing the stress field will raise the hole traps' energy level and prevent the hole back to channel, which finally increases the emission time of RTN which is corresponding to the result in the low stress range.

However the electrical behaviour of τ_e in the high stress range is hard to be explained by this theory. One possible explanation is that the hole emission from trap is not to the Si substrate side but to the gate side by tunneling [27, 28]. In this case, increasing the stress field not only could prevent the hole back to channel but also will encourage it to be emitted to gate, which finally results in a weakly field dependence. Therefore, these switching traps behave as hole current path from channel to gate at high gate bias, which is consistent with the reverse correlation of I_D and I_G-RTN.

For verifying the current path induced by switching traps under high gate bias, the field and temperature dependence of the I_G-RTN is measured. As shown in the inset of Figure 5, the extremely weak temperature dependence was observed in ΔI_G, which is the typical behavior of elastic tunneling. In one-step elastic TAT model, channel charges could tunnel to gate side with the assistance of a trap in oxide. And the TAT probability in the model is described as [27, 29]

$$I_{\mathrm{TAT}} = AF_{\mathrm{OX}}^2 \cdot \left(\frac{\Phi_T}{xF_{\mathrm{OX}}}\right) \cdot \left(\frac{2\Phi_T}{xF_{\mathrm{OX}}} - 1\right) \cdot \exp\left(-\frac{8\pi\sqrt{2m_{\mathrm{OX}}}\Phi_T^{3/2}}{3hqF_{\mathrm{OX}}} \cdot \left[1 - \left(1 - \frac{xF_{\mathrm{OX}}}{\Phi_T}\right)^{3/2}\right]\right). \quad (2)$$

Here Φ_T is the energy depth of the trap from the valence band of dielectric, m_{ox} is the hole effective mass in dielectric, F_{ox} is electric field in oxide, and x is the trap's distance from the interface of gate and oxide. When $x = 1.5$ nm and $\Phi_T = 4$ V, it is observed that it provides a good description of the experimental data in Figure 5, which verifies that these switching traps could perform as hole tunneling paths.

Finally, the step-like fluctuations detected in Figure 1(b) are investigated. To avoid the mixture of several fluctuations, we selected the device which has only one active trap under the measurement condition. The gate voltage dependence of Id fluctuation of this trap is measured. Under the high bias of −1.7 V, the emission of the carriers from the trap is not detected until the end of measurement time of 300 s. Therefore the step-like behavior at −1.7 V is presented. When the gate bias is reduced from −1.7 V to −1.5 V, the emission of carriers from the trap occurs at about 210 s and the emission time (τ_e) is about 170 s. Further decreasing the gate bias reduces the emission time to about 70 s at $V_G = -1.4$ V and about 10 s at $V_G = -1.2$ V (Figure 6). The voltage dependence of the emission time observed here is consistent with the field behaviors of I_D-RTN in Figure 4(a). The results clearly inform that I_D-RTN transforms to I_D-step when the gate bias is increased. In other words, both I_D-step and I_D-RTN are originated from the switching traps.

According to the above analyses, I_G-RTN, I_D-RTN, and I_D-step observed in NBTI degradation are due to the generated NBT traps. Under the relatively low NBT stress, the

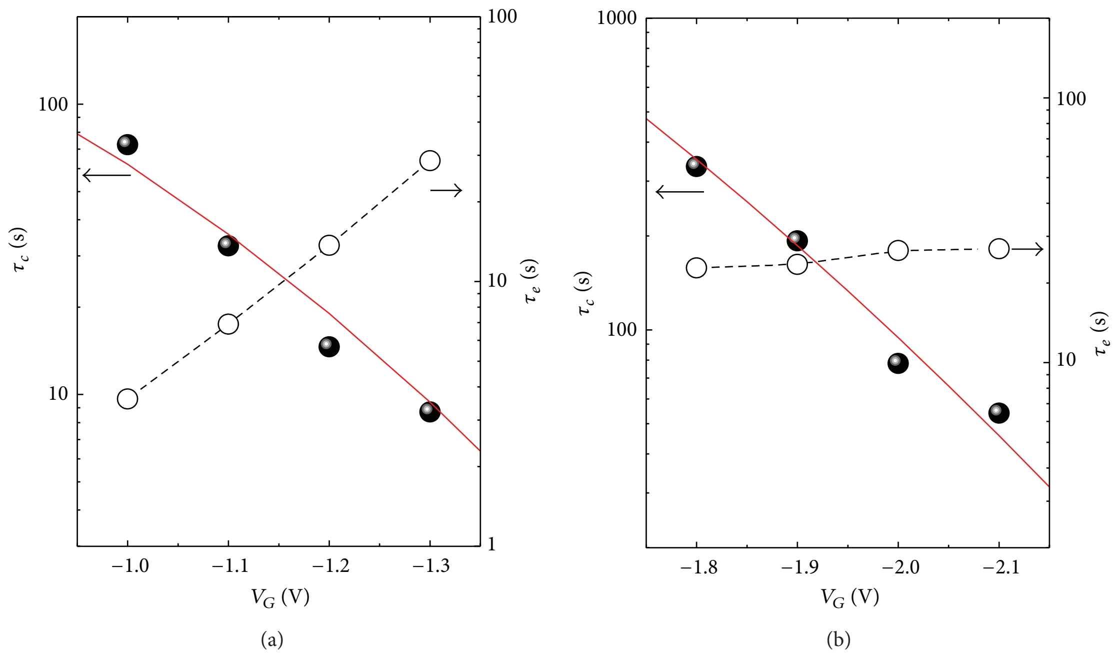

FIGURE 4: Field dependence of the average value of τ_c and τ_e of the RTN under (a) higher and (b) lower gate bias regions. The red lines present MPFAT simulation results for τ_c.

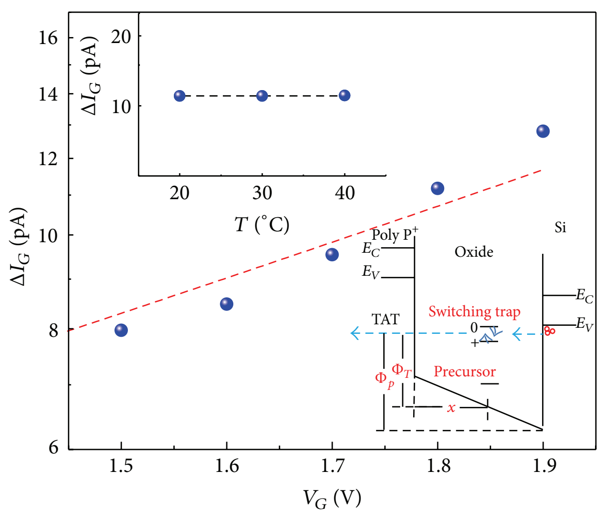

FIGURE 5: The field dependence of ΔI_G amplitude. The red dash line presents the simulation results by trap-assisted tunneling (TAT) modeling. The inset shows temperature behaviors of ΔI_G.

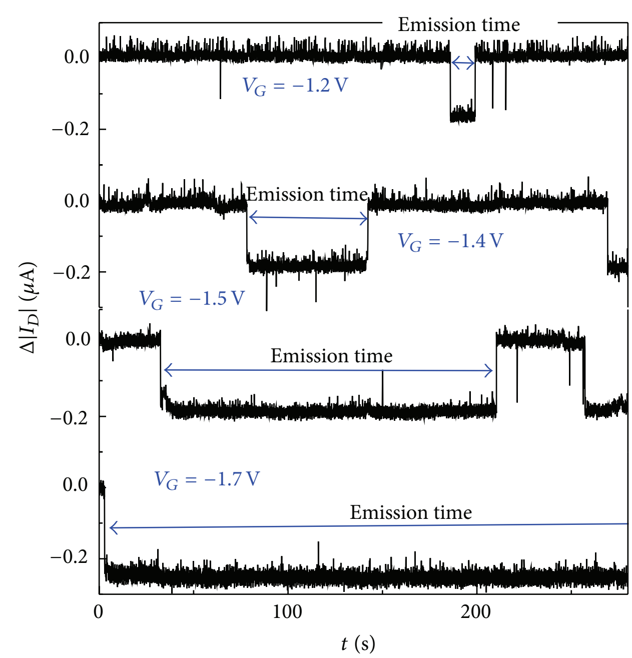

FIGURE 6: The transformation of transience signal from I_D-Step to I_D-RTN could be seen by decreasing the gate bias from −1.7 V to −1.5 V. And the emission time of this trap is obviously decreased from larger than 300 s to about 10 s when gate bias is decreased from −1.7 V to −1.2 V.

generated traps exchange holes with channel as shown in Figure 7(a), which induces the RTN fluctuations in I_D. Under the high NBT stress, larger oxide field raises the hole traps' energy level and prevents the hole back to channel. Some traps keep charged state for very long time, as observing step-like behaviors in I_D, while the other traps emit charged holes to the gate side through TAT process as shown in Figure 7(b). In the latter case, the hole current path from channel to gate is formed. As a result, RTN fluctuations in I_G are detected.

4. Conclusions

In this paper, the fluctuations including I_G-RTN, I_D-RTN, and I_D-step are studied under various NBT stress. Note

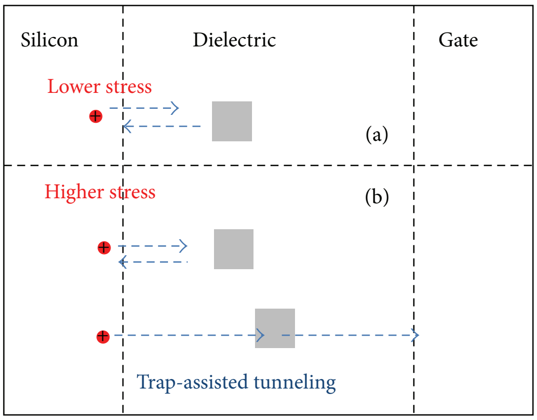

FIGURE 7: Schematic view of the switching traps in pMOSFETs. Under low gate bias, the switching traps in oxide layer could only be recovered by exchanging hole with channel and induce only I_D-RTN. Under the high gate bias, part of generated switching traps can capture and hold the hole while some others transform the hole from the channel to gate by TAT mechanism.

that, under the relative low NBT stress, only I_D-RTN could be detected while under the relative high NBT stress the I_D-RTN, I_G-RTN, and I_D-step are observed. Through the analysis of the field dependence of emission constant and the carrier separation measurement, it is found that under the relative high NBT stress some traps keep charged state for very long time, as observing step-like behaviors in I_D, while other traps emit charged holes to the gate side through TAT process, which originate both I_D-step and I_D-RTN.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

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References

[1] K. O. Jeppson and C. Svennson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," *Journal of Applied Physics*, vol. 48, no. 5, pp. 2004–2014, 2004.

[2] S. Ogawa and N. Shiono, "Generalized diffusion-reaction model for the low-field charge-buildup instability at the Si-SiO_2 interface," *Physical Review B*, vol. 51, p. 4218, 1995.

[3] C. R. Parthasarathy, M. Denais, V. Huard et al., "Designing in reliability in advanced CMOS technologies," *Microelectronics Reliability*, vol. 46, no. 9-11, pp. 1464–1471, 2006.

[4] H. C. Ma, J. P. Chiu, C. J. Tang, T. Wang, and C. S. Chang, in *Proceedings of the International Reliability Physics Symposium*, 2009.

[5] D. K. Schroder, "Negative bias temperature instability: what do we understand?" *Microelectronics Reliability*, vol. 47, no. 6, pp. 841–852, 2007.

[6] V. Huard, C. Parthasarathy, C. Guerin et al., "NBTI degradation: from transistor to SRAM arrays," in *Proceedings of the 46th IEEE International Reliability Physics Symposium*, pp. 289–300, May 2008.

[7] B. Kaczer, T. Grasser, P. J. Roussel et al., "Origin of NBTI variability in deeply scaled pFETs," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 26–32, May 2010.

[8] M. Toledano-Luque, B. Kaczer, E. Simoen et al., "Correlation of single trapping and detrapping effects in drain and gate currents of nanoscaled nFETs and pFETs," in *Proceedings of the IEEE International Reliability Physics Symposium (IRPS '12)*, pp. XT.5.1–XT.5.6, IEEE, Anaheim, Calif, USA, April 2012.

[9] X. Ji, Y. Liao, C. Zhu et al., "The physical mechanisms of IG random telegraph noise in deeply scaled pMOSFETs," in *Proceedings of the IEEE International Reliability Physics Symposium (RPS '13)*, pp. XT.7.1–XT.7.5, Anaheim, Calif, USA, April 2013.

[10] R. Degraeve, T. Kauerauf, M. Cho et al., "Degradation and breakdown of 0.9 nm EOT SiO_2 ALD HfO_2 metal gate stacks under positive constant voltage stress," in *Proceedings of the IEEE International on Electron Devices Meeting, IEDM Technical Digest*, pp. 408–411, Washington, DC, USA, December 2005.

[11] S. Tsujikawa, "SILC and NBTI in pMOSFETs with ultrathin SiON gate dielectrics," *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 524–530, 2007.

[12] P.-J. Wagner, B. Kaczer, A. Scholten et al., "On the correlation between NBTI, SILC, and flicker noise," in *Proceedings of the IEEE International Integrated Reliability Workshop (IIRW '12)*, pp. 60–64, October 2012.

[13] S. Tsujikawa and J. Yugami, "Evidence for bulk trap generation during NBTI phenomenon in pMOSFETs with ultrathin SiON gate dielectrics," *IEEE Transactions on Electron Devices*, vol. 53, no. 1, pp. 51–55, 2006.

[14] Y. Gao, D. S. Ang, C. D. Young, and G. Bersuker, "Evidence for the transformation of switching hole traps into permanent bulk traps under negative-bias temperature stressing of high-k P-MOSFETs," in *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 5A.5.1–5A.5.5, April 2012.

[15] W. Mizubayashi, N. Yasuda, H. Ota et al., "Carrier separation analysis for clarifying leakage mechanism in unstressed and stressed $HfAlO_x/SiO_2$ stack dielectric layers," in *Proceedings of the 42nd Annual IEEE International Reliability Physics Symposium*, Phoenix, Ariz, USA, April 2004.

[16] Y. Shi, T. P. Ma, S. Prasad, and S. Dhanda, "Polarity dependent gate tunneling currents in dual-gate CMOSFETs," *IEEE Transactions on Electron Devices*, vol. 45, no. 11, pp. 2355–2360, 1998.

[17] S.-I. Takagi, N. Yasuda, and A. Toriumi, "Expérimental evidence of inelastic tunneling in stress-induced leakage current," *IEEE Transactions on Electron Devices*, vol. 46, no. 2, pp. 335–341, 1999.

[18] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "A two-stage model for negative bias temperature instability," in *Proceedings of the IEEE International Reliability Physics Symposium (IRPS '09)*, pp. 33–44, IEEE, Montreal, Canada, April 2009.

[19] C. H. Henry and D. V. Lang, "Nonradiative capture and recombination by multiphonon emission in GaAs and GaP," *Physical Review B*, vol. 15, no. 2, p. 989, 1977.

[20] V. Huard, in *Proceedings of the International Reliability Physics Symposium*, 2010.

[21] G. Richard, B. William, B. Kaczer, and T. Grasser, "On the thermal activation of negative bias temperature instability," IIRW Final Report 36, 2009.

[22] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, in *Proceedings of the IEEE International Reliability Physics Symposium*, 2010.

[23] T. Grasser, H. Reisinger, W. Goes et al., "Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise," in *IEEE International Electron Devices Meeting*, pp. 1–4, 2009.

[24] S. Makram-Ebeid and M. Lannoo, "Quantum model for phonon-assisted tunnel ionization of deep levels in a semiconductor," *Physical Review B*, vol. 25, no. 10, pp. 6406–6424, 1982.

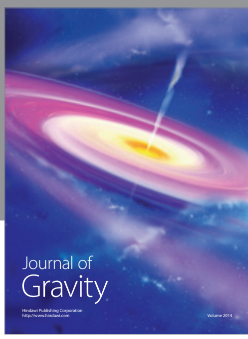
[25] S. D. Ganichev, W. Prettl, and I. N. Yassievich, "Deep impurity-center ionization by far-infrared radiation," *Physics of the Solid State*, vol. 39, no. 11, pp. 1703–1726, 1997.

[26] X. Ji, Y. Liao, F. Yan, Y. Shi, G. Zhang, and Q. Guo, "The energy distribution of NBTI-induced hole traps in the Si band gap in PNO pMOSFETs," in *Proceedings of the IEEE International Reliability Physics Symposium (IRPS '12)*, XT.12.5, p. XT.12.1, Anaheim, Calif, USA, April 2012.

[27] F. Schuler, R. Degraeve, P. Hendrickx, and D. Wellekens, "Physical charge transport models for anomalous leakage current in floating gate-based nonvolatile memory cells," *IEEE Transactions on Device and Materials Reliability*, vol. 2, no. 4, pp. 80–88, 2002.

[28] M. O. Andersson, Z. Xiao, S. Norrman, and O. Engström, "Model based on trap-assisted tunneling for two-level current fluctuations in submicrometer metalsilicon-dioxidesilicon diodes," *Physical Review B*, vol. 41, no. 14, pp. 9836–9842, 1990.

[29] R. Degraeve, F. Schuler, B. Kaczer et al., "Analytical percolation model for predicting anomalous charge loss in flash memories," *IEEE Transactions on Electron Devices*, vol. 51, no. 9, pp. 1392–1400, 2004.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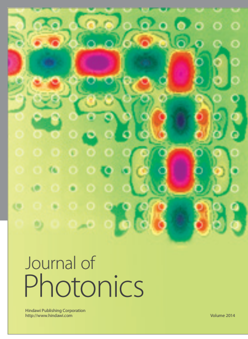
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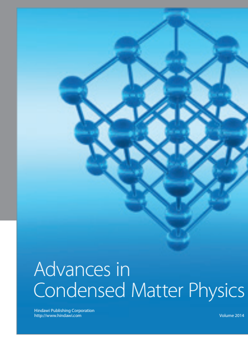
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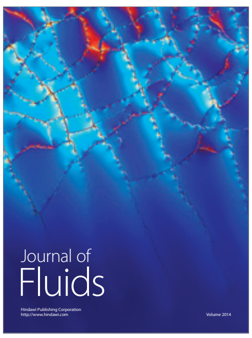
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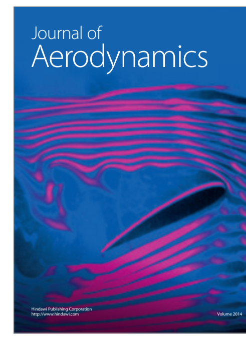
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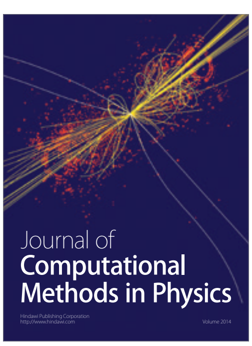
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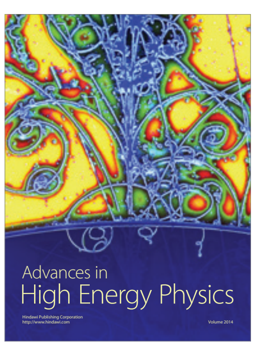
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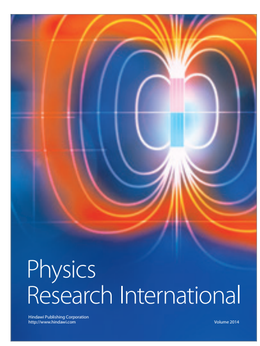
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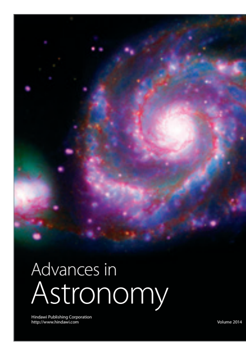
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