Hindawi Publishing Corporation
Advances in Condensed Matter Physics
Volume 2015, Article ID 639218, 9 pages
http://dx.doi.org/10.1155/2015/639218

Review Article

Interface Engineering and Gate Dielectric Engineering for High Performance Ge MOSFETs

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Received 3 October 2014; Accepted 1 December 2014

Academic Editor: Rui Zhang

In recent years, germanium has attracted intensive interests for its promising applications in the microelectronics industry. However, to achieve high performance Ge channel devices, several critical issues still have to be addressed. Amongst them, a high quality gate stack, that is, a low defect interface layer and a dielectric layer, is of crucial importance. In this work, we first review the existing methods of interface engineering and gate dielectric engineering and then in more detail we discuss and compare three promising approaches (i.e., plasma postoxidation, high pressure oxidation, and ozone postoxidation). It has been confirmed that these approaches all can significantly improve the overall performance of the metal-oxide-semiconductor field effect transistor (MOSFET) device.

1. Introduction

After continuously pursuing higher performance complementary metal-oxide-semiconductor field effect transistor (MOSFET) devices for more than four decades, it is becoming increasingly difficult for Si-based MOSFET to enhance performance through traditional device scaling [1–5]. Recently, Ge has attracted intensive interests as the most promising channel material for next generation MOSFET because of the intrinsic higher carrier mobility in Ge than that in Si (2x higher mobility for electrons and 4x for holes) [6–14]. In order to realize high performance Ge p-type MOSFETs, advanced high-k/Ge gate stacks with scaled EOT and superior MOS interfaces are mandatory [15, 16]. Electrically active defects on the Ge surface and Ge/oxide interfaces are suspected as the probable cause of the mobility degradation of performance characteristics in MOSFETs. Hence, high quality MOS interfaces are not guaranteed due to the large amount of defects at direct high-k/Ge interfaces [17]. To solve this problem, an interfacial layer (IL) is introduced between the high-k layer and the Ge substrate, which can provide effective electrical passivation of the Ge surface. Among a variety of ILs, high quality GeO_2 has been considered as the most promising choice due to its extremely low interface defect density D_{it} (~$6 \times 10^{10}\,cm^{-2}eV^{-1}$) [18] and its potential to enable high performance Ge n-MOSFETs [19]. But there is a problem: the formation of volatile GeO either during growth or at elevated temperatures around 550°C–600°C, which are often used in MOSFET processing. Initially it was believed that GeO is formed at the interface between GeO_2 and Ge. More experimental evidences though suggest that GeO is formed at the top surface of GeO_2 and desorbs at high enough temperature [20–22]. In addition, the relative dielectric constant (k-value) of GeO_2 is much lower than that of Hf- and La-based high-k gate dielectrics used for advanced Si technology [23–30]. This means that gate stacks containing thick interfacial GeO_2 layers are difficult to scale below 1 nm EOT as required for future technology nodes. Therefore, a high-k/GeO_2 IL/Ge gate stack with a high quality and ultrathin GeO_2 interfacial layer is obviously required to achieve subnanometer overall EOT in high performance Ge MOSFETs. The biggest challenge at present is how to manufacture, in a controlled manner, an ultrathin GeO_2 passivation layer without compromising its electrical quality.

The most promising route is to use well-controlled oxidation method to introduce the GeO_2 IL of very good quality. Recently, it has been reported that high quality GeO_2/Ge interfaces have been fabricated by thermal oxidation [31],

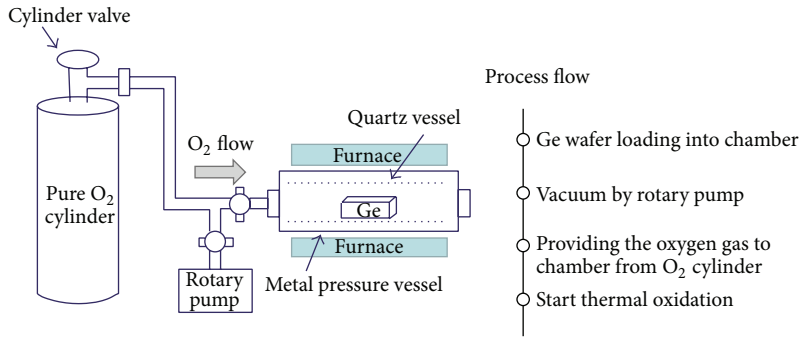

Figure 1: Schematic illustration of HPO system and process flow [35].

ozone oxidation [32], plasma oxidation [33], and so forth. Among them, high-temperature thermal oxidation [34] and ozone oxidation [35] can realize superior GeO_2/Ge MOS interfaces with a D_{it} value less than $5 \times 10^{11}\,cm^{-2}eV^{-1}$. Plasma postoxidation enables the formation of ultrathin GeO_x interfacial layer between high-k dielectrics and Ge, suitable for equivalent oxide thickness (EOT) scaling while keeping low D_{it} ($\sim 5 \times 10^{10}\,cm^{-2}eV^{-1}$) [33]. In this review, the three effective oxidation methods will be discussed in detail.

2. Ge/Dielectric Interface Passivation Methods

2.1. High-Pressure Oxidation. Many approaches were investigated to form a stable and desirable GeO_2 IL in high-k/Ge gate stack. One of the most effective methods was high-pressure oxidation. Lee et al. recently reported that the high-pressure oxidation (HPO) of germanium (Ge) for improving electrical properties of Ge/dielectric stacks was investigated [11, 34–39]. Figure 1 shows the schematic illustration of HPO system and the process flow used in their work. The system mainly composes of an oxygen cylinder, a vacuum pump, and a tube furnace. The furnace consists of a quartz oxidation tube enclosed in a steel pressure vessel.

During the process, the HPO system is evacuated to approximately 1 Pa by rotary pump after the cleaned Ge wafers are placed into quartz oxidation tube. Then, the furnace chamber surrounding the steel pressure vessel is heated to a thermal oxidation temperature. Temperature calibration of HPO furnace was carried out in the temperature range from 200°C to 600°C for precise measurements [35].

By applying the HPO method followed by low-temperature oxygen annealing (LOA), the interface state density was reduced to less than $10^{11}\,cm^{-2}eV^{-1}$ near the midgap, as shown in Figure 2. Moreover, the refractive index of thermally oxidized GeO_2 was increased by HPO which is indicating higher density of GeO_2 grown by HPO, as shown in Figure 3. It was also revealed that the dielectric constant of GeO_2 increases from 5.2 in the case of atmospheric-pressure oxidation (APO) to 5.8 in the case of HPO. With HPO method followed by LOA, Lee et al. also obtained the highest hole mobility of 725 cm^2/Vs in Ge/GeO_2 gate stack which is 3.5 times higher than (100) Si universal mobility. With this method, they also demonstrated the highest electron mobility

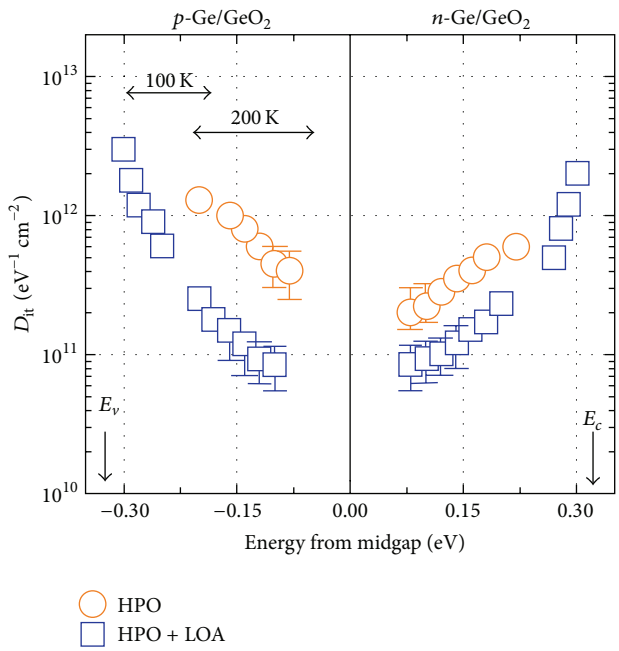

Figure 2: Energy distribution of the interface states density (D_{it}) estimated by the conductance method at 100 and 200 K. [37].

of 1920 cm^2/Vs in Ge/GeO_2/Y_2O_3 gate stack, as shown in Figure 4. Both are the record-high values of Ge MOSFETs, and this is a strong evidence that high quality Ge interface from conduction to valence band edge is possible by the Ge surface passivation. Discussed from a thermodynamic point of view, the GeO desorption from Ge/GeO_2 stacks could be efficiently suppressed by HPO.

Furthermore, by applying the combination of Y_2O_3 and low-temperature high-pressure oxidation (LT-HPO) method, Lee et al. also have demonstrated the peak mobility of 787 cm^2/Vs and high-N_s mobility (at $N_s = 1 \times 10^{13}\,cm^{-2}$) of 429 cm^2/Vs in Ge n-MOSFET with sub-nm EOT, which are the highest ones to date among scaled Si and Ge MOSFETs [38]. It is expected that electrical properties of GeO_2 metal-insulator-semiconductor capacitor (MISCAP) can be further improved by optimizing the oxidation temperature and oxygen pressure of HPO.

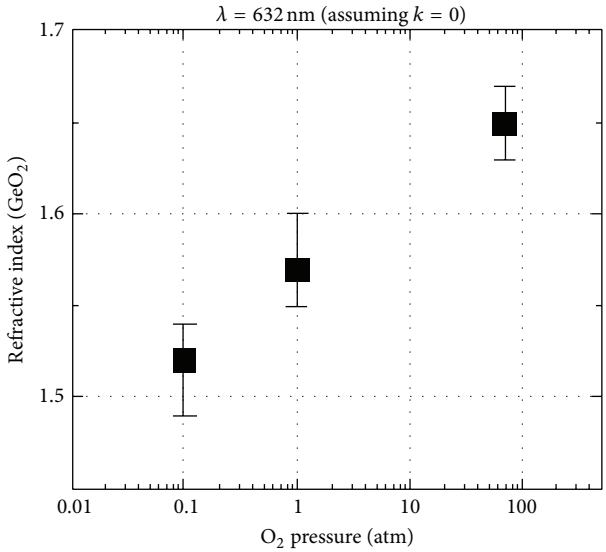

FIGURE 3: Refractive index (n) of GeO_2 films estimated by spectroscopic ellipsometry at λ of 632.8 nm under the assumption that the extinction coefficient is zero [35].

2.2. Plasma Postoxidation. O_2 plasma treatment is a very effective approach to form low defect GeO_2/Ge interfaces and GeO_2 IL at low substrate temperatures, due to the highly reactive O radicals [48, 49]. Zhang et al. have proposed a novel GeO_2 IL formation process by applying the electron cyclotron resonance (ECR) oxygen plasma to form high quality GeO_x ILs through a thin Al_2O_3 oxygen barrier, which can realize a low D_{it} and a thin EOT of around 1 nm at the same time [33]. The basic process flow is shown in Figure 5. In this plasma postoxidation method, a thin GeO_x IL is formed by oxidizing the Ge surface beneath a thin Al_2O_3 layer. The Al_2O_3 serves as a sufficient oxygen barrier which suppresses the growth of unnecessarily thick GeO_x IL. In more detail, an ultrathin (1–1.5 nm) Al_2O_3 layer is first deposited on Ge by atomic layer deposition, followed by oxygen plasma treatment to oxidize the Ge substrate. The Al_2O_3 layer then acts as a barrier layer of oxygen and effectively protects Ge surfaces from direct exposure of ECR oxygen plasma and any damages during the fabrication processes. In addition, low processing temperature provided by the ECR plasma oxidation is expected to minimize the thermal degradation of the GeO_x/Ge interface. They have improved this process to realize EOT less than 1 nm by employing this plasma postoxidation (PPO) process to HfO_2-based gate stacks [45].

A plasma postoxidation time of 10 s is sufficient to reduce D_{it} while maintaining the equivalent oxide thickness (EOT). The D_{it} of Au/Al_2O_3/GeO_x/Ge MOS capacitors is found to be significantly suppressed down to a value lower than 10^{11} $cm^{-2}eV^{-1}$. As shown in Figure 6, they can achieve the minimum D_{it} of 5×10^{10} $cm^{-2}eV^{-1}$ and 6×10^{10} $cm^{-2}eV^{-1}$ for pMOS (1.67 nm EOT) and nMOS (1.83 nm) capacitors, respectively.

High performance Ge MOSFETs with 0.98 nm (EOT) Al_2O_3/GeO_x/Ge gate stack have also been demonstrated by Zhang et al. [12]. The Ge n-MOSFETs have a record-high peak mobility of 937 cm^2/Vs as shown in Figure 7, and the Ge pMOSFETs with EOTs of 1.18, 1.06, and 0.98 nm have provided peak mobility values of 515, 466, and 401 cm^2/Vs, respectively. The Ge pMOSFET with an EOT of 0.98 nm has been found to provide around 1.8 times mobility enhancement against the previously reported values at this EOT value.

Figure 8 shows the mobility benchmark of Ge pMOSFETs in the ultrathin EOT range. From the comparison among the data record so far, a record-high peak mobility (596 cm^2/Vs) has been achieved in EOT of ~0.8 nm for HfO_2/Al_2O_3/GeO_x/Ge pMOSFETs, which is 5.1 times large as the previous value. This proves the novel gate stack structure and plasma postoxidation method can provide sufficient MOS interface passivation. In the same work, a high quality gate stack (HfO_2/Al_2O_3 (0.2 nm)/GeO_x/Ge) with a record 0.7 nm EOT was also successfully demonstrated. The D_{it} of this 0.7 nm gate stack is in the order of 10^{11} $cm^{-2}eV^{-1}$, which leads to a record 546 cm^2/Vs peak mobility.

So, we can conclude that, by applying the PPO method, one can realize both ultrathin EOT less than 1 nm and low D_{it} value at the same time. As a result, the ECR plasma postoxidation method is a promising solution for fabricating advanced high-k/GeO_x/Ge gate stacks with superior MOS interfaces and thin EOT.

2.3. Ozone Postoxidation. Ozone oxidation provides an alternative method to form a high quality GeO_2 IL. The minimum D_{it} of 3×10^{11} $cm^{-2}eV^{-1}$ was demonstrated by using ozone oxidation at 400°C [32]. In previous experimental investigation, Kuzum et al. demonstrated a ~1.5 times higher mobility than universal Si mobility, where a GeO_2 passivation layer was first formed by ozone oxidation and an Al_2O_3 dielectric was followed by ALD [50]. Considering the promising aspect of this ozone-based surface passivation, in the remainder of this review, the research of ozone postoxidation for Ge surface passivation will be discussed in more detail.

Aiming at realizing Ge surface passivation and thin EOTs at the same time, Sun et al. proposed a new ozone postoxidation (OPO) method for Al_2O_3/Ge MOS devices [46]. The OPO treatment performed on Al_2O_3/Ge gate stack is schematically shown in Figures 9 and 10 comparing the C-V characteristics of Al_2O_3/Ge MOS capacitors with different OPO times. It could be found that the sample without the OPO treatment process exhibits very poor C-V behaviors, and the C-V properties were significantly improved with the increase of the OPO time. The inset shows the EOT value of the capacitors decreases from ~2.39 nm to ~1.79 nm with the increasing time of OPO.

In order to investigate the impact of OPO treatment on the interface features of Al_2O_3/Ge gate stack, the high-resolution cross-sectional transmission electron microscopy (HR-TEM) images were taken and shown in Figure 11. It can be seen that the as-deposited sample is uniform and amorphous with a sharp interface. The physical thickness of the Al_2O_3 layer is deduced to be 3.6 nm. Furthermore, there was no GeO_2 interfacial layer (IL) growth between Al_2O_3

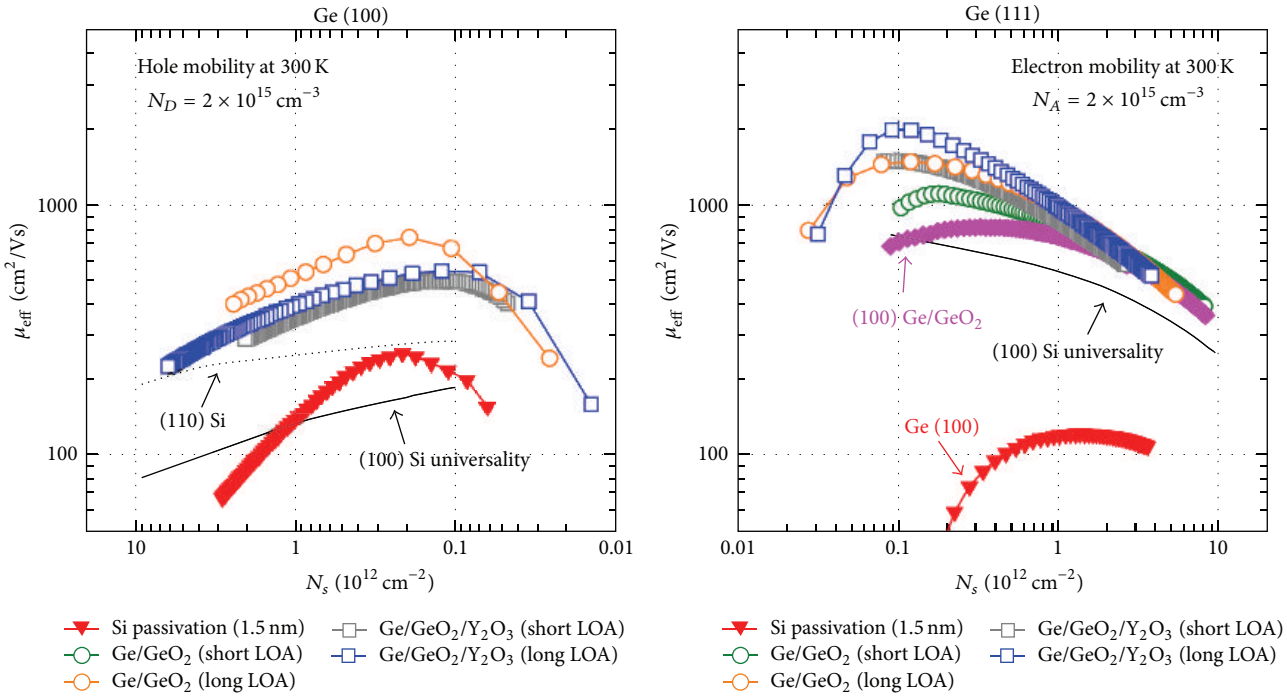

FIGURE 4: A hole mobility of 725 cm^2/Vs was achieved in Ge/GeO$_2$ gate stack with long LOA, which is 3.5 times higher than Si universal mobility. In case of electron mobility, Ge/GeO$_2$/Y$_2$O$_3$ gate stack shows the highest electron mobility of 1920 cm^2/Vs. Both are record-high values of Ge MOSFETs [11].

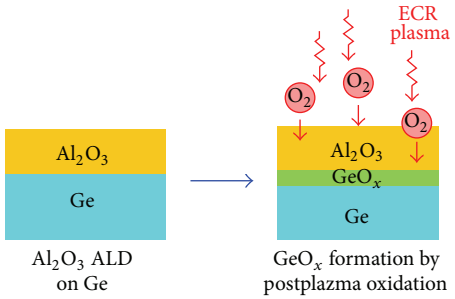

FIGURE 5: Al$_2$O$_3$/GeO$_x$/Ge gate stack formation process by using oxygen plasma through a thin ALD Al$_2$O$_3$ layer [40].

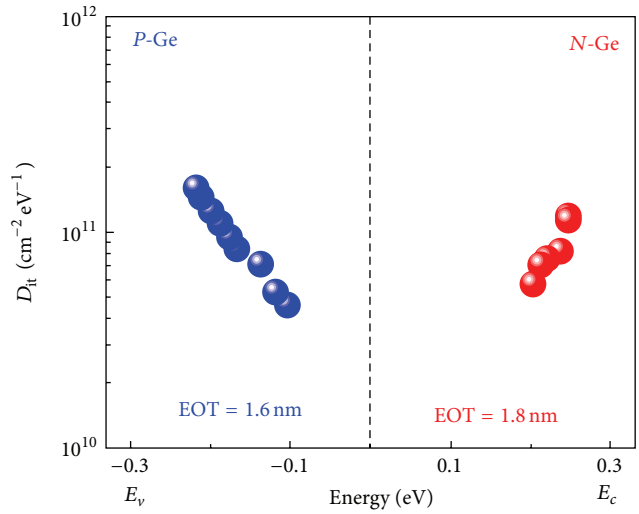

FIGURE 6: D_{it} distribution of the Au/Al$_2$O$_3$/GeO$_x$/Ge MOS capacitors versus energy [33].

films and Ge substrates even after the OPO treatment for 3 and 5 min.

To further understand the impact of the OPO treatment on Al$_2$O$_3$/Ge gate stack, the chemical components of Al$_2$O$_3$ films and the interfacial stoichiometry of all samples were examined by X-ray photoelectron spectroscopy (XPS) measurement. As shown in Figure 12, except the Ge^0 component, no germanium-related peak signals could be observed in the XPS spectrum of both as-deposited and OPO treated samples. This indicates that the Ge substrate was not oxidized after the OPO treatment even for 5 min or the amount of the GeO$_x$ at the interface is under the XPS's detection limit. It could also be found that the Al 2p spectrum of as-deposited sample exhibits two split peaks of Al–Al bonding at 73.0 eV and Al–O bonding at 74.1 eV, indicating the coexistence of the oxygen-deficient composition and the stoichiometric composition in the Al$_2$O$_3$ film. From the OPO treated samples' XPS spectra, we could find that the Al–Al bonding feature intensity rapidly decreases, while the Al–O bonding feature intensity continues to increase with the increase in the OPO time. It indicates that the OPO treatment could cure the oxygen deficiency in the Al$_2$O$_3$ film and finally enhance the average oxygen content of the film.

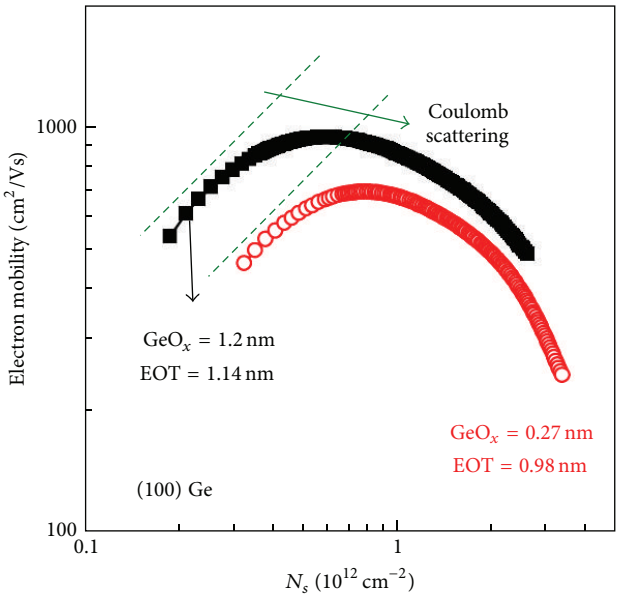

FIGURE 7: Mobilities of Ge n-MOSFETs with an Al_2O_3/GeO_x/Ge gate stack having different GeO_x IL thickness [12].

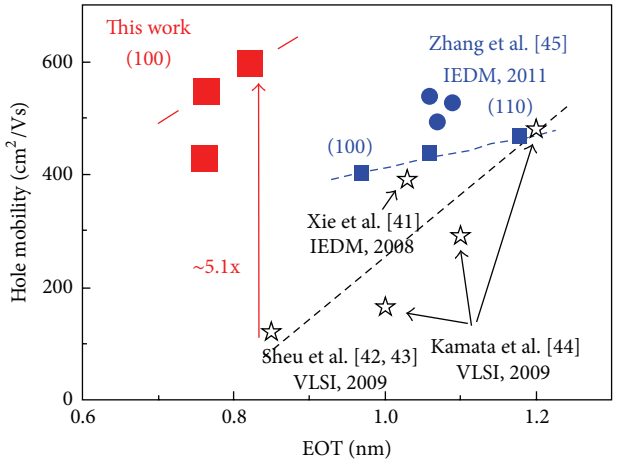

FIGURE 8: Peak mobility of Ge (100) pMOSFETs in Zhang et al.'s work versus EOT, compared with the results reported so far [41–45].

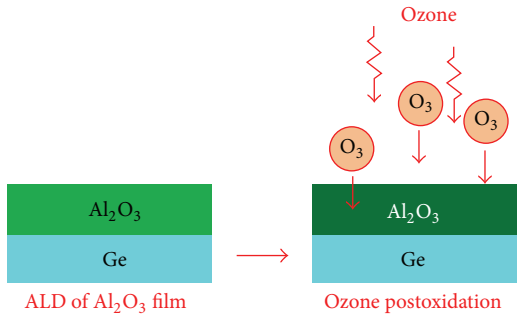

FIGURE 9: Process flow of the OPO treatment on Al_2O_3/Ge gate stack [46].

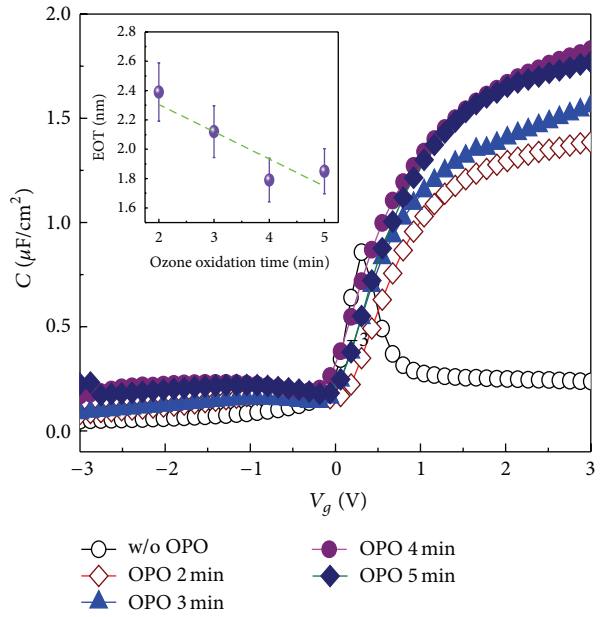

FIGURE 10: C-V characteristics (1 MHz) of Al_2O_3/Ge MOScap improved significantly with the OPO treatment. The inset shows the reduction of EOT versus the OPO treatment time [46].

The EOT value of the MOS capacitor, extracted from the C-V characterizations, decreases from ~2.39 nm to ~1.79 nm, which may be attributed to the continuous improvement in the permittivity of the ALD-Al_2O_3 film with the increase in the OPO time. After a careful process optimization with the OPO technology, sub-1 nm EOT and surface passivation could be achievable at the same time in Ge MOSFETs.

Just recently, Yang et al. have introduced the cycling ozone oxidation (COO) method into the ALD process to form a high quality Al_2O_3/GeO_x/Ge stack [47]. Figure 13 shows the process flow of COO method used in their work. This COO method is proved to be effective in repairing the defects like OH-related groups to suppress the gate leakage current. The minimum D_{it} value of 1.9×10^{11} cm^{-2}eV^{-1} is obtained by inserting GeO_x passivation layer with the COO treatment, as shown in Figure 14 [47].

3. Conclusion and Further Outlook

In order to realize high-mobility Ge CMOS device, different interface control and gate dielectric enhancement methods of Ge were systematically investigated. In this review, we have summarized and discussed various interface control technologies which are effective in obtaining high quality Ge MOSFETs. For reducing the interface state density and enhancing the mobility in Ge MOSFETs, the high-pressure oxidation, plasma postoxidation, and ozone postoxidation have been proven to be very effective based on the formation of good quality Ge oxide. For high-pressure oxidation and plasma postoxidation techniques, both of them can obtain a relatively low minimum value of D_{it} in the order of 10^{11} cm^{-2}eV^{-1} even at a thin EOT of subnanometer [12, 38].

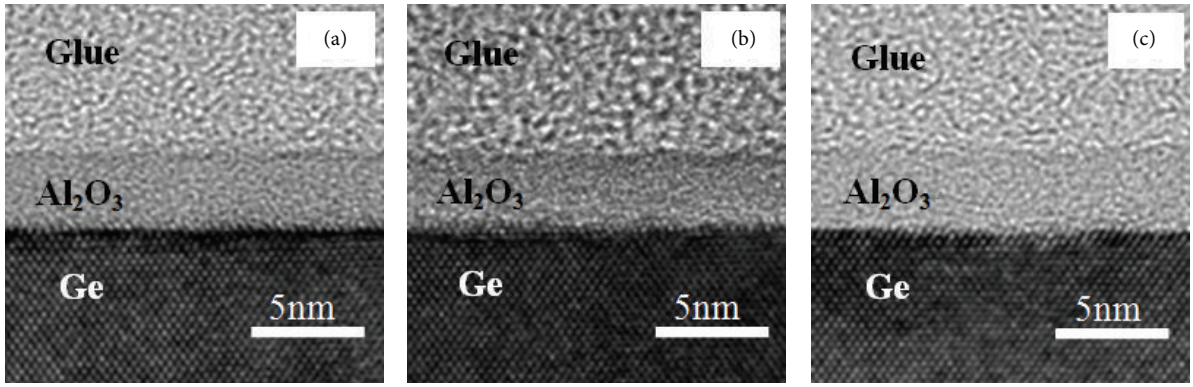

FIGURE 11: High-resolution cross-sectional transmission electron microscopy (HR-TEM) image of ALD-Al_2O_3 on Ge structure: (a) without OPO treatment; (b) OPO treatment for 3 min; and (c) OPO treatment for 5 min [46].

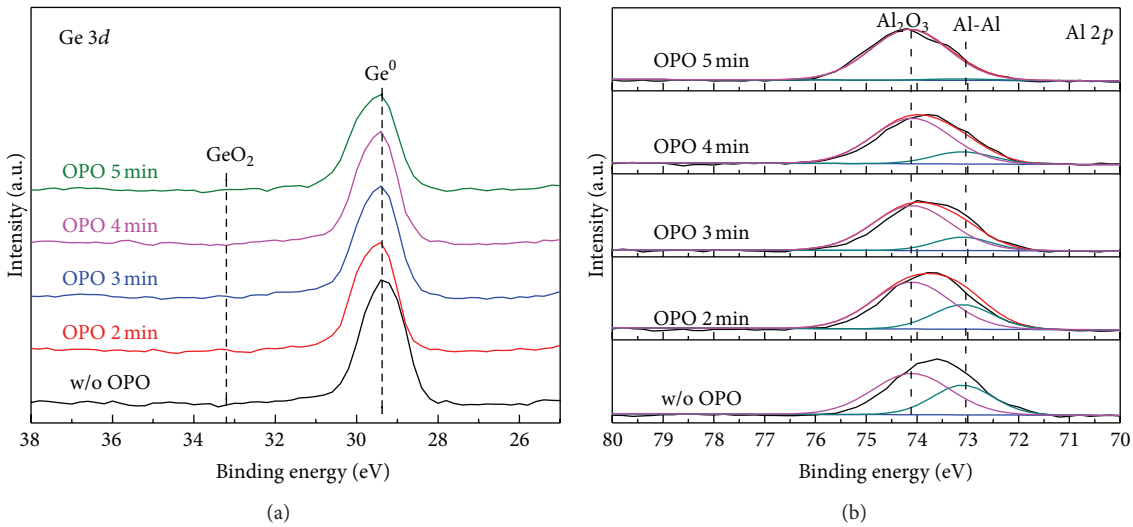

FIGURE 12: (a) Ge 3*d* and (b) Al 2*p* XPS spectra of Al_2O_3/Ge structure before and after an OPO treatment [46].

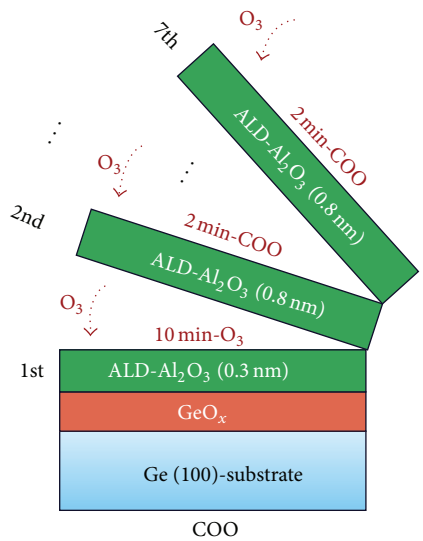

FIGURE 13: Schematic of fabrication procedure of Ge MOS gate stacks for samples with cycling ozone oxidation (COO) treatment [47].

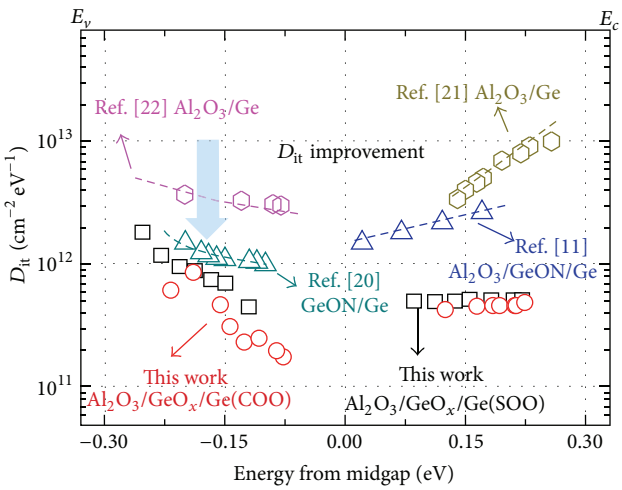

FIGURE 14: Energy distribution of D_{it} of Al_2O_3/GeO_x/Ge MOS capacitors with cycling ozone oxidation (COO) and single ozone oxidation (SOO) treatments, in comparison with previously reported data by other groups [47].

For ozone postoxidation technique, a relatively low minimum value of D_{it} of 1.9×10^{11} $cm^{-2}eV^{-1}$ was also obtained under a relatively thick EOT (definite data not given in their report) [47]. Thus, these three techniques are all potential methods to improve the interfacial properties of Ge/dielectric gate stack in Ge MOSFETs.

It is noted that there are still several challenges for this Ge MOS interface passivation technique. The high-pressure oxidation technique has to be performed under a high pressure of ~70 atm, and thus its applicability to integrate with the current Si CMOS technology is still not clear. On the other hand, the plasma postoxidation technique is well approved in planar Ge MOSFETs. However, its applicability in 3D channel device, especially the gate-all-around (GAA) device, is not investigated yet. For ozone postoxidation, it is still desired to examine the scalability of Ge gate stacks. Due to the drawbacks or limits of each technique, further optimization is still needed to improve the mobility and to scale down the EOT in Ge MOSFETs. The compatibility with existing integrated circuit technology platform is also an important issue.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

This work was supported by the National Program on Key Basic Research Project (973 Program) of China (Grant no. 2011CBA00607), National Natural Science Foundation of China (Grants nos. 61106089 and 61376097), and the Zhejiang Provincial Natural Science Foundation of China (Grant no. LR14F040001).

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