Hindawi
Advances in Condensed Matter Physics
Volume 2017, Article ID 7820676, 8 pages
https://doi.org/10.1155/2017/7820676

Research Article

Fast Switching 4*H*-SiC *P-i-n* Structures Fabricated by Low Temperature Diffusion of Al

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Received 12 January 2017; Revised 30 March 2017; Accepted 3 May 2017; Published 30 May 2017

Academic Editor: Jörg Fink

P-i-n 4*H*-SiC⟨Al⟩ diode structures are fabricated by a new approach which is low temperature diffusion of aluminium (Al) in SiC using flow of vacancy defects from surface into volume of crystal. In conventional diffusion in SiC, the operating temperature is usually >2050°C while, in this approach, the diffusion temperature is between 1150 and 1300°C. As the conditions of formation of junction in this method essentially differ from conventional diffusion (low temperature and process of diffusion are accompanied by forming structure defects), it is interesting to identify the advantages and disadvantages of a new method of diffusion. Fabricated *p-i-n* structures have low breakdown voltage between 80 and 140 V (due to the influence of dislocations and micropipes) and are capable of operating at temperatures up to 300°C. Structure has fast switching time and duration of the reverse recovery current less than 10 ns. We believe that because of low diffusion temperature, the concentration of nitrogen related trapping levels is relatively low and as a result the fast switching time is observed in our samples. It has been shown that this low temperature diffusion technology can be used to fabricate *p*-region and high resistive *i*-region of SiC diode in single-step process.

1. Introduction

Silicon carbide (SiC) has some unique properties which improve the performance of the SiC based devices and provide a number of advantages over devices made of traditional semiconductor materials such as silicon and gallium arsenide. One of these advantages is the high thermal stability of SiC made devices [1, 2] which makes it suitable for power and extreme electronics [3].

An important characteristic of SiC diodes for power and pulse techniques is the switching time (τ) of diodes which is usually >20 ns for a diode with an area of $100 \times 100\ \mu m^2$ [4]. This switching time is probably related to a trapping level in SiC material. It has been found that the base region of SiC diodes doped with aluminium has a deep trapping level with an ionization energy ~1.45 eV and trapping level ~0.16 eV which is due to nitrogen impurity [2]. Capture processes and thermal activation of electrons associated with these levels can greatly increase the duration of the relaxation of current through the *p-n* junction.

Currently, power diodes made of silicon carbide using diffusion technology have a breakdown voltage ~700 V for 4*H* polytype [5] and ~1000 V for 6*H* polytype [6]. The most important steps in manufacturing silicon carbide based devices are the formation of *p-n*-junctions and fabrication of low-resistance ohmic contacts.

Previously it has been shown that to fabricate diodes with high breakdown voltage, highly resistive *i*-region of *p-i-n* SiC diodes needs to be created by epitaxial growth of thin SiC layer (free from micropipe defects) [7, 8]. Afterwards (second technological step), *p*-region of *p-i-n* SiC diodes is formed by thermal diffusion at a temperature >2050°C or ion implantation of SiC by aluminium [4, 9]. It is worth mentioning that heavily doped SiC crystal fabricated by ion implantation (with concentration of impurities up to $10^{19}\ cm^{-3}$) should be annealed at a temperature ~1800°C to remove the defects [10, 11]. Extremely high temperature processing (>2050°C) needed during thermal diffusion [12–14] or after ion implantation [10, 11] may increase the production cost.

Thus epitaxy and ion implantation have gained popularity to fabricate concurrent SiC based devices. And conventional thermal diffusion of impurity is regarded as old and unstable technology for fabrication of *p-n* junction on the base of SiC.

In this article we report on properties of *p-i-n* structures fabricated by low temperature diffusion of aluminium (Al) in SiC using flow of defects (silicon and carbon vacancies) from surface into volume of crystal. In conventional diffusion in SiC, operating temperature is usually >2050°C while in our developed method the diffusion temperature is between 1150 and 1300°C. As the conditions of formation of junction in this method essentially differ from conventional diffusion (low temperature and process of diffusion are accompanied by formation of structure defects) it is interesting to identify the advantages and disadvantages of a new method of diffusion.

2. Materials and Methods

P-i-n diodes are fabricated on the basis of single crystal samples of silicon carbide 4*H*-*n*-SiC grown by the Physical Vapour Transport (PVT) method (Cree Research, Inc, USA) with a relatively low concentration of growth defects: N_d dislocations 10^4 cm^{-2} and N_m micropipes ~10–10^2 cm^{-2}, thickness ~300–600 μm, surface ~0.25 cm^2 and specific resistance ~3.6–20 Ω·cm, and nitrogen impurity concentration ~$(0.5–1.0) \times 10^{17}$ cm^{-3}.

Etching of samples is performed in KOH–water solution upon stimulation by ultraviolet (UV) light. Unlike reactive ion etching the UV light stimulated etching does not create defects and allows fabricating a smooth surface [16, 17].

After the removal of the surface layer, the low temperature diffusion of aluminium is carried out. This diffusion in 4*H*-SiC is performed at different temperatures ranging between 1150 and 1300°C during 30 min by our new method patented in USA and Uzbekistan and described in detail [17–26]. Below some information about new method of diffusion is given briefly. Well known diffusions of impurities in SiC are carried out via Si- and C-vacancies and the solubility of impurity and diffusion coefficient in SiC are different in Si and C - sublattice [13]. In our method the diffusion process is carried out in air atmosphere in condition of surface oxidation to create a flow of vacancies of Si and C from the crystal surface into the bulk of the sample [17]. Increasing vacancy concentration increases the diffusion constant and solubility of impurity up to 10^{20} cm^{-3} [20–22]. Temperature of diffusion in this method is between 1150 and 1300°C which is lower compared to the conventional diffusion process (more 2000°C). Thus low disintegration of SiC surface is expected.

The source of impurity of aluminium atoms for diffusion is formed by two ways: (1) thin pure aluminium film is thermally evaporated onto the sample in Vacuum Universal Post VUP-4 (10^{-6} Torr.). (2) The aluminium chloride thin film is created on the surface of sample using the saturated solution of aluminium chloride in methanol. The sample is then heated in the air up to 650°C for 30 min, which leads to the formation of an Al and Si oxides glass layer on the surface. Afterwards the sample is annealed in the air during 30 min in the diffusion furnace at a temperature ranging between 1150°C and 1300°C. In these conditions of surface oxidation from the surface of SiC the SiO and CO molecules are evaporated and flow of vacancies is created from the surface into volume of crystal. After the sample is cooled to room temperature, it is immersed in buffered oxide etch to remove the top oxide layer [18–20].

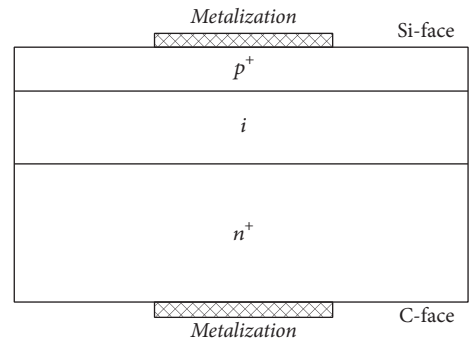

Figure 1: Schematic diode structures of *p-i-n* 4*H*-SiC⟨Al⟩ diode.

As a first assumption it is presumed that the diffusion of aluminium goes via carbon and silicon vacancies like conventional mechanism diffusion in SiC and differs only by increased concentration of vacancies. Of course, the real mechanism of aluminium diffusion in our case can differ from conventional mechanism of diffusion via C- and Si-vacancies. It is clear that increased concentration of vacancies near the surface of the crystal leads to SiC lattice distortion. Other factors can also influence the diffusion process; for example, the formation of nanopores or new defects can influence the diffusion of aluminium. But in this presented article the diffusion mechanisms are not investigated as for this study additional experiments and thorough analysis are required. Our approach is based on an obvious fact that the increased concentration of silicon and carbon vacancies leads to low temperature diffusion.

Further study shows that during diffusion process vacancies of Si and C penetrate into volume deeper than doping impurity and lead to the formation of *i*-region simultaneously with the formation of *p*-region. So in one processing step both the *p*- and *i*-regions can be formed. The *i*-region is created (compensated) by deep level defects related to Si- and C-vacancies.

Type of conductivity of doped layers and silicon carbide single crystals was tested by hot probe (thermoprobe) method [27]. Impurity concentration was measured using standard capacitance-voltage (*C-V*) measurements [28]. Impedance measurements were carried out at different frequencies with the amplitude of the alternating current (AC) signal kept constant at 20 mV, while the researched structure was under applied direct current (DC) bias. Switching time of 4*H*-SiC⟨Al⟩ diode structures was measured on a special pulse stand [29].

3. Results

Schematic structure of the fabricated SiC diode and its current-voltage (*I-V*) characteristics of *p-n* 4*H*-SiC⟨Al⟩ junction (area of *p-n*-junction ~ 6 mm^2) are shown in Figures 1 and 2, respectively. Figure 2 shows that the diode has a breakdown voltage between 80 and 140 V which is significantly low

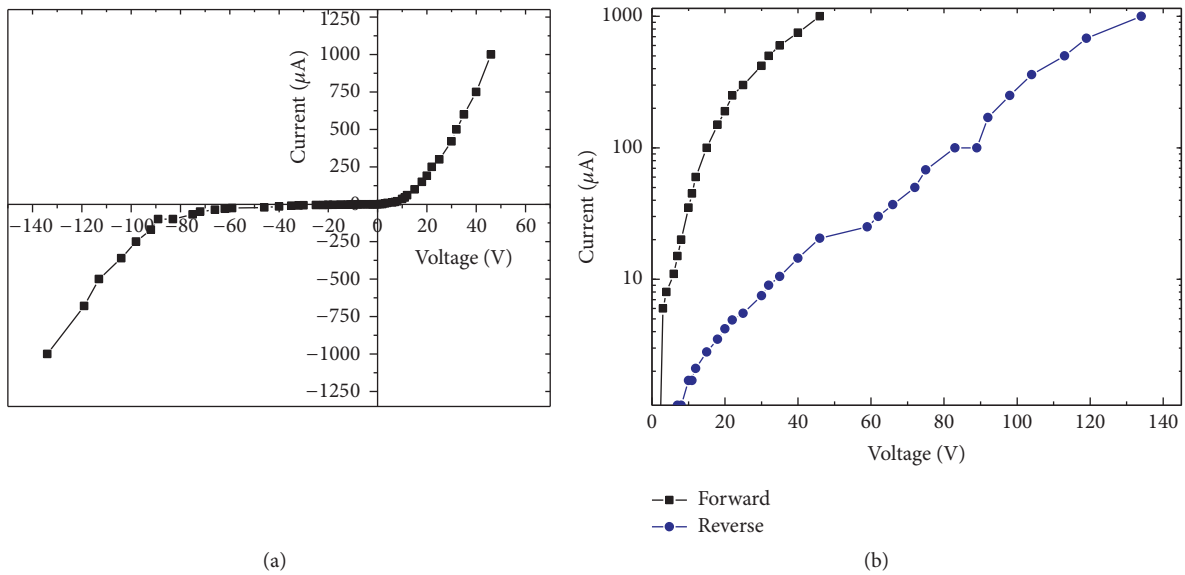

FIGURE 2: I-V characteristic of p-i-n 4H-SiC⟨Al⟩ junction, in the (a) linear and (b) semilog scale.

compared to the results reported elsewhere (>600 V, 1.2 kV, and 1.7 kV) [30, 31]. It is well known that the breakdown voltage in SiC structures is greatly reduced in the presence of such defects like micropipes, screw dislocations, stacking faults, and so on. The largest breakdown voltages are achieved in SiC/SiC structures with epitaxial layers without micropipes and with a low concentration of dislocations [7, 8].

In our structures low value of breakdown voltage is mainly due to the influence of dislocations ($N_d \sim 10^4$ cm^{-2}) and micropipes ($N_m \sim 10$–10^2 cm^{-2}) in used SiC crystals. It has been reported previously [32] that with a screw dislocation concentration of ~10^4 cm^{-2} the maximum breakdown voltage (V_b) of samples with diameter 300–500 μm between 350 and 400 V can be reached. For our samples with area 4000 × 4000 μm the breakdown voltage was ~140–160 V.

This breakdown voltage can be improved in several ways, for example, by improving low temperature diffusion technology, by the formation of mesa-structure, and by surface passivation. But to get a significantly high breakdown voltage up to 1-2 kV like Cree Inc. [33], it is necessary to use SiC crystal free from micropipes and with lower concentration of dislocations.

An increasing of direct current is observed at voltages higher than 10 V, which indicates the presence of a high-resistance layer between the p-region and n-region. This is also confirmed by C-V measurements at 1 MHz. For the applied reverse voltage, capacitance is ~2.2 pF (Figure 3) and the series resistance is ~70 kΩ.

Thickness of p-i-n junction (W) is found to be $W(V = 0) \sim 12$ μm using [28]

$$C = \frac{\varepsilon\varepsilon_0 S}{W}, \quad (1)$$

where C is capacitance of the diode, ε is dielectric constant of the silicon carbide, ε_0 is electric constant, S is layer area, and W is thickness of the depletion layer.

Figure 4 shows the distribution of impurities in the i-layer, determined from dependence of the $C(V)$ characteristics. This figure shows that the depletion region spreads from 12.2 μm at $V_r = 0$ up to 13.7 μm for $V_r = 40$ V. So the thickness of i-region is about 1.5–2 μm.

The high-resistance region is caused by defects, which is probably introduced during the diffusion and it has inhomogeneous distribution of the carrier density. According to Figure 4 the carrier concentration at the interface of the junction and a high-resistance n-layer increase from 10^{13} to 5 × 10^{16} cm^{-3} (impurity concentration in the substrate of silicon carbide).

To further study the fabricated diode, impedance measurements at relatively low frequencies 5000, 10000, 15000, and 20000 Hz (see Figure 5) were carried out to evaluate the capacitance, series resistance, and other parameters of structure.

Assuming the parameters of the structures do not change in this frequency range, on the base of the equivalent circuit it is possible to evaluate the capacitance and the series resistance of structure. Figure 6 shows the equivalent circuit of our structure which is created based on the equivalent circuit of p-i-n diode reported in [15]. According to the work done in [15], L_s inductance has to be added in equivalent circuit. But in our case, L_s can be neglected as this small parasitic element has little effect on p-i-n diode performance below 1 MHz.

According to [15] the simplified equivalent circuit of p-i-n junction at direct applied bias consists of diffusion capacity (which is parallel to barrier capacitance) and series resistance (Figure 7(a)). And simplified equivalent circuit for the p-i-n junction for reverse applied bias consists of barrier capacitance and parallel and series resistances (Figure 7(b)) [15].

If we assume that at constant applied voltage, resistance and capacitance of the junctions do not change or slightly change with frequency, the module of impedance of the above equivalent circuits can be considered.

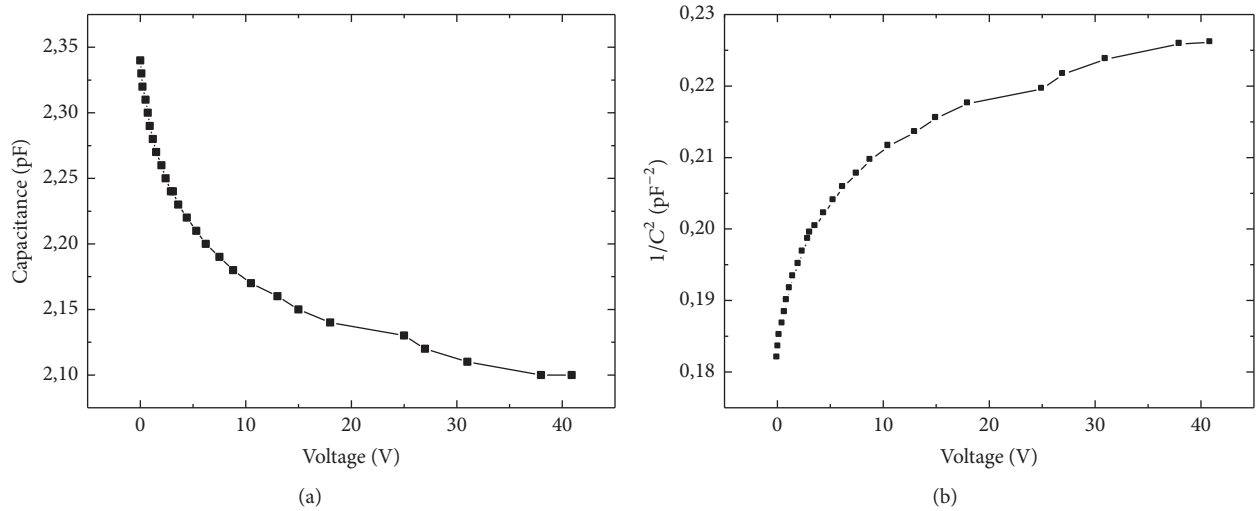

Figure 3: The dependence of capacitance (a) and the value $1/C^2$ (b) for one of the diodes under reverse voltages measured at 1 MHz.

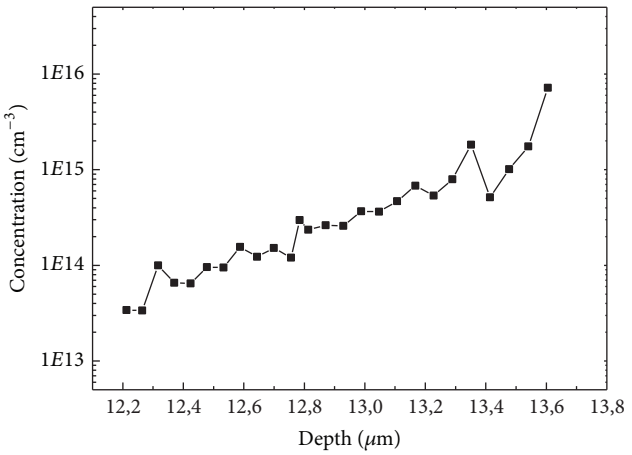

Figure 4: The distribution of aluminium concentration versus $W(V)$ according to C-V data in high-resistance layer of the sample 4H-SiC⟨Al⟩.

For direct bias C_{dif} and C_b are parallel ($C = C_{\text{dif}} + C_b$) and with serial resistance R_S have the total impedance

$$Z = R_S + \frac{1}{j\omega C}, \tag{2}$$

where $j\omega C$ is capacitance conductivity ($j = \sqrt{-1}$ means that capacitance changes the phase of AC) and $w = 2\pi\nu$ is angular frequency. Module of total impedance for direct bias is

$$Z = \left(R_S^2 + \frac{1}{(\omega C)^2}\right)^{1/2}. \tag{3}$$

Let us consider case of reverse bias.

The conductivity of parallel connected C_{rev} and R is

$$\Sigma = j\omega C + \frac{1}{R} = \frac{1 + j\omega CR}{R} \tag{4}$$

and total impedance for reverse bias is

$$Z = \frac{R}{1 + j\omega CR} + R_S. \tag{5}$$

Let us transform this expression to the canonical form (using multiplication on conjugate expression)

$$\begin{aligned} Z &= \frac{R\left(1 - j\omega CR\right)}{\left(1 + j\omega CR\right)\left(1 - j\omega CR\right)} + R_S, \\ Z &= \left(R_S + \frac{R}{\left(1 + w^2C^2R^2\right)}\right) - \frac{j\omega CR}{\left(1 + w^2C^2R^2\right)}. \end{aligned} \tag{6}$$

Module of this impedance is

$$\begin{aligned} Z = \Bigg[&\left(R_S + \frac{R}{\left(1 + (\omega CR)^2\right)}\right)^2 \\ &+ \left(\frac{\omega CR^2}{\left(1 + (\omega CR)^2\right)}\right)^2\Bigg]^{1/2}. \end{aligned} \tag{7}$$

The computer fitting of expression (3) (Figure 7(a)) and (7) (Figure 7(b)) to experimental data was performed using Origin 60 which is shown in Figure 8.

At direct connection, the forward capacitance increases from 34 pF at 6 V to 276 pF at 12 V and series resistance decreases from 260 kΩ at 6 V to 80 kΩ at 12 V.

Lifetime of the minority carriers is found to be ~7 ns using

$$C_D = \frac{\tau_p J}{kT/q}, \tag{8}$$

where τ_p is the minority carrier lifetime, J is a forward current through the diode, k is Boltzmann constant, T is the temperature, and q is electron charge.

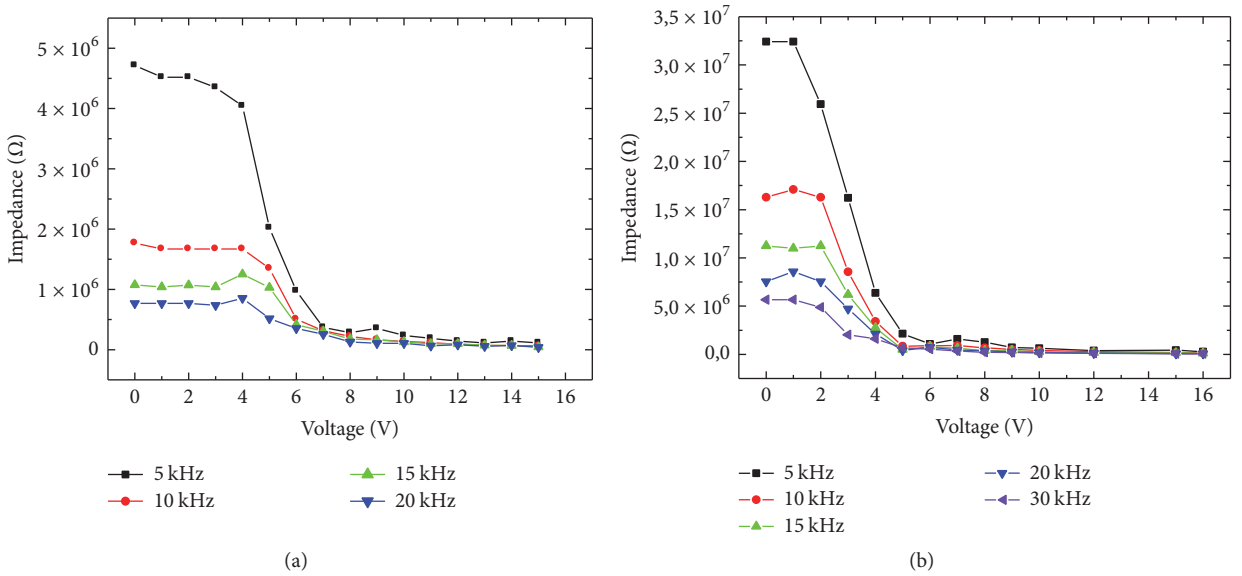

FIGURE 5: Impedance of the diode structure at different frequencies at direct (a) and reverse (b) bias (●: 5 kHz, ▲: 10 kHz, ▼: 15 kHz, ■: 20 kHz, ◄: 30 kHz).

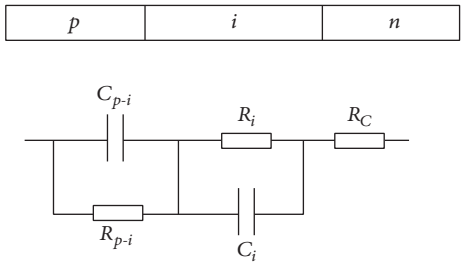

FIGURE 6: Equivalent circuit diagram of *p-n* junction with the intermediate layer of high resistance, constructed on the basis of an equivalent circuit of *p-i-n* diode [15].

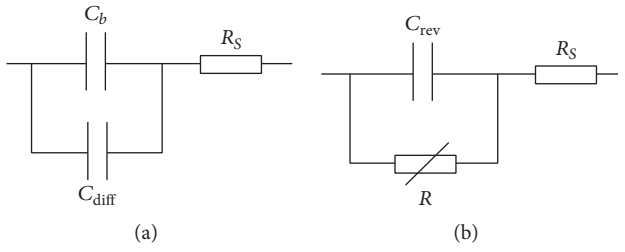

FIGURE 7: Simplified equivalent circuit of *p-i-n* junction for direct connection (a) and reverse connection (b).

Forward biased *p-i-n* diode is a Current Controlled Resistor [29] and relationship between R_S and I_f can be described using

$$R_S = \frac{W^2}{I_f \tau \left(\mu_n + \mu_p\right)}, \tag{9}$$

where I_f is forward bias current, τ is minority carrier lifetime, and μ_n, μ_p are electron and hole mobility, respectively.

For perfect SiC single crystal, $(\mu_n + \mu_p) \sim 1000\ \text{cm}^2/(\text{V}\cdot\text{s})$ [34]. If *i*-region has a thickness ~ 2 μm, minority carrier lifetime will be ~0.1 ns from (9). For SiC material with micropipes and dislocations and concentration of electrons $\sim 10^{17}\ \text{cm}^{-3}$ the sum $(\mu_n + \mu_p)$ is ~400–500 $\text{cm}^2/(\text{V}\cdot\text{s})$ [35]. Thus in *i*-region the minority carrier lifetime is ~0.20–0.3 ns.

It is necessary to mention here that the (1) and (3) will not remain exactly the same as it is now because under various applied voltages, fitting parameter R_S will change (because it includes the series resistance of contacts and resistance of *i*-region which is often nonlinear in SiC devices). It should be also noted that at least 20 data points need to be used for fitting. For our study, measurements are performed in four frequencies only, which is why the values we have obtained are just estimations.

The current waveform of 4*H*-SiC⟨Al⟩ diodes was measured at room temperatures and shown in Figure 9. The switching of diodes from forward current (I = 0.25 mA) to reverse voltage 60 V is measured. As seen from Figure 9, the diodes have very fast switching time and duration of the reverse recovery current (of the order of 5–7 ns) for junctions with an area of approximately 6 mm^2. Obtained experimental data do not contradict above stated estimations of minority carrier lifetime.

Literature suggests switching time (τ) > 20 ns can be obtained for a diode with an area of 100 μm × 100 μm in laboratory [4]. In the catalogue of Toshiba, reverse recovery time for SiC Schottky commercial diodes is ~40 ns [36]. The reverse recovery characteristics of a 4*H*-SiC *p-i-n* diode under higher voltage and faster switching are investigated elsewhere [37] where it is shown that at a room temperature τ is ~80 ns.

Now we will further investigate the origin of fast switching time. If we assume that junction process is determined only by electrical capacitance of the junction (capacitive

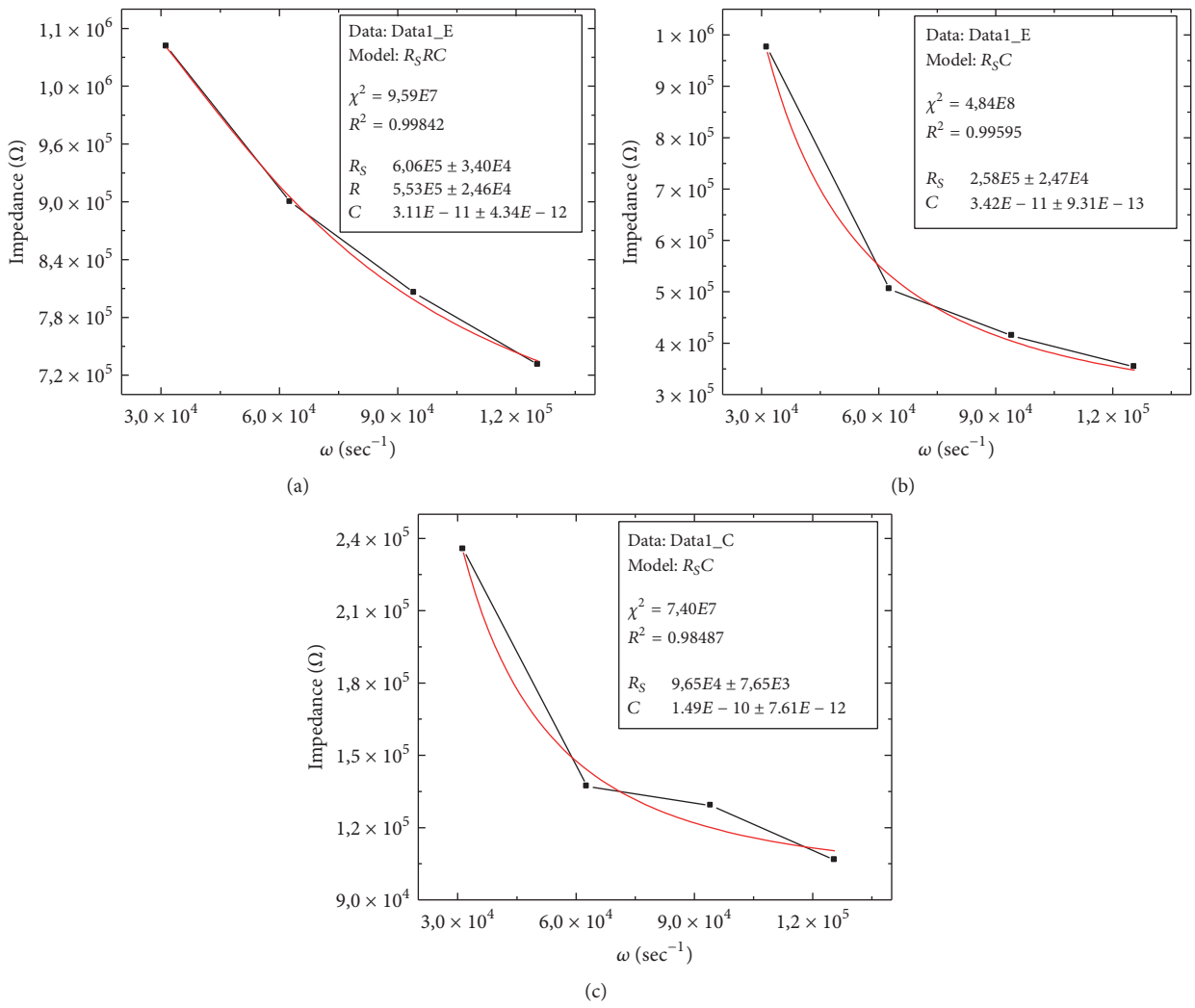

FIGURE 8: Results of fitting of expressions (2, 3) to experimental data: (a) reverse applied voltage 6 V; (b) direct applied voltage 6 V; (c) direct applied voltage 10 V.

processes) and resistivity the relaxation time $t_r = RC$ (R is series resistance and C is capacity of the junction) then the relaxation time should be ~10^{-10} s. However, as it is shown earlier [2], junction processes involve nonequilibrium carriers in silicon carbide determined by trapping level (EK_2 with energy $E_c \sim 0.16$ eV). This trap level is ascribed to the donor impurity of nitrogen and the observed concentration profile in silicon carbide diode associated with the diffusion of nitrogen as background impurities [2]. The diffusion temperature in our technology is 1150–1300°C, significantly lower than the conventional diffusion temperature which is ~2000–2200°C. Because of this low diffusion temperature, the concentration of trapping levels due to nitrogen is relatively low and as a result the fast switching time is observed in our samples.

Measurement of the I-V characteristics at different temperatures has also been performed. In reverse branch of the I-V characteristic, we have not seen any sharp electrical breakdown and reverse current of 100 mA was considered to be the beginning of electrical breakdown. With increasing temperature up to 300°C the breakdown voltage has decreased down to 15 V. Thus the fabricated SiC diodes keep their rectifying properties up to 300°C.

The fabricated SiC diodes with relatively low breakdown voltage of ~150 V and fast switching time less 10 ns have the prospect of being used in application devices like mobile phones, DSC, lighting, Notebook PCs, HDD, PPC, power supplies for communication devices, and so on [38, 39].

4. Conclusions

P-i-n 4*H* SiC⟨Al⟩ diodes are fabricated by low temperature diffusion of Al in SiC by using flow of Si, C-vacancies from surface into volume of crystal. In this method the diffusion temperature is about 1150–1300°C, lower than conventional diffusion temperature (>2050°C). Fabricated *p-i-n* structure have low breakdown voltage between 80 and 140 V (due to the influence of dislocations and micropipes) and are capable

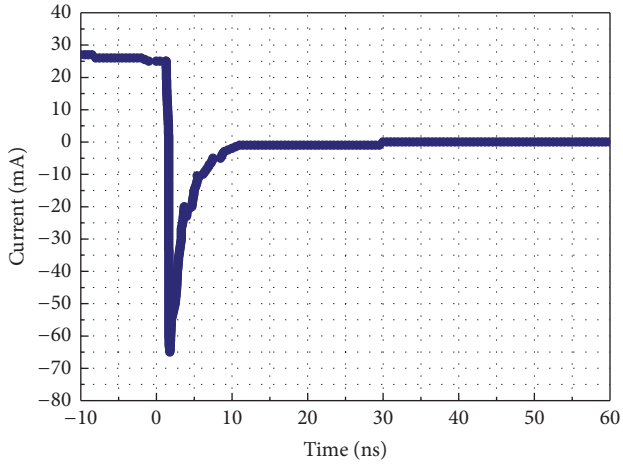

FIGURE 9: Oscillogram of the current of 4*H*-SiC⟨Al⟩ diode measured at switching from the forward current (I = 25 mA) to a reverse voltage of 60 V.

of operating at temperatures up to 300°C. Structure has fast switching time and duration of the reverse recovery current less than 10 ns. It has been shown that this low temperature diffusion technology can be used to fabricate *p*-region and high resistive *i*-region of SiC diode in single-step process.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

The authors would like to thank Farsad Imtiaz Chowdhury and Ulug'bek Abdurakhmanov for assisting during the proofreading of the manuscript.

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