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Research Article

DC Performance Variations of SOI FinFETs with Different Silicide Thickness

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DC performance and the variability of n-type silicon-on-insulator dopant-segregated FinFETs with different silicide thickness (T_{sili}) are analyzed. DC parameters including threshold voltage, low-field-mobility-related coefficient, and parasitic resistance are extracted from Y-function method for the comparison of DC performance and variability, and the correlation analysis. All the devices show similar subthreshold characteristics, but the devices with thicker T_{sili} have greater threshold voltages. The devices with thicker T_{sili} suffer from the DC performance degradation and its greater variations because the Schottky barrier height at the NiSi/Si interface increases and fluctuates greatly. This effect is validated by greater threshold voltages, larger parasitic resistances, and high correlations among all the DC parameters for the thicker T_{sili}. The devices with thicker T_{sili} also have higher low-frequency noise because of larger parasitic resistances and their correlated mobility degradations. Therefore, the device with relatively thin T_{sili} is expected to have better DC performance and variability concerns.

1. Introduction

Silicon-on-insulator (SOI) MOSFETs maintain short channel immunity successfully due to the absence of substrate leakage current [1]. SOI-based devices having fin-shaped [2], ultra-thin-body [3], or gate-all-around [4] channel regions attain great scalability without short channel degradation. Meanwhile, dopant-segregated SOI MOSFETs have been considered as one of the promising candidates due to their several advantages over the planar bulk MOSFETs: low Schottky barrier height (SBH) at the silicide/semiconductor interface, possibility of low-temperature process, and near-abrupt junction formation [5–9]. Not only MOSFETs but also tunneling FETs also utilize abrupt doping profile to enhance the band-to-band tunneling transport at the source/channel junction [10, 11].

Two-step annealing process during silicidation was suggested to decrease the lateral excursion of silicide into the channel region [12]. The influence of NiPt thickness prior to silicidation on the DC performance of SOI MOSFETs has been studied [13]. Increasing the NiPt thickness increased the contact resistance due to the decreased interfacial area between silicide and semiconductor but decreased the variations of sheet resistance due to its full silicidation. In this regard, it is necessary to analyze both DC performance and its variability in the perspective of the silicidation for the nanoscale dopant-segregated SOI MOSFETs.

Thus, DC performance and variations of SOI FinFETs with different silicide thickness (T_{sili}) were investigated. Then, the variability sources inducing the drain current (I_{ds}) variations were studied using the correlation analysis. Low-frequency noise was also measured for the detailed analysis of the devices with different T_{sili}.

2. Materials and Methods

(100) undoped SOI with 140-nm-thick buried oxide (BOX) and 20-nm-thick top Si region was prepared. BOX overetching process was performed to define omega-shaped fin structure as shown in Figure 1(b) of [13]. After the formation of gate stack (HfO_2, TiN, amorphous-Si), Arsenic dopants were implanted at extension regions to reduce the underlap resistance. After defining nitride spacer regions with the spacer length (L_{sp}) of 20 nm, low-energy implantation and annealing at 1070°C and 1.5 s were done for the source/drain (S/D) regions. Different from [13] where the NiPt with

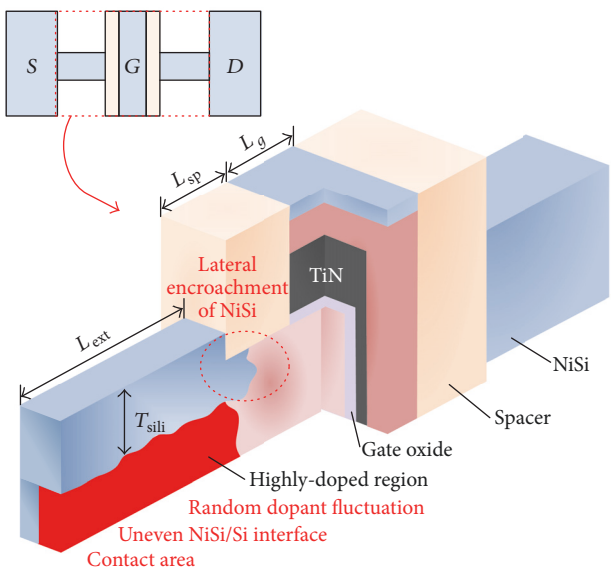

Figure 1: 3D schematic diagram of the SOI FinFETs. Geometrical parameters such as gate length (L_g), spacer length (L_{sp}), extension length (L_{ext}), and silicide thickness (T_{sili}) are also specified. Top left figure describes the real device structure, and red-colored phrases indicate the possible variability sources.

different thickness of 5 or 10 nm was deposited, the same 10-nm-thick NiPt (4% Pt) was deposited and annealed under two-step rapid thermal process (RTP) conditions to remove the unreacted NiPt in the middle. Instead, different RTP temperature and time conditions were used to form the NiSi with different T_{sili} of 8 and 10 nm. Otherwise, all the measured devices have the equivalent number of fins (N_{fin}) of 2, fin width (W_{fin}) of 40 nm, fin height (H_{fin}) of 20 nm, extension length (L_{ext}) of 80 nm, and gate length (L_g) of 40 nm. The detailed process flow and device geometry are shown in [13].

All the devices have the active regions with equivalent size and structure, so the differences of DC performances and the variations are induced mostly by different T_{sili}. Figure 1 shows the possible variability sources of the S/D regions. Uneven NiSi/Si interface [14] and random dopant fluctuation (RDF) [15, 16] can also fluctuate the contact resistivity and thus induce the DC performance variations. Different NiSi/Si contact area by different T_{sili} would also affect the DC performance and variations because typical transfer lengths, defined as the distances that carriers below the contact travel before entering into the contact, of SOI devices are in the order of 100 nm [17, 18], which is longer than L_{ext}. Different RTP conditions involved with different T_{sili} can vary the device performance by statistical piping effect [19] or lateral encroachment of NiSi into the S/D extension regions [20]. To understand DC performance and its variations for different T_{sili}, their transfer characteristics were measured using Keithley 4200 semiconductor characterization system, whereas low-frequency noise was measured using HP 89410A vector signal analyzer.

3. Results and Discussion

3.1. DC Performance and Variations at Different Silicide Thickness. I_{ds} and transconductance (g_m) of the 50 measured devices each with different T_{sili} of 8 and 10 nm are shown in Figure 2. Each wafer has a different T_{sili}, and the measured devices with each T_{sili} are at the same position of each wafer to minimize the die-to-die variations between two different T_{sili}. Gate voltage (V_{gs}) is swept from 0.0 to 1.3 V in steps of 0.02 V, and drain voltages (V_{ds}) are 0.05 and 1.0 V. Red lines indicate the averages of I_{ds} and g_m for each T_{sili}. In both linear and saturation regimes, the devices with T_{sili} of 8 nm have greater DC performance by showing higher on-state currents (I_{on}), while the subthreshold characteristics for T_{sili} of 8 and 10 nm are similar. Figure 2(c) shows that all the devices with T_{sili} of 8 and 10 nm do not have ambipolar effects at high V_{ds} of 1.0 V near the off-state, validating the absence of Schottky contact [13].

R_{on} ($= V_{ds}/I_{on}$) values of the 20 measured devices each with different W_{fin} and T_{sili} are shown in Figure S1. I_{on} are extracted at the gate overdrive voltage ($V_{gs} - V_{th\_CCM}$) of 1.0 V, where V_{th_CCM} is the threshold voltage (V_{th}) extracted from constant current method (CCM) at $I_{th} = W_{eff}/L_g \cdot 10^{-7}$ A ($W_{eff} = N_{fin} \cdot (2H_{fin} + W_{fin})$). The devices with T_{sili} of 8 nm have smaller R_{on} for all W_{fin}. But the difference of R_{on} between two different T_{sili} is smaller for greater W_{fin} because the ratio of the NiSi/Si contact area between two different T_{sili} decreases. Additionally, raised S/D structure would be beneficial to improve the DC performance by increasing the NiSi/Si contact area. But for raised S/D structure, likewise, thicker T_{sili} also decreases the contact area, increases the contact resistance, and thus degrades the DC performance [21].

Several parameters from the transfer characteristics are extracted to analyze the DC performance variations: V_{th}, low-field-mobility-related coefficient (X_0), and parasitic resistance (R_{sd}). V_{th} values are extracted using CCM or Y-function method [16, 22]. V_{th_CCM} is measured at $I_{th} = W_{eff}/L_g \cdot 10^{-8}$ A, whereas V_{th} from Y-function method (V_{th_y}) is extracted from the x-axis intercept of the linearly extrapolated curve as shown in Figure 3.

The simple and general expression of I_{ds} at low V_{ds} in the strong inversion regime is given by

$$I_{ds} = X_0 \cdot \left(V_{gs} - V_{th\_y}\right) \cdot \left(V_{ds} - I_{ds} R_{sd}\right), \quad (1)$$

where X_0 is defined as $\mu_{eff} \cdot C_{ox} \cdot W_{eff}/L_g$ (μ_{eff} is effective mobility and C_{ox} is oxide capacitance). Y-function is simply expressed as

$$Y \equiv \frac{I_{ds}}{\sqrt{g_m}} = \sqrt{X_0 \cdot \left(V_{ds} - I_{ds} R_{sd}\right)} \cdot \left(V_{gs} - V_{th\_y}\right). \quad (2)$$

According to (2), Y-function is linear in the strong inversion regime if X_0 or μ_{eff} does not depend on V_{gs}. In other words, the Y-function does not satisfy the linearity condition if the devices suffer from surface roughness scattering greatly [22]. Another assumption is that $I_{ds} \cdot R_{sd}$ is almost invariant to V_{gs} and smaller than V_{ds} in the strong inversion regime, which is satisfied in this study. Almost all the measured devices also meet the linearity condition at V_{ds} of 0.05 V (Figure 3)

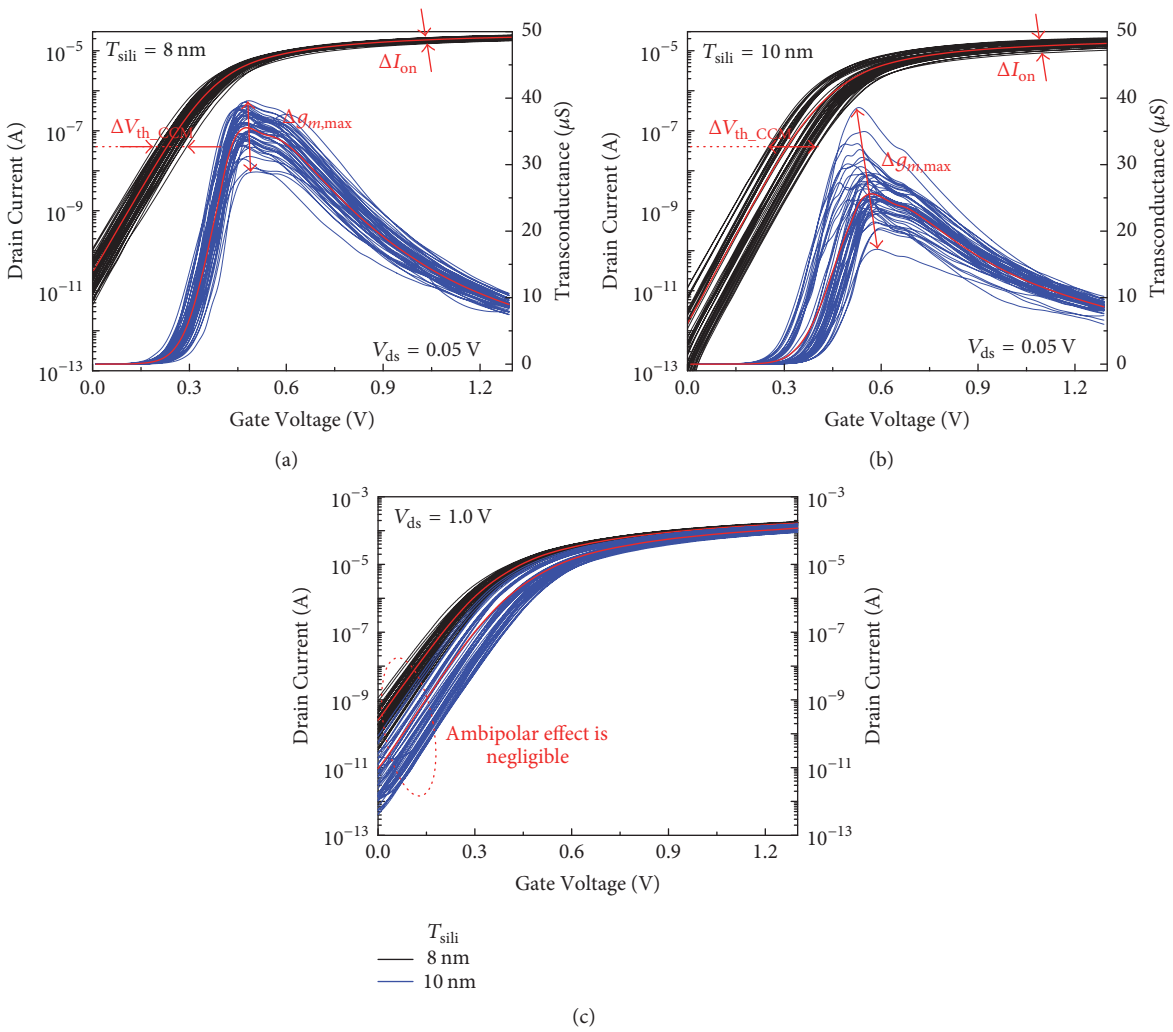

Figure 2: DC performance and variations of the SOI FinFETs with the T_{sili} of (a) 8 and (b) 10 nm at drain voltage (V_{ds}) of 0.05 V and (c) 1.0 V. The number of measured devices is 50 for each T_{sili}.

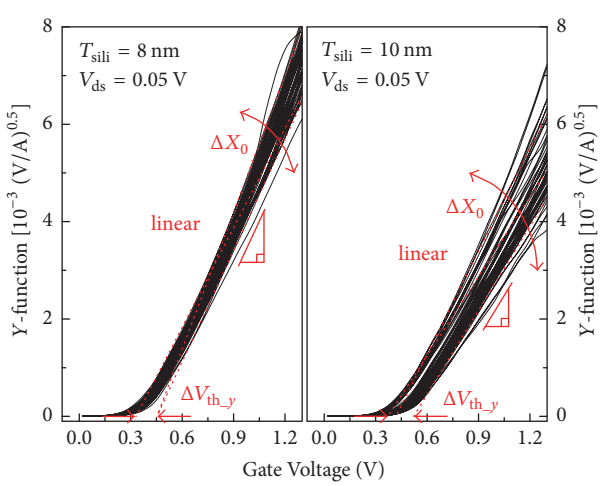

Figure 3: Y-function variations of the SOI FinFETs with T_{sili} of 8 and 10 nm. Almost all the Y-functions satisfy the linearity condition in the strong inversion regime.

because all the devices have omega-shaped structure with ultra-thin fin channel, which induces volume inversion and thus attenuates the surface roughness scattering.

Figure 4 shows V_{th_y}, X_0, and R_{sd} of the measured devices at V_{ds} of 0.01, 0.02, 0.03, 0.04, and 0.05 V extracted from Y-function method. Average X_0 and R_{sd} are independent of V_{ds}, whereas V_{th_y} increases slightly as V_{ds} increases. V_{th_y} includes the band-bending by gate voltage as well as the body-effect expressed by $m/2 \cdot V_{ds}$, where m is the body-effect coefficient (m is simply approximated as 1 for fully depleted devices), thus showing a slight increase of V_{th_y} with the slope of $V_{ds}/2$ as V_{ds} increases [23]. The devices with T_{sili} of 8 nm show greater X_0 and smaller R_{sd} due to greater NiSi/Si contact area.

The devices with T_{sili} of 10 nm have greater variations of V_{th_y}, X_0, and R_{sd} (Figure 4). Standard deviations (σ) of X_0 and R_{sd} for T_{sili} of 10 nm increase by 62.4 and 48.5%, respectively, with respect to those for T_{sili} of 8 nm. Not only V_{th_y} but also V_{th_CCM} variations are severer for T_{sili} of 10 nm

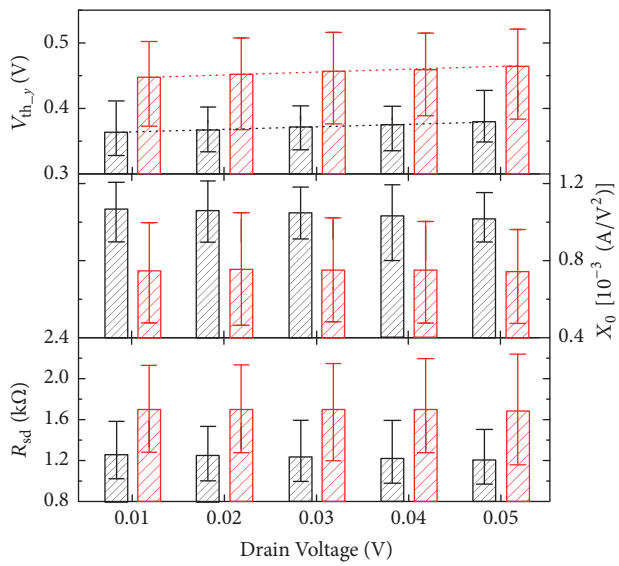

FIGURE 4: Average and standard deviations of dc parameters for the SOI FinFETs with T_{sili} of 8 nm (black) and 10 nm (red) at different V_{ds}: V_{th_y}, X_0, and R_{sd}.

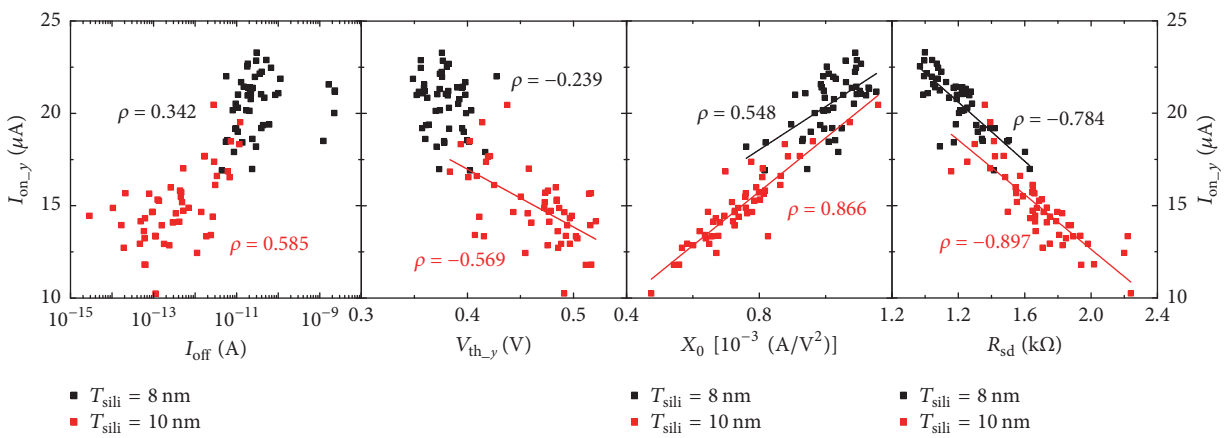

FIGURE 5: Scatter plots of I_{on_y} at ($V_{gs} - V_{th\_y}$) of 0.8 V with respect to the DC parameters (I_{off}, V_{th_y}, X_0, and R_{sd}) for the SOI FinFETs at V_{ds} of 0.05 V. All the linear regressions indicate the sensitivity of I_{on_y} with respect to the DC parameters.

(σ = 45 mV) than for T_{sili} of 8 nm (σ = 22 mV) at all different V_{ds}.

3.2. DC Performance Variability Analysis. To investigate why the devices with T_{sili} of 10 nm suffer from smaller DC performance and greater variations, correlation analysis of I_{on} with off-state currents (I_{off}), V_{th_y}, X_0, and R_{sd} is done in Figure 5. Spearman's correlation is used to calculate the correlation coefficient (ρ) [15]. I_{off} values are I_{ds} at V_{gs} of 0.0 V, whereas all the I_{on} values are extracted at the gate overdrive voltage ($V_{gs} - V_{th\_y}$) of 0.8 V (I_{on_y}) to neglect the V_{th_y} effect [24]. Since all the devices have similar SS and no gate-induced drain leakages, I_{off} is mostly determined by V_{th_y} (ρ = −0.781 and −0.907 for T_{sili} of 8 and 10 nm, resp.). Due to these perspectives, therefore, a slight correlation between I_{on_y} and I_{off} along with V_{th_y} is expected.

Nonetheless, there are correlations between I_{off}, V_{th_y}, and I_{on_y} for T_{sili} of 10 nm (left of Figure 5). In addition, V_{th_y} for T_{sili} of 10 nm is correlated with X_0 (ρ = −0.530) and R_{sd} (ρ = 0.491), whereas V_{th_y} for T_{sili} of 8 nm is independent of X_0 (ρ = −0.077) and R_{sd} (ρ = 0.200) at all different V_{ds}. X_0 is also correlated with R_{sd} for T_{sili} of 10 nm (ρ = −0.581), whereas the correlation is small for T_{sili} of 8 nm (ρ = −0.162).

These high correlations among all the DC parameters (I_{off}, V_{th_y}, X_0, R_{sd}) and I_{on_y} for T_{sili} of 10 nm are related to the high SBH at the NiSi/Si interface. Higher SBH for thicker T_{sili} is expected due to greater lateral encroachment of NiSi into the S/D extension regions [19, 25]. Greater V_{th_CCM} (or V_{th_y}) and larger R_{sd} for T_{sili} of 10 nm are the indicatives of higher SBH according to equation (2) in [26] and higher contact resistivity [27], respectively. Higher SBH for thicker T_{sili} requires much band-bending for the carrier injection from source (related with I_{off} and V_{th_y}) and impedes carrier

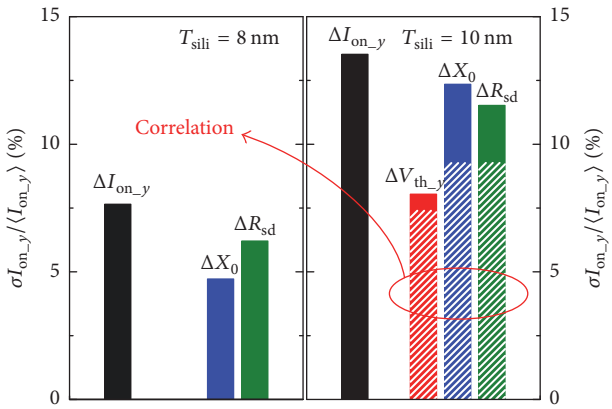

FIGURE 6: I_{on_y} variations and variations of the dc parameters (V_{th_y}, X_0, and R_{sd}) contributing to the I_{on_y} variations for T_{sili} of 8 and 10 nm.

flow under operation (related with X_0, R_{sd}, and thus I_{on_y}) [28]. For the low-SBH devices, the SBH variations induce the on-state performance variations, not the V_{th} variations [26]. Therefore, the V_{th} variations for T_{sili} of 8 nm are dominantly induced by other variability sources (gate work function (WF) variation [24], RDF [15], and interface traps [29]) except the SBH. And that is why V_{th_y} for T_{sili} of 8 nm is not correlated with X_0, R_{sd}, and I_{on_y}.

Greater variations of all the DC parameters for T_{sili} of 10 nm can also explain the increased SBH and its variations. The R_{sd} variations for SOI FinFETs are dominantly affected by NiSi/Si contact resistance [20, 27]. The NiSi/Si interface consists of NiSi crystal grains having different WF and surface roughness [14]. The extension regions suffer from RDF [15] along with the WF variations, having different SBH at each of NiSi crystal grains and also for each of the devices. And this induces the SBH variations greatly for T_{sili} of 10 nm due to smaller contact area.

Figure 6 shows the relative contributions to the I_{on_y} variations with respect to the DC parameters each. When the DC parameters are correlated with each other, the contributions to the variations of I_{on_y} for the correlated portion are calculated using the correlation coefficient, sensitivity (the slope of scatter plots in Figure 5), and standard deviations [24]. All the correlated portions are presented as the shaded area. All the three DC parameters are correlated with each other and the X_0 variations affect the I_{on_y} variations greatly for T_{sili} of 10 nm, whereas they are independent and the R_{sd} variations affect the I_{on_y} variations greatly for T_{sili} of 8 nm.

3.3. Low-Frequency Noise Analysis. Low-frequency noise was measured at V_{ds} of 0.05 V and at the overdrive voltage ($V_{ov} = V_{gs} - V_{th\_CCM}$) of 0.3 V (Figure 7). Frequency range was from 1 to 1000 Hz, and the 10 devices each with T_{sili} of 8 and 10 nm, closest to the average I_{ds}, were measured. All the results follow the $1/f$ trend except at the frequency near 1 Hz where Lorentzian-type noise plateau is observed due to the small-area devices. The devices with T_{sili} of 10 nm have greater average S_{Ids} for all the frequency range.

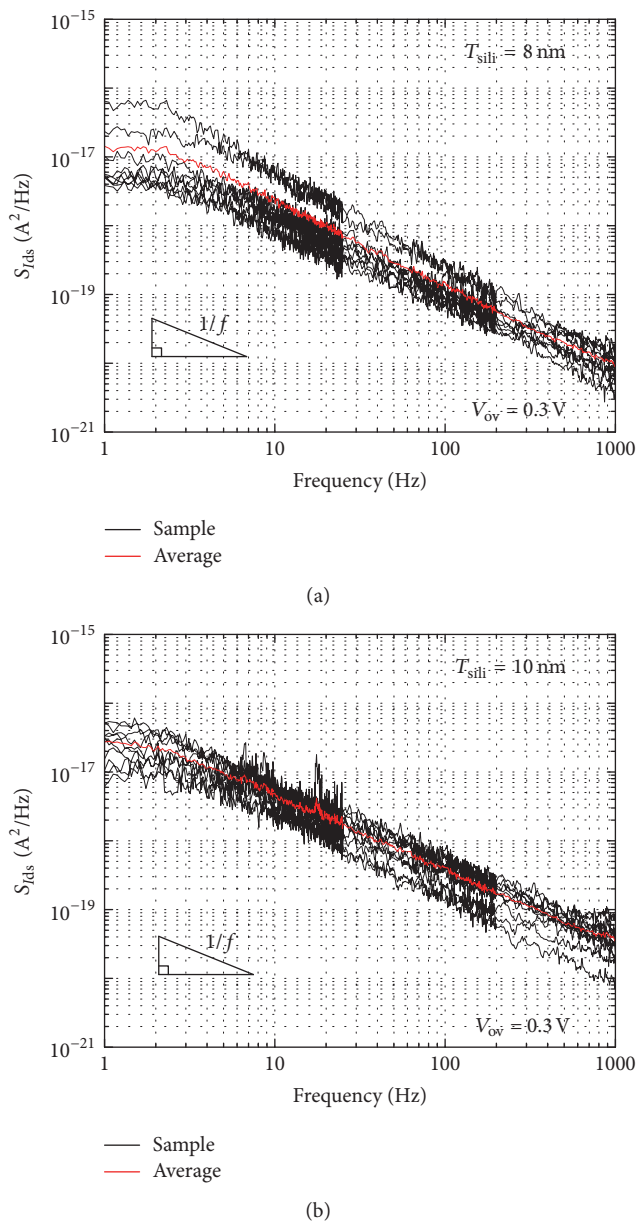

FIGURE 7: Drain current noise spectral density (S_{Ids}) measured at V_{ds} of 0.05 V and the overdrive voltage ($V_{ov} = V_{gs} - V_{th\_CCM}$) of 0.3 V for T_{sili} of (a) 8 and (b) 10 nm. The number of measured devices, close to the average I_{ds}, is 10 each.

Figure 8 shows S_{Ids} normalized by ${I_{ds}}^2$ of the devices with different T_{sili} at V_{ov} from 0.1 to 0.6 V in steps of 0.1 V measured at 10 Hz. In case of V_{ov} from 0.3 to 0.6 V, the normalized S_{Ids} values are almost independent of V_{ov}, where the noise induced by R_{sd} (S_{Rsd}) is dominant to the device [30]. The noise within the channel (S_{Rch}) is from the Si/SiO_2 interface and the channel itself, whereas S_{Rsd} is from the S/D contact at NiSi/Si interface. But the quality of Si/SiO_2 interface is almost similar for all the devices because the only difference is RTP, performed under low temperature around 300~450°C [13, 19, 20, 31, 32] enough not to induce the Si/SiO_2 interface damage. In spite of that, the devices with T_{sili} of 10 nm have greater

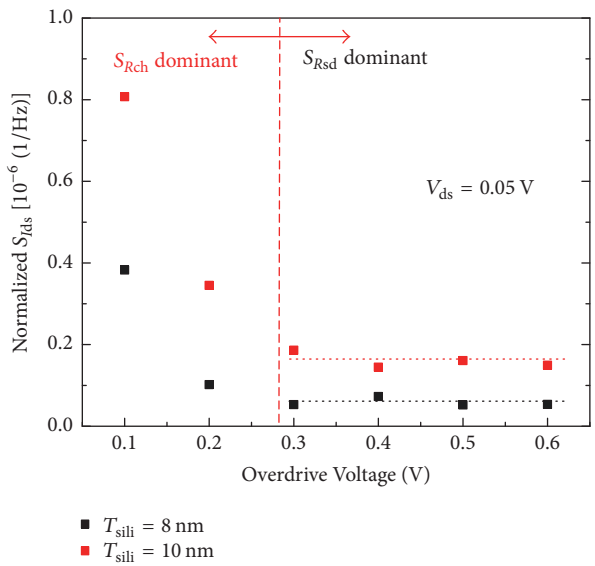

FIGURE 8: Normalized S_{Ids} at 10 Hz with respect to I_{ds} at different V_{ov}.

S_{Rch} because high SBH close to the lightly doped extension region decreases X_0 (related to μ_{eff}) which is correlated with R_{sd}. Greater S_{Rch} for T_{sili} of 10 nm is also explained by the lateral encroachment of NiSi into the S/D extension regions. More lateral encroachment of NiSi for thicker T_{sili} induces higher SBH, which impedes the carrier flow and decreases the channel length [33]. These physical phenomena increase S_{Rch} according to equation (3) of [30]; thus the greater S_{Rch} for T_{sili} of 10 nm is obtained (Figure 8). As a result, the devices with T_{sili} of 10 nm have greater normalized S_{Ids} for all V_{ov}.

4. Conclusions

DC performance and variability of the dopant-segregated SOI FinFETs with different T_{sili} are analyzed in terms of the DC parameters extracted from Y-function method and Spearman correlation, respectively. Thicker T_{sili} degrades DC performance by decreasing I_{on} and $g_{m,max}$ and fluctuates V_{th}, X_0, R_{sd}, and I_{on} greatly because the SBH increases greatly and varies along with WF variation and RDF at the S/D region. In addition, the devices with T_{sili} of 10 nm suffer from large low-frequency noise due to high SBH, which is caused by greater lateral encroachment of NiSi into the S/D extension regions and related to greater variations and correlations of V_{th_y}, X_0, R_{sd}, and I_{on_y}. Therefore, the device with relatively thin T_{sili} is promising to improve DC performance and minimize the variation.

This variability study would be helpful to design nanoscale devices having a few dopants and small contact area because the SBH values and variations of the devices depend on T_{sili} greatly.

Data Availability

All the data analyzed in this study are included in this published article.

Conflicts of Interest

The author declares that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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Supplementary Materials

Supplementary materials contain one figure (Figure S1). Figure S1: on-state resistance (R_{on}) as a function of fin width (W_{fin}) for different T_{sili} of 8 and 10 nm. The number of fins (N_{fin}) for each device is 20. As W_{fin} increases from 40 to 80 nm, the difference of R_{on} between two different T_{sili} decreases from 36 to 23%. *(Supplementary Materials)*

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