Hindawi
Advances in Condensed Matter Physics
Volume 2018, Article ID 4927829, 8 pages
https://doi.org/10.1155/2018/4927829

Research Article

Peculiarities of Charge Transfer in SiO_2(Ni)/Si Nanosystems

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Received 31 January 2018; Accepted 17 May 2018; Published 2 July 2018

Academic Editor: Yuri Galperin

This work is devoted to study the peculiarities of charge transfer in SiO_2(Ni)/Si nanosystems formed as a result of the electrochemical deposition of nickel into the pores of the ion-track silicon oxide template on silicon. Special attention is given to analysis of the results in the context of the band structure and physical properties of dielectric on semiconductor systems with metallic inclusions in the dielectric matrix. Experimental studies of the current-voltage characteristics of SiO2(Ni)/Si nanostructures demonstrated that value of potential barrier on the Si/metal interface in the pores of the silicon oxide template depended on temperature. On the basis of these results an interpretation of the charge transfer mechanisms in SiO_2(Ni)/Si nanosystems at different temperature ranges was proposed. In the temperature region of ~300–200 K charge carrier motion occurs through the *n*-Si with an employment of metallic clusters in pores being in a contact with the semiconductor, by means of the overbarrier emission of electrons from higher energy levels of Si conduction band. In the lower temperatures (~200-100 K) a current flow takes place only through the semiconductor due to an increase of resistivity on energy barriers *n*-Si/metal, which leads to a practically complete exclusion of a participation of the metal in the charge transport process. In the low temperatures (~100–20 K), the variable range hopping conduction between pores on the SiO_2/Si boundary, containing localized states, dominates.

1. Introduction

Nanostructured materials are a special state of condensed matter with properties not usual for materials with mesoscopic or microscopic dimensions. Nanostructures are widely used in biomedicine, chemistry, physics, electronics, and materials science [1–5] and application areas are constantly expanding. It initiates an active search for new approaches to the creation of various types of nanostructures [6–11]. Natural conditions for nanostructures formation are realized using a porous dielectric template on a semiconductor, for the creation of which it is reasonable to use the technology of swift heavy ions tracks [12, 13]. This technology makes it possible to create pores in the silicon oxide layer, the filling of which with appropriate materials, organically adapts resulting heterostructures to the silicon technology standards [14, 15]. The system complexity, which connected with discreteness of metal particles in contacted with the semiconductor and separated by dielectric interlayers of pores, predetermines the nontriviality of charge transfer processes, the dominant mechanisms of which will be different in a wide range of temperatures and magnetic fields. In such structures, a number of unusual physical effects are noted [16, 17], among which one of the most interesting is the magnetoresistance [17]. Despite intensive studies on nanosized metallic inclusions, a systematic research analyzing those nanoinclusions with respect to electrophysical and galvanometric properties is required. This study is carried out based on the analysis of electrophysical characteristics of systems, containing electrochemically deposited nickel particles in pores of silicon oxide on silicon.

2. Materials and Methods

To create SiO_2(Ni)/Si structures, porous templates of silicon oxide on silicon were used. Si/SiO_2 has the following characteristics: electronic conductivity; doped with phosphorus with donor impurity concentration $N_D = 9 \times 10^{14}$ cm^{-3}, resistance 4.5 $\Omega * cm^{-1}$) obtained using of fast heavy ion tracks technology (irradiation with $^{197}Au^{26+}$ ions with energies of 350 MeV and fluence of 5×10^8 cm^{-2}); through (up to the Si surface) pores with truncated conic shape (base diameters of ~ 300 nm on SiO_2 surface and ~ 200 nm on the boundary with Si) and length corresponding to dielectric layer thickness (~ 350 nm) and average distances between pores of 500 nm. The features of produced SiO_2(Ni)/Si templates are described in detail in our previous work [18].

SiO_2(Ni)/Si nanosystems was made using of boric acid electrolyte (0.5 mol/l H_3BO_3) and nickel sulfate containing solution (0.5 mol/l $NiSO_4$), which was used as cations source. The selected concentration of $NiSO_4$ promoted maximum deposition rate [19, 20]. The electrodeposition potential value was −1 V; it ensured the current efficiency of metal of about 93.3%. The degree of pores filling with metal was controlled by changing process time. The error in potentials measured during deposition did not exceed 1 mV, and the current was not more than 25 nA.

The morphological features of SiO_2(Ni)/Si samples were measured by scanning electron microscopy (SEM, LEO-1455VP, Carl Zeiss (Germany). Elemental analysis was provided by energy dispersive analysis system (EDS, included to LEO-1455VP). The study SiO_2 surface morphology and distribution of outgrown/unreached metal clusters on it was carried out by atomic force microscopy (AFM, NT-206, Microtestmachinery, Belarus) using silicon nitride (Si_3N_4) cantilever with rounding radius of 10 nm. The degree of metallic phase localization in dielectric pores and its outgrowth on SiO_2 surface was determined by X-ray spectral microanalysis (SiLi detector, Röntec).

SEM studies (Figures 1(a), 1(b), and 1(c)) and mapping with X-ray spectral microanalysis (Figures 1(d) and 1(e)) of surface (Figures 1(a), 1(b), and 1(d)) and cross sections (Figures 1(c) and 1(e)) of Si/SiO_2(Ni) samples showed that nickel precipitates uniformly and completely fills the pores, without formation of any outgrown or unreached metal clusters. AFM-scanning of surface showed that change in surface relief does not exceed 40 nm. Carrying out of samples elemental composition analysis by mapping surface and cross sections during X-ray spectral microanalysis, it was established that nickel was localized exclusively in Si/SiO_2 template pores, without nucleation on SiO_2 surface. Our previous studies [21, 22] showed that formed precipitates consist of metal nanoclusters with size of ~ 30-50 nm with stochastic crystallographic orientation.

To study the current-voltage characteristics (I–V curves) of SiO_2(Ni)/Si nanosystems, samples with size of 10×3 mm^2 were prepared. On their surface from the side of SiO_2(Metal), contact area of ~1 mm^2, to which copper electrodes were fed (Figure 2), was applied by ultrasonic soldering with indium. Such contacting method provided mechanically stable ohmic contact to the sample, which was then verified by thermal cycling over a wide range of temperatures. The I–V curves were investigated in the temperature range of 4-300 K using universal measurement system "Liquid Helium Free High Field Measurement System" (Cryogenic Ltd). The measurement error throughout temperature range did not exceed 5%.

3. Results and Discussion

The value of the specific electrical conductivity of semiconductors, depending on type and concentration of impurities and defects, can change by several orders. In addition, such factors as complexity and heterogeneity of interfaces of contacting materials with substantially different band structure affecting on conductivity are important. It leads to an additional resistance associated with the appearance of an energy barriers and dimensional and edge effects.

To understand a dominant factor having effect on studied system, it is necessary to predict the conditions of current transfer. Schematic representation of current flow paths through the structure was presented in (Figure 2). It is apparent that, at room temperature, presence of silicon substrate, metal-semiconductor interface, and the contact electrical resistivity between the metal clusters in the pores are the predominant factors affecting electrical transfer.

Charge transfer through the pores in dielectric template occurs over concatenation of metal particles pervading entire pore from electrode to boundary with semiconductor. According to [5], the current flow through such clusters grid provides predominantly metallic type of conductivity in spite of the fact that dielectric layers are possible, it is associated with oxides formation on clusters surface. They increase electrical resistivity of material as a whole, but do not affect the conduction mechanism [23, 24].

During current transfer through SiO_2 (Ni)/Si nanosystems after the passage of concatenation of metal particles, the charge carriers continue to move through the silicon substrate, where the electronic type of conductivity is predominant. After the passage of silicon, charge transfer is again provided by metal particles located in the pores. The processes of electromigration in silicon were thoroughly studied and described in detail in [25–27].

When charge carriers move from metal to semiconductor and back, depending on thermodynamic work functions ratio, different types of contacts can be realized: neutral, ohmic, nonohmic (Schottky barrier). To determine the contact type, it is necessary to know the peculiarities of SiO_2(Ni)/Si nanosystems band structure of nickel/silicon contact region.

It is known that the work function of nickel $W_{Ni} = 4.9$ eV and n-Si (100) $W_{Si} = 4.3$ eV [28]. Since the relation $W_s < W_{Me}$ is satisfied when the metal is in contact with semiconductor, current of thermionic emission from semiconductor surface is greater than from metal surface. Therefore, in the contact zone of metal particles with silicon, a positive space charge accumulates, and it leads to formation in contact region of an electron-depleted region of depth d_0 (Figure 3(a)) and

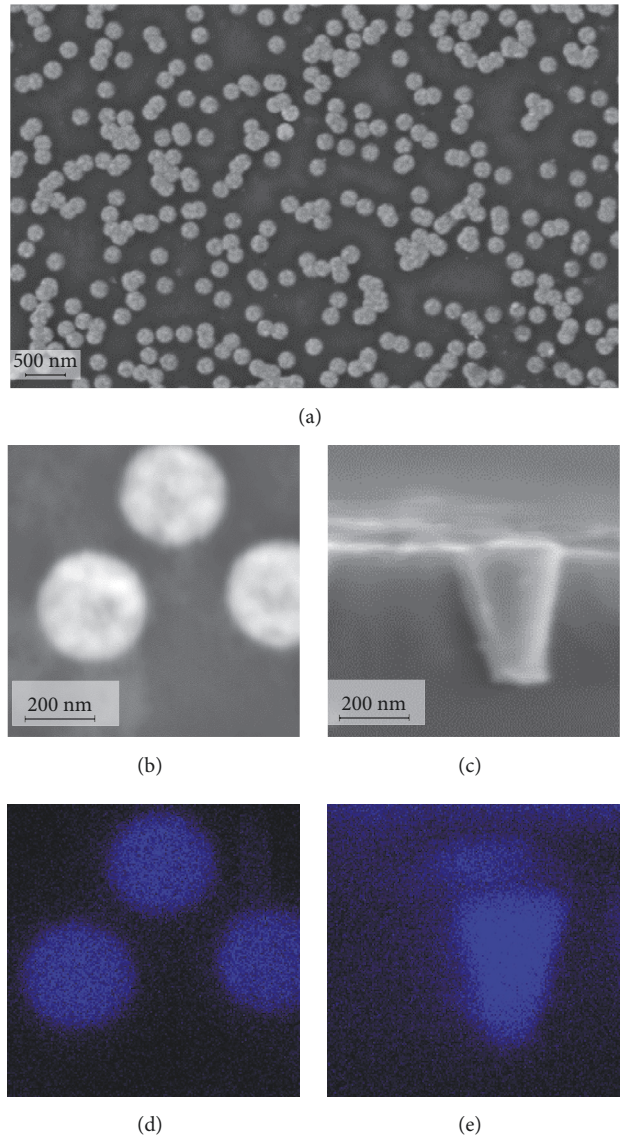

Figure 1: SEM images SiO_2(Ni)/Si nanosystems: surface (a, b), cross sections, (c) and EDS mapping images (d, e) of regions (b, c).

bending of energy bands (Figure 3(b)) with the formation of Schottky barrier. The values of barrier height, determined by difference of work function $\varphi_к = W_{Me} - W_s$, are found to be 0.6 eV for nickel.

The application of an external electric field with "+" sign on the metal side (Figure 3(c)) leads to decreasing of potential barrier height and value of electric field in space semiconductor charge region d_+ (Figure 3(d)). The application of E_{ext} in opposite direction (Figure 3(d)) contributes to an increasing of potential barrier and depletion region depth d_- (Figure 3(e)).

Thus, during applying voltage in any direction, the current will flow through SiO_2(Ni)/Si nanosystem in the metal-semiconductor-metal scheme. At the same time, on one contact, electrons freely move from metal to semiconductor, and on the other (during transition from semiconductor to metal) they overcome the potential barrier; that is, the contacts have rectifying properties. Accordingly, in this structure a symmetric I–V curve with two Schottky barriers included towards each other should be observed.

Such property of band structure in the contact region of metallic clusters with n-silicon is observed on an ideal (infinitely large and homogeneous) interface. Accounting of inhomogeneities due to relief and size of contact surface introduces additional corrections to the potential barrier value and I–V curves behavior due to the fact that the actual interface has emission parameters, which substantially differs from corresponding parameters of ideal barrier.

Metallic nanoparticles localized in pores do not have a preferential crystallographic orientation. This fact can affect the height of Schottky barrier in both its increasing and decreasing. The reason for such changes is the difference in work functions for different crystallographic faces, and such difference reaches values of ~ 1 eV (in nickel it fluctuates

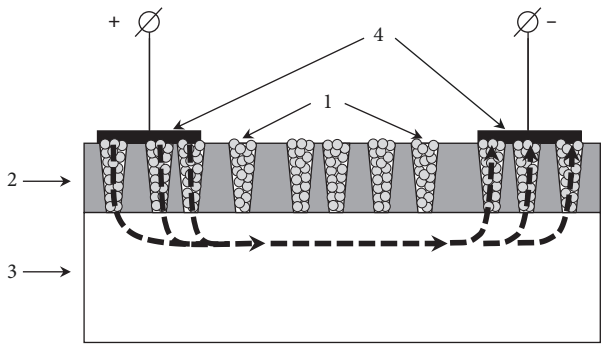

Figure 2: Schematic representation of SiO_2(Ni)/Si nanosystems. (1) Metal in the pores, (2) silicon oxide layer, (3) silicon substrate, and (4) electrodes.

within 4.6-5.5 eV [29]). In addition, it is necessary to take into account the small area and inhomogeneity of contact surface. Applying the reverse bias voltage, considerable currents leakage can arise from curvature of space charge region of semiconductor along the contact periphery; it helps to reduce the actual height of potential barrier. Moreover, the number of metal pores filled with current electrodes (Figure 2) is large but the area of electrical contact with semiconductor is a set of parallel connected and electrically noninteracting microcontacts, as a result the potential barrier value has a certain averaged value. For these reasons, it is impossible to correctly estimate the potential barrier without conducting an experimental study of SiO_2(Ni)/Si curves I-V. Typical results of current-voltage characteristics measuring for samples with nickel nanoparticles in pores are shown in Figure 4(a).

These characteristics present two symmetrical Schottky barriers, which are formed in different directions of current flow and charge transfer from a silicon substrate to metal clusters. It is easy to determine the height of potential barrier. The current flowing through the Schottky barrier is determined by the Richardson equation [30]:

$$I_0 = SAT^2 \exp\left(-\frac{\varphi_k}{kT}\right), \quad (1)$$

where I_0 is the saturation current; S is metal-semiconductor contact area; A is Richardson constant; k is Boltzmann constant.

So equation can be rewritten as follows:

$$\varphi_k = kT \exp\left(-\frac{SAT^2}{I_0}\right). \quad (2)$$

The contact area S is defined as the effective contact area of one pore (10^4 nm^2) multiplied by the number of pores under the conductive electrode (10^6) and is 10^{-4} cm^2.

The Richardson constant is usually assumed to be 120 A cm^{-2} K^{-2}, but in [31] it is indicated that the experimental values of A may not coincide with the given value. It should be noted that the value of $\varphi_к$ is not very sensitive to the choice of the Richardson constant, because even at room temperature the error twice as large in parameter A leads to an error in determining $\varphi_к$ by only 0.018 eV.

The value of I_0 is determined as follows: the branch of the current-voltage characteristic, plotted in scale $\ln I$ from $V^{1/4}$, for $V \gg kT/e$, is represented by a straight line. By extrapolating the linear part of the dependence on the semilogarithmic scale $\ln I$, the saturation current at $V = 0$ V (Figure 4(b)), which is 1.08×10^{-6} A, is on the ordinate axis. Thus, in accordance with (2), the value of potential barrier was $\varphi_к = 0.56$ eV; it correlates well with the data obtained earlier for the contact of nickel with silicon [32, 33].

The analysis of the I-V curves obtained in the temperature range of 25-300 K (Figure 5(a)) shows that the dependencies are symmetric, qualitatively similar to each other with the preservation of two distinct Schottky barriers in the entire temperature range. As the temperature is lowered, the nonlinearity of the I-V curves begins to appear at higher voltages and has a sharper character, which is associated with increasing of potential barrier and is accompanied by an increase in the resistance at barrier: at $T = 25$ K the resistance of the structure reaches values of the order of 10^8 ohm, becomes of the order of 10^6 ohm at $T = 100$ K, and goes down to $\sim 10^5$ ohm at room temperature. It is explained by the fact that as the temperature increases, electrons in the semiconductor layer near the Schottky barrier are excited to higher energy levels and, accordingly, the tunneling probability of barrier increases (Figures 5(b) and 5(c)).

In the room temperature region, the energy of electrons thermal motion kT is commensurable with band gap, so the electrons go from the valence band to the conduction band with the formation of pair charge carriers (electrons and holes). With temperature decreasing, the number of such electrons decreases, leading to a sharp increase in the resistance. Then there is depletion of the impurity, and the resistance increases due to increasing of silicon band gap width, when temperature decreases.

It should be taken into account that, in the region of metal-semiconductor contact, the relief of valence band and conduction band changes. It leads to competition of tunneling through a potential barrier with charge carriers activated at the percolation level [34, 35]. By the level of percolation it is usually understood the energy, with which the charge carrier moves through the sample from one contact to another contact, bending around the barrier (above-barrier emission). It is clear that at high temperatures the conductivity is predominant in terms of the percolation level, while at low temperatures the tunneling of electrons from one potential well to the other at Fermi level is dominant.

With a resistance at the Schottky barrier less than silicon resistance, charge transfer occurs over the metal, then the charges move in the silicon layer to the next filled track, and the process is repeated in the same way further, leading to a decrease in the system impedance. In addition to such transitions from silicon to metal and back, such mechanisms as the Schottky thermionic emission (at high temperatures) and tunnel emission of charges or hopping conductivity (at low temperatures) can also influence process of charge transfer [17].

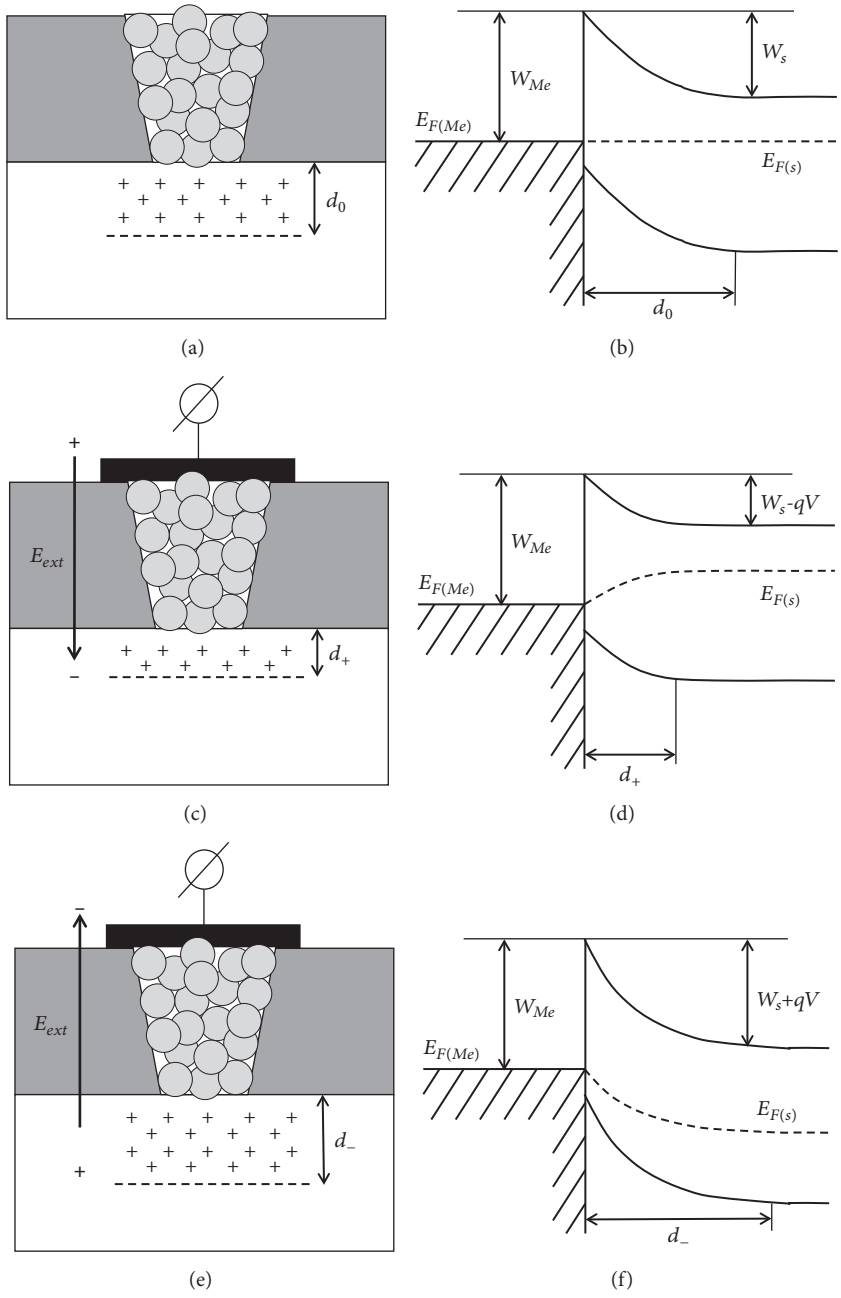

FIGURE 3: Schematic representation of electron-depleted region formation in contact area of metallic particles with *n*-Si in absence of an external electric field (a), at E_{ext} with "+" sign on metal side (c), with a "–" sign (e); scheme for band structure formation in contact region at $E_{ext} = 0$ (b), $E_{ext} > 0$ (d), $E_{ext} < 0$ (e).

Summarizing the above findings it is possible to propose the following interpretation of the mechanisms of charge transfer in SiO_2(Ni)/Si nanosystems realized in different temperature ranges:

(i) In the region ~300–200 K: charge carrier motion through the *n*-Si with an employment of metallic clusters in pores being in a contact with the semiconductor, by means of the overbarrier emission of electrons from higher energy levels of Si conduction band

(ii) In the lower temperatures region (~200–100 K): a current flow taking place only through the semiconductor due to an increase in resistivity on energy barriers Si/metal, which leads to a practically complete exclusion of a participation of the metal in the charge transport process

(iii) In the low temperatures region (~100–20 K): a domination of hopping charge transport with a variable hopping length between pores on the SiO_2/Si boundary, containing localized states.

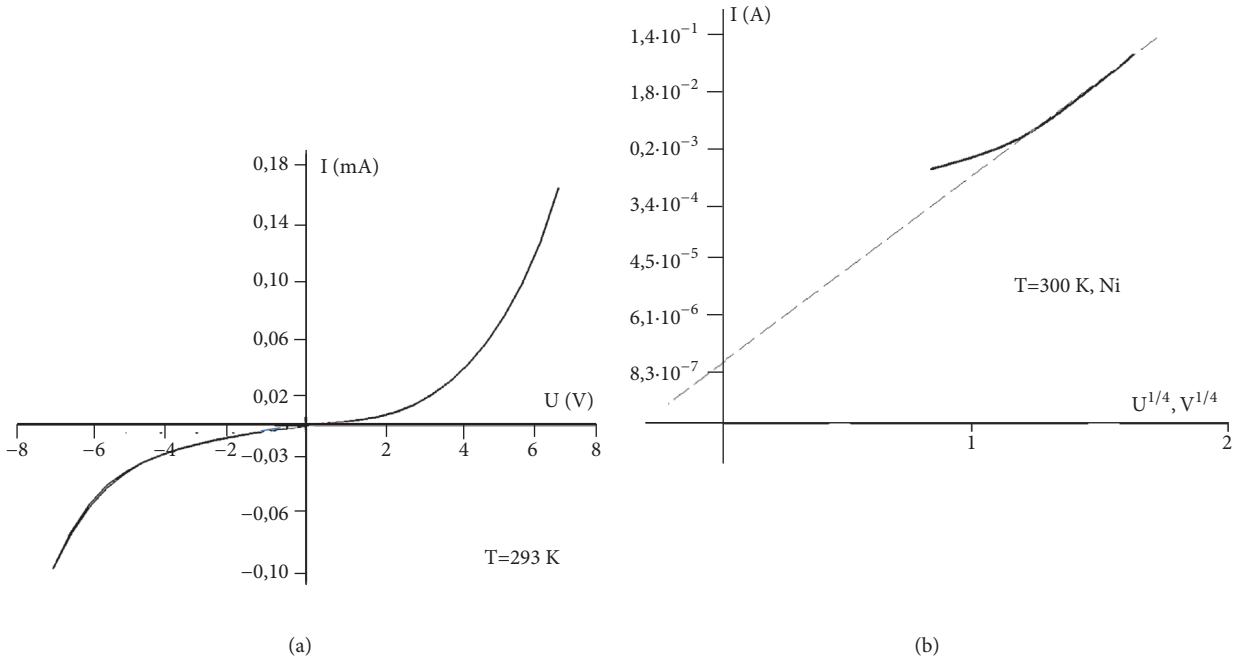

FIGURE 4: I–V characteristics curves of SiO_2(Ni)/Si nanosystems at room temperature: I–V curve (a). Dependencies of $\ln I$ on $V^{1/4}$ and the approximating curve for structures (b).

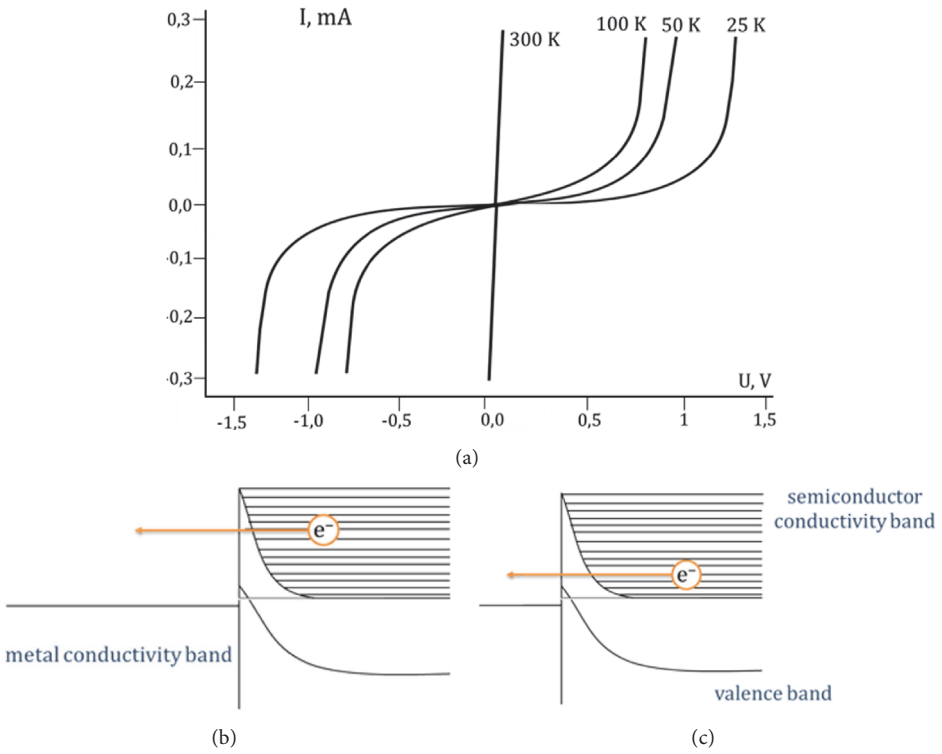

FIGURE 5: (a) I–V curves of SiO_2(Ni)/Si nanosystems for different temperatures. Band structure of n-type semiconductor system, metal with a Schottky barrier: (b) at high temperatures; (c) at low temperatures.

4. Conclusions

Data on the formation of SiO_2(Ni)/Si nanosystems with nickel in the pores of amorphous silicon oxide and the results of its electrical characteristics over a wide temperature range are presented. It is shown that ion-track technology can serve as a connecting link for the adoptive nanosystems to the technological processes of standard silicon technology. It was demonstrated that the selected electrochemical deposition method, due to the high degree of control, allows selectively filling the pores with Ni, at a minimum spread of the protuberances of the metal precipitate over the surface of the template. When considering the mechanisms of charge transfer, it is shown that as the charge carriers move into a pore, a metallic type of conductivity is realized. A Schottky barrier is created at the bottom of the pore thanks to the presence of silicon. Investigations of the current-voltage characteristics show that dependencies are typical for structures with double Schottky barrier. The value of potential barrier at *n*-Si/Ni interface (0.56 eV) was determined. It was shown that applying of external electric field to metal-semiconductor contact with plus sign on the metal side leads to decreasing of potential barrier height in the region of semiconductor space charge, and applying of inverse field leads to increasing of barrier and charge-depleted region depth. Analyzed current-voltage curve indicates that, over the entire temperature range 25-300 K at high voltages, the nonlinear character of I–V curve takes place, which causes increasing of potential barrier. In this case, the resistance on barrier increases: at T = 25 K structure resistance is of the order of 10^8 ohms, at T = 100 K it is 10^6 ohms, and at room temperatures it decreases to 10^5 ohms.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Disclosure

This material have been presented as poster presentation at the XXII International Scientific Conference of Young Scientists and Specialists (AYSS-2018) 23-27 April 2018.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

This work was supported by the Scientific-Technical Program "Technology-SG" (Project no. 3.1.5.1) and Belarusian Foundation for Basic Research (Project no. Ф17М-005).

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