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Research Article

Electrical Characterization of Postmetal Annealed Ultrathin TiN Gate Electrodes in Si MOS Capacitors

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Focusing on sub-10 nm Silicon CMOS device fabrication technology, we have incorporated ultrathin TiN metal gate electrode in Hafnium Silicate (HfSiO) based metal-oxide capacitors (MOSCAP) with carefully chosen Atomic Layer Deposition (ALD) process parameters. Gate element of the device has undergone a detailed postmetal annealed sequence ranging from 100°C to 1000°C. The applicability of ultrathin TiN on gate electrodes is established through current density versus voltage (J-V), resistance versus temperature (R-T), and permittivity versus temperature analysis. A higher process window starting from 600°C was intentionally chosen to understand the energy efficient behavior expected from ultrathin gate metallization and its unique physical state with shrinking thickness. The device characteristics in form of effective electronic mobility as a function of inverse charge density were also found better than those conventional gate stacks used for EOT scaling.

1. Introduction

As the miniaturization and scaling-down of CMOS manufacturing technology continues to sub-22 nm node, usage of metal gates with high-k dielectrics is getting increasingly desirable to minimize quantum gate tunneling and associated leakages [1]. The problems associated with the use of Poly-Si depletion, high resistivity, boron penetration, Fermi level pinning, and so forth can be addressed effectively by fabricating the combination of the metal gate and high-k stacks in MOSCAP and CMOS structures [2–4]. Novel materials to be used as gate materials such as TiN and TaN have the property to tune the work function in accordance with the process requirements due to their thermal stability [5]. The TiN/TaN double-layer stack is also incorporated to tune the work function for the MOSCAP structure [5, 6]. The added advantage of TiN is its midgap work function and alongside compatibility with the standard CMOS processing techniques making it a viable choice to investigate it further [7–13].

In this study we analyze the MOSCAP structure as part of the CMOS routine in terms of its sensitive electrical characteristics where the focus lies on the TiN gate electrode formed by a carefully chosen Atomic Layer Deposition process matrix. The device sensitive electrical behavior is mapped with respect to change in the postprocess annealing window to analyze the energy efficiency of the manufacturing process.

2. Experimental

Devices were fabricated by utilizing 2.9 nm HfSiO layer as high-k dielectric material in standard MOSCAP structure. The deposition of both the high-k dielectric HfSiO layer and 1.5 nm TiN metal gate was accomplished with Atomic Layer Deposition system. Details of ALD parameters are reported elsewhere [14]. The deposition chamber was preheated at 315°C. A high-k dielectric layer is deposited on Si (100) wafers by injecting the Hf and Si liquid precursors one by one. This resulted in a proper reaction yielding a fine layer of dielectric material. TiN layer, as a follow-up step, was deposited on top of the dielectric layer using the same ALD technique. With the chamber temperature maintained at 400°C, $TiCl_4$ and NH_3 gases were duly injected in the reaction chamber [15–17]. N_2 was used as a carrier gas which also acted as a purge gas at the same time. Ammonia gas was used as a

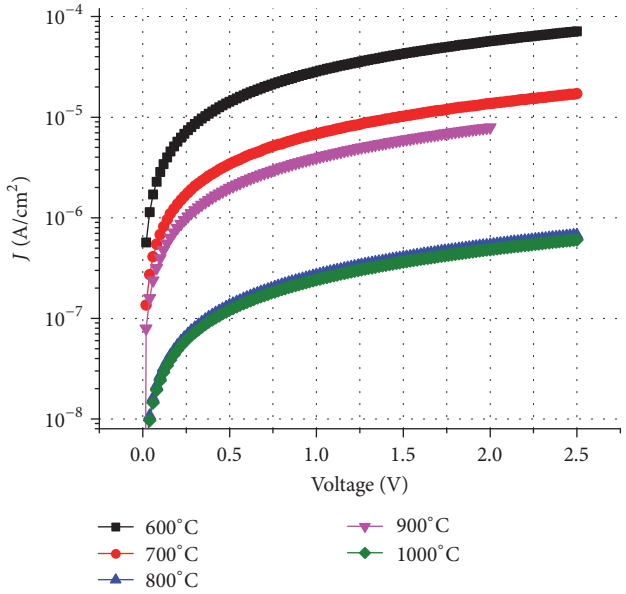

Figure 1: J-V curves for ultrathin ALD processed TiN gate in Si MOSCAP structure at different annealing temperatures.

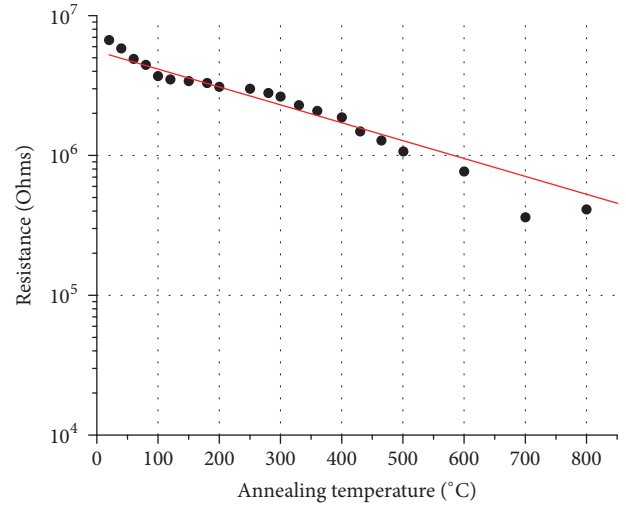

Figure 2: Resistance analysis of the TiN thin film as a function of postmetal annealing temperatures.

reactant in this process. The working pressure of the ALD reaction chamber was maintained at 0.55 Torr. The annealing sequences were performed on the Rapid Thermal Processor (RTP) during the fabrication of MOSCAP devices. Annealing of ALD deposited HfSiO is carried out for 470°C for 30 seconds. Similarly, the atomic layer TiN ultrathin layers were also subjected to RTP with temperatures chosen for a variety of electrical characterization purposes in the range from 100°C to 1000°C for 20 seconds. The intentional short pulse of annealing time is important to see the effect of external energy efficient processing of these structures. Nitrogen gas ambience is utilized to anneal the samples at nominal atmospheric pressure. The electrical characterization of the devices was measured using a sophisticated Automatic System for Material Electrical Characterization (ASMEC) tool in the Advanced Electronics Laboratory. Electrical measurements (resistance, mobility, etc.) were also cross-checked by the Hall Effect system with an electrical currents of 0.1 μA and magnetic flux of 5300 G.

3. Results and Discussion

While performing the current density profiling (J-V), we have examined the behavior of TiN ultrathin film as a function of annealing temperature as shown in Figure 1. We have plotted current density "J" for various annealing temperatures and its maximum value is found in the tune of 10^{-4} A/cm^2, whereas applied voltage is varied from 0 to 2.5 volts. It is observed that the samples annealed at higher temperatures have lower values of current density as compared to their lower valued counterparts, when applied bias is increased steadily from 0 to 2.5 volts. The extent of profile (trend) remains the same for all the samples annealed at a variety of temperatures, whereas the magnitude varies with the varying temperature. For some distinct values of temperature, its behavior is almost the same; that is, the cases for 800°C and 1000°C annealed sample provided almost the same amount of energy to this device system with the carrier transport mechanism. The behavior shown in Figure 1 is not unusual. The J-V curves obtained at different annealing temperatures follow a systematic trend (profile) until they reach 900°C. The oxygen redistribution effect starts to occur at TiN/HfSiO interface at temperatures about and above 900°C, which is known to impact both the diffusion sites and trap states in the MOS structures. The oxygen atoms behave differently and tend to greatly impact the transport at relatively small intervals of thermal flux given to the device matrix. This, in turn, may disturb the in and out diffusion process that takes place in the device particularly at interfaces and towards the bulk and hence provides a sudden shift in the resistivity/conductivity behavior at a higher annealing temperature. Such behavior and trends in form of measurement profile for these structures are known and discussed in related studies [18–20].

Electrical measurements were performed to determine the resistance of the atomic layer deposited TiN thin films. The graphical analysis is shown in Figure 2, where resistance is plotted as a function of varying annealing temperatures from RT to 800°C. The best fit of the measured values provides a straight line with a negative slope. The orders of magnitude ($\geq 10^5$ to almost 10^7 Ω) are relatively higher but in total agreement with the work performed by Van Bui et al. [21] for such films deposited by the ALD technique in thickness ranging below 2.5 nm. A negative slope directly revealing a negative Temperature Coefficient of Resistance (TCR) and high resistivity values of this ultrathin TiN layer in this MOSCAP structure is linked with the metal-semimetal transition phenomena observed in TiN Atomic Layer Deposition experiments [22]. This indicates that the choice of deposition technique as well as thickness of TiN gate electrode, to make the CMOS fabrication process rather

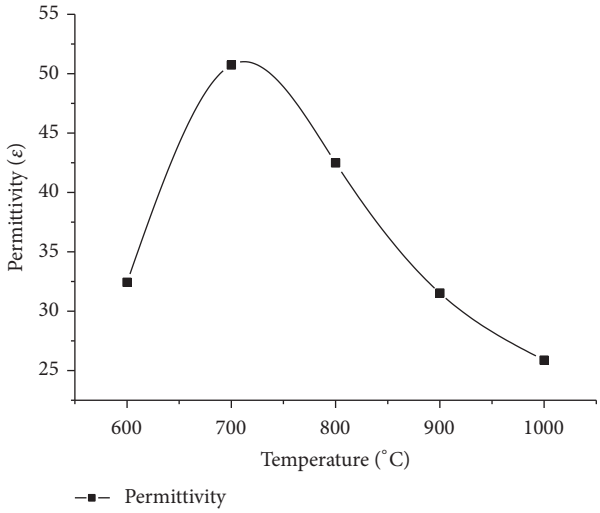

Figure 3: Evolution of permittivity with respect to annealing temperatures.

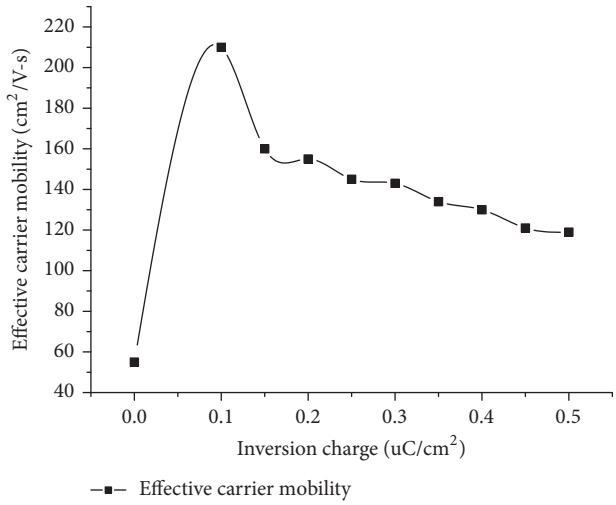

Figure 4: Effective carrier mobility versus inversion charge density.

energy efficient, is critical. The annealing characteristics for a large process window (starting from RT to 800°C) exhibited in Figure 1 explain the evolution of progressively stabilized atomic structure with the rising temperature in form of decreasing resistance (improved conduction properties of ultrathin layers duly undergone the deposition related distortion during the ALD process). In contrast to the usually expected values of resistance in the order of $<10^2\ \Omega$ for such devices, the phenomenal increase at relatively thin layer also suggests that the choice of layer thickness in our experiments is below the so-called threshold thickness for such TiN depositions. In such cases the impact of electron scattering by thermally activated lattice vibrations significantly changes [17, 22]. The behavior depicted in Figure 2 was observed in multiple samples undergoing the measurements suggesting it to be a reproducible one. The negative TCR (slope of the straight line in Figure 2) and higher resistivity values in our work indicate the presence of appreciable electric field effect in the devices (this may be due to this nonmetallic or predominantly semimetallic behavior) in these ultrathin films.

We also performed the mobility and permittivity analysis for a 1.5 nm TiN layer together with 2.9 nm HfSiO as gate-dielectric stack as a function of inverse charge density and annealing temperature, respectively. This is important to evaluate the energy efficiency of the process in terms of charge storage capacity in a certain space medium and carrier transport associated with it. The graphical representation is shown in Figures 3 and 4. Thermal flux corresponding to the temperature of 700°C seems most appropriate for the optimum permittivity values. Figure 3 also depicts the permittivity analysis after the device is processed. This analysis is drawn out of capacitance-voltage profiling at progressively increasing annealing temperatures. One can see that the charge storage/dielectric behavior is rather distorted at higher annealing temperatures (>700°C for instance), which eventually signifies the relative distortion in the crystallinity at such thermal flux compared to the lower annealing temperatures.

The effective mobility versus the inversion charge density is phenomenally important to forecast the device characteristics in charge (energy) efficient domain. Three distinctive regions can be identified in Figure 4 (effective mobility scan) for this dielectric-gate stack arrangement measured at room temperature. A sufficiently fair number of carriers available at rather low vertical fields (low inversion charge density) provide an insight into the energy efficiency of process despite the Coulomb scattering phenomenon usually responsible for limited mobility. This may be due to the out-diffusion of the oxides towards the tail of the dielectric profile from the TiN/HfSiO interface region.

One may also signify the traces of important role of possible phonon scattering at a rather higher inversion density before the usual surface phenomenon gains momentum and limits the mobility to a relatively degraded value. The process, however, in totality exhibits appreciable effective mobility and permittivity of the MOSCAP structure even at low vertical fields (inversion charge density) or high values of annealing temperatures (such as >600°C), respectively, proposing the presence of an energy efficient device design with a critically thin TiN metal gate.

4. Conclusion

The work presented here deals with the formation of ultrathin TiN metal gate in combination with HfSiO dielectric, integrated into a Si MOSCAP structure, where Atomic Layer Deposition technique was fully utilized to process the device structure. Relatively short-time postdeposition and post-metal annealing was employed to provide a variable thermal flux to critically thin TiN metal gate where a state transition is envisaged. Electrical characterization of the system revealed the formation of such thin layers of TiN metal gate which are in the region where the state transition is evident with a full scan of annealing cycles from 100°C to 800°C. Analysis in this

extended range was presented for the first time to evaluate the process characteristics in terms of energy efficiency. Charge storage and impact of low vertical fields on the effective carrier mobility were also presented to determine the utility of such device designs in sub-10 nm CMOS manufacturing with process proficiency and energy efficiency schemes.

Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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