A novel additive-assisted acidic etching method is proposed to improve the etched morphology of the diamond wire sawn (DWS)-processed multicrystalline silicon (mc-Si) wafers. The proposed etching technique is a cost-effective method for surface texturization of DWS-processed mc-Si wafers, which can be used for large-scale production of Si-based solar cells. Moreover, the mechanism of additive-assisted etching is explained by decoupling the roles of surfactants and etching inhibitors. The additive-assisted etching of DWS-processed mc-Si wafers resulted in different morphology to the slurry wire sawn (SWS)-processed mc-Si wafers under optimized etching conditions. It has been observed that the etched morphology and reflectivity of DWS-processed mc-Si wafers are significantly influenced by the ratio of hydrofluoric acid (HF): nitric acid (HNO₃) solution. High-quality etching morphologies have been obtained. Therefore, high-power conversion efficiency of 19.0% and open-circuit voltage (Voc) of 0.6386 V have been demonstrated by additive-textured DWS-processed Si-based solar cells. The improved power conversion efficiency and Voc can be ascribed to the reduced defect area of the wafer surface. In summary, the proposed additive-assisted acidic etching is an effective strategy to obtain the desired surface texturization of DWS-processed Si wafers for high-performance solar cell applications.

1. Introduction

Surface texturization of silicon wafers is a critical process step for the production of mc-Si-based solar cells. It can reduce the light reflection of the front surface and remove the damaged layers of the wafers, which improves the power conversion efficiency of the solar cells. During large-scale production of Si-based solar cells, the hydrofluoric acid (HF): nitric acid (HNO₃): H₂O mixed-acidic etching is widely utilized for surface texturization of the mc-Si wafers due to its excellent performance and cost-effectiveness [1]. The surface of the as-received mc-Si wafer significantly influences the textured morphology of the etched mc-Si wafer [2]. Apart from the influence of the cutting method, the surface of the as-received wafer also influences the evolution of the resulting morphology. During the past few years, instead of the conventional SWS method, the cutting of mc-Si wafer is carried out by using the DWS process due to its distinct advantages, such as lower wafer cost and higher yield productivity [3]. Despite the lack of a compatible surface texturization process, multicrystalline silicon (mc-Si) wafers have to use the DWS method due to the high cost of the SWS process [4]. One should note that the surface of the DWS-processed mc-Si wafer is significantly different from the SWS-processed mc-Si wafer surface in terms of the different cutting methods [5]. In SWS, free-SiC particles are driven by a high-speed moving wire saw to grind and cut silicon ingots [6]. As a result, the wafer surface exhibits brittle fracture with a large number of irregular pits and homogeneously distributed defects. On the other hand, the diamond wire is directly used to cut silicon ingots in the DWS process, which results in few irregular cracks and pits in the vicinity of the fractured region. Moreover, the remaining area of the wafer exhibits a smooth surface with
parallel grooves due to the plastic deformation [7–9]. In the case of DWS mc-Si, the smooth regions, without surface defect, resist the etching, whereas the defective regions are excessively etched [10–12]. Therefore, the DWS mc-Si wafer cannot be effectively textured by using conventional mixed-acidic etching. In general, the average light reflectivity of the DWS mc-Si wafer in the visible light range is 3–5% higher than the SWS mc-Si wafer after the conventional HF: HNO$_3$: H$_2$O solution acid-texturization process [13, 14].

Even though the reactive ion etching (RIE) and metal-assistant chemical etching (MACE) methods can effectively solve, the large-scale utilization and industrial acceptance are hindered by the high cost and complicated processing [15–18]. Therefore, cost-effective and high-performance texturization techniques need to be developed for the mass production of DWS mc-Si-based solar cells.

Herein, a novel and cost-effective method for the surface texturization of the DWS mc-Si wafer is proposed by using an additive-enhanced conventional HF: HNO$_3$: H$_2$O solution acid-texturization process. The surfactants and etching inhibitors were introduced to improve the etched morphology. The microstructural evolution during the additive-assisted acid-texturization of DWS wafers was investigated in detail. For reference, the surface morphology of the SWS wafer using the conventional acid-texturization process was also analyzed, and all the textured wafers were fabricated into solar cells under the same processes for parallel investigation. Finally, we characterized the reflectivity, current-voltage (I–V), and quantum efficiency (QE) of the solar cells that are related to the texturing. The proposed method rendered desired surface texture which ascribed to the less defective area, and the resulting DWS mc-Si-based solar cells demonstrated excellent performance.

2. Experimental

In the present study, the DWS p-type mc-Si wafers, with a thickness of ∼190 µm and an area of 157 × 157 mm$^2$, were processed. SWS mc-Si wafers were also analyzed to compare the influence of the proposed surface texturization method. One group of SWS mc-Si wafers and three groups of DWS mc-Si wafers from the same batch were prepared. Each group consists of 1000 pieces of wafers, which were provided by GCL New Energy Co., Ltd. For comparison, four groups of the wafer were all fabricated into solar cells according to the convention production process and analyzed in parallel. The experimental procedure for this study, including the whole process flow of solar cells, was outlined as follows: texturing → phosphorous doping → edge etching and PSG (phosphosilicate glass) removal → SiN$_x$ deposition (by PECVD, plasma-enhanced chemical vapor deposition) → screen printing silver and aluminum paste → cofiring → electrical characterization.

During the etching experiment, the wafers were textured by the Inline Texture Etching Machine (InTex, RENA Corporation, Germany) in the etching solution of HF (49 wt. %)/HNO$_3$ (65 wt. %)/H$_2$O. The etching process was carried out for 90 sec at 8°C. The surfactant is a mixture solution of polyvinyl alcohol, alkyl amine salt, sodium dodecyl benzene sulfonate, and deionized water.

The scanning electron microscope (SEM, JSM-6510, JEOL) was utilized to characterize the etched morphologies. The average reflectivity, in the wavelength range of 350–1050 nm, was used to represent the light reflectivity of the acid-texturized wafers by a spectrometer (D8, radiation technology). The internal quantum efficiency (IQE) and external quantum efficiency (EQE) of the as-prepared mc-Si-based solar cells were tested on a QEX7 system by PV Measurements Inc. The power conversion efficiency of the cells was tested by an online I–V measurement system (HALM, Germany) by using the standard TUV Rheinland reference cell.

The cell (246.49 cm$^2$) performance was measured at the irradiance of 1000 W/m$^2$ and an operating temperature of 25°C.

3. Results and Discussion

3.1. Influence of Additive-Free Etching. The SEM images of the SWS- and DWS-processed wafers reveal the influence of both cutting processes on the as-cut microstructure (Figure 1). SWS-processed wafers exhibited a random and rough fractured surface with homogeneously distributed defects and cracks. On the other hand, a smooth surface, with parallel grooves and fewer cracks, has been observed in DWS-processed wafers, which is an undesirable texture. The smooth regions of the DWS-processed wafer might be responsible for the high reflectivity values. One should note that DWS-processed wafers exhibited 1/3 times lower depth of the damaged layers than SWS-processed wafers [1, 8].

The microstructure of the as-received wafer surface has a significant impact on etched texture, which is generated by using the conventional acid-texturization process. Figures 2(a) and 2(b) present the etched morphology of SWS- and DWS-processed wafer after conventional additive-free acidic solution etching, respectively. The acidic solution consists of HF, HNO$_3$, and H$_2$O in a volumetric ratio of 1 : 5.1 : 2.6. The SWS-processed Si wafers were etched by using conventional acidic etching and obtained a large number of earthworm-like corrosion pits. In DWS-processed wafers, the smooth and defect-free regions resisted the etching process, whereas the defect-containing regions experienced excessive etching. When the surface is exposed to chemical attack, the smooth regions of DWS-processed wafers exhibited a small increase in the folded surface, whereas the reflectivity is not influenced by varying the composition of the etching solution. On the contrary, the defective regions experienced an aggressive attack like grain boundaries, dislocations, and defects due to the low activation energy, originating from the disordered atom packing. This has been exhibited in the relatively darker region in Figure 2(b). Moreover, the poor wafer surface renders inferior semiconducting properties and light trapping, whereas the recombination of electron-hole pairs is increased due to the poor surface. In general, the conventional texture process can reduce the reflectivity of SWS- and DWS-processed mc-Si wafers by ∼23% and ∼28%,
respectively. One should note that the higher reflectivity of the DWS-processed mc-Si wafer results in a serious power conversion efficiency loss of 0.4% [13].

Etching in the photovoltaic (PV) industry is performed in the so-called “feed-and-bleed” regime [14, 19]. The electrochemical reactions at the silicon surface can be described as

\[
2\text{NO}_2 \rightarrow 2\text{NO}_2^- + 2\text{h}^+ \quad (1)
\]

\[
\text{Si}^0 + 2\text{h}^+ \rightarrow \text{Si}^{2+} \quad (2)
\]

\[
\text{Si}^{2+} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2 \rightarrow \text{SiO}_2 + \text{H}_2\text{O} \quad (3)
\]

\[
\text{SiO}_2 + 6\text{HF} \rightarrow \text{H}_2\text{SiF}_6 + 2\text{H}_2\text{O} \quad (4)
\]

HNO₃ and HF are continuously dosed in the etch bath, which implies the consumed etching solution mainly consists of HNO₃ and HF. Moreover, the hexafluorosilicic acid (H₂SiF₆) is continuously removed from the etch bath as a byproduct. In order to obtain a high-quality texturization of DWS-processed Si wafers, an additive can be introduced to balance the “feed-and-bleed” process during etching.

3.2. Influence of Additive-Assisted Surface Texturization. The smooth surface of the DWS-processed mc-Si wafer, with fewer defects, is more hydrophobic than the SWS-processed mc-Si wafer surface. Hence, the etching solution cannot effectively attack the wafer surface due to poor contact [20]. Therefore, a variety of surfactants, with different functions, have been used as additives to enhance the etching kinetics. In addition, some hydrophilic groups, with an excellent affinity towards water, were added to increase the viscosity of the etching solution. In general, the presence of additives reduces the solid-liquid surface tension and enhances the spreading of the etching solution on the wafer surface [21]. Once the wettability is improved, etching inhibitors are required to adsorb on the wafer surface and reduce the etching rate by controlling the supply of NO₂⁻. Moreover, the foam stabilizer results in finer pores and stays on the wafer surface, which results in uniform and slower etching. Furthermore, the nucleating agents and dispersants contribute to nucleate and uniformly disperse various components of the chemicals on the wafer surface, enhancing the rate of texturization yield [22]. Figure 3 schematically illustrates the working process of the additive on the wafer surface, which consists of three key steps. Firstly, the additive improves the wettability of the silicon wafer. Secondly, the etching inhibitors and pores adsorb on the wafer surface and act as a template for uniform and slower etching. Thirdly, the nucleating agents reach and interact with the wafer surface through the hydrophilic groups. Therefore, the hydrophilic groups and wafer surfaces should have enough contact time to obtain uniform etching.
3.3. Surface Morphology and Reflectivity after Additive-Assisted Acidic Etching. Furthermore, the morphology and reflectivity of DWS-processed Si wafer after etching with additive-containing HF: HNO₃ solution were studied, as shown in Figures 4 and 5, respectively. Three different recipes of HF: HNO₃ solutions were used for additive-assisted acidic etching, as shown in Table 1. As the damage layer of the DWS-processed Si wafer is much shallower than the SWS-processed Si wafer, the DWS-processed Si wafer exhibited a lower amount of removed mass (0.25–0.28 g) than the SWS-processed Si wafer (0.35–0.38 g).

Figure 4 presents the morphology of the DWS-processed Si wafer after etching with different recipes, as given in Table 1. After etching with recipe-I, a small area has exhibited long and deep etching pits, whereas most of the regions remained unaffected and only shallow pits have been observed. In general, the etched surface is smooth, and a compact textured structure has not been formed, which resulted in high reflectivity. After etching with recipe-II, closely arranged circular pits are generated, whereas the longer and deeper pits have not been observed, implying that the defective regions did not experience excessive etching. In addition, the inhibitors and pores decreased the etching rate, and the etching process continued slowly and led to slightly decreased reflectivity of the etched wafer. Furthermore, the recipe-III resulted in a large number of smaller-sized circular pits. One should note that the as-obtained morphology is
highly desirable for template generation on wafer surface (Figure 3).

The textured wafer samples, respectively, the DWS-processed Si wafers were etched by using recipe-I, recipe-II, and recipe-III, and the SWS-processed Si wafer was etched by using conventional acidic etching, were compared with the light reflectivity versus wavelength curves in the wavelength range of 350–1050 nm, as shown in Figure 5. The weighted average reflectance (Ra) for the recipe-III-textured DWS-processed wafer was 23.92%, which was 1.63% and 3.32% lower than 25.55% and 27.24% of the recipe-II and recipe-I-textured DWS-processed wafers, respectively, but 0.82% slightly higher than 23.10% of the conventional acidic-textured SWS-processed wafer. The conventional acidic textured wafers had the lowest reflectivity, owing to these a large number of earthworms like corrosion pits increase the refraction times of light on the surface and have the opportunity to make more reflected light return to the wafer. It was clear that with the decrease in HF:HNO₃ volume ratio, the light-trapping effect on the surface of the DWS-processed Si wafer was strengthened.

### Table 1: Different recipes of HF:HNO₃ etching solution (volume ratio).

<table>
<thead>
<tr>
<th>Acid name</th>
<th>Recipe-I</th>
<th>Recipe-II</th>
<th>Recipe-III</th>
</tr>
</thead>
<tbody>
<tr>
<td>HF</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>HNO₃</td>
<td>5.1</td>
<td>4.2</td>
<td>3.1</td>
</tr>
</tbody>
</table>

3.4. Solar Cell Performance. Four groups of textured wafer samples, respectively, the DWS-processed Si wafers were etched by using recipe-I, II, and III, and the SWS-processed Si wafers were etched by using conventional acidic etching, were fabricated into solar cells according to the standard production process. The quantum efficiency (EQE/IQE) of these cells was compared as shown in Figure 6, and the weighted average EQE/IQE values in the wavelength range of 300–1000 nm were marked.

It was clear that the different surface structures had an obvious impact on the QE value. The weighted average EQE of the recipe-III DWS-processed cells with 78.09% was higher than 76.34% and 73.68% of the recipe-II, I DWS-processed cells, respectively, but was lower than 79.91% of the SWS-processed cells in the wavelength range of 300–1000 nm, as shown in Figure 6(a). This result was consistent with the light reflectivity curves of the four groups’ textured wafers in Figure 5, that is, the lower the surface light reflectivity, the better the light-trapping effect, and the higher the probability of photons absorption, leading to the higher cell EQE value. The weighted average IQE value of the recipe-III DWS-processed cells was 92.01%, lower than 93.32% and 94.61% of the recipe-II, recipe-I DWS-processed cells, respectively, but higher than 90.05% of the SWS-processed cells in the wavelength range of 300–1000 nm, as shown in Figure 6(b). Compared to the SWS-processed cells, the surface of the recipe-III DWS-processed cells with smaller-sized circular pits was beneficial to improve the coverage and contact between the SiNx layer and silicon substrate during the PECVD process, which may result in a decreased lower surface defect rate and improved the passivation performance. The SWS-processed cells with a large number of Earth worm-like deep pits had the higher ratio of surface defects, which always resulted in IQE deterioration due to carrier recombination. The recipe-I, II DWS-processed cells with a smoother surface caused superior IQE. That indicated that the smaller-sized circular pits were beneficial to reduce the residual microdefects in the etch-pits, thereby, to improve the collection rate of charge carriers.

Figure 7 presents the distribution of different types of solar cells’ electrical performance parameters, including the open-circuit voltage (Voc, V), the short-circuit current (Isc, A), the fill factor in percent (FF, %), and the power conversion efficiency (Effi = Voc × Isc × FF/(P × S)%) were listed and compared. The Isc data of the four groups of solar cells were highly consistent with the reflectivity comparison in Figure 5 and the EQE comparison in Figure 6(a). Obviously, the Isc data were directly related to the reflectivity, lower reflectivity means more light will enter the solar cells, and more light has the opportunity to produce the photoelectric effect and made a contribution to the higher Isc. The Isc of the recipe-III DWS-processed cells was slightly lower than that of the SWS-processed cells. The Voc value of the recipe-III DWS-processed cells was higher than that of the SWS-processed cells, which was correspond well with the IQE comparison in Figure 6(b), and it also shows that the surface with smaller-sized circular pits as shown in Figure 4(c) was beneficial to improve the coverage and contact between the SiNx layer and silicon substrate which may result in a decreased lower surface defect rate and improved the passivation performance. Theoretically, the higher Voc renders enhanced Effi with a superior temperature coefficient, which improves the module output power under high-temperature operation [23]. These solar cells fabricated with SWS and recipe-III exhibited higher FF values than that of the other two kinds of ones. The comparison of three different recipes reveals that the recipe-I additive-textured DWS-processed cells exhibited the lowest Voc and Isc, and recipe-II demonstrated higher Voc and Isc than recipe-I, but the performance was still inferior to the recipe-III additive-textured DWS-processed cells. The Effi of recipe-III solar cells was slightly higher 0.01% than SWS solar cells and higher 0.22% and 0.33% than recipe-II and recipe-I solar cells, respectively. We got the maximum efficiency cell (19.23%) in the recipe-III solar cells, and it was owning excellent Voc (0.6412, V) performance. The results indicated that the recipe-III texturing process worked well in industrial production, and we have the opportunity to further improve the efficiency by optimizing the process.
**Figure 6**: The EQE/IQE of the solar cells by the different texturing processes. (a) The EQE of the solar cells by the different texturing processes. (b) The IQE of the solar cells by the different texturing processes.

**Figure 7**: Electrical performance parameters of the solar cells with different texturing processes.
4. Conclusions

In summary, we have developed an additive-assisted acidic etching technique to obtain the desired surface texture of DWS-processed Si wafers. For the DWS-processed Si wafers, the smooth regions, without surface defect, resist the etching, whereas the defective regions are excessively etched. The surfactants with different functions have been used as additives to enhance the etching kinetics to improve the etched morphology. As a result, high-quality etching morphologies have been obtained, which are different from the SWS-processed Si wafers. Moreover, the high-power conversion efficiency of 19.0% and open-circuit voltage (Voc) of 0.6386 V have been demonstrated by additive-textured DWS-processed Si-based solar cells. These results reveal that the proposed etching technique is a cost-effective process to obtain the required surface texturization of the DWS-processed mc-Si wafer, which can be used for large-scale production of solar cells.

We got the maximum efficiency cell (19.23%) in the group of recipe-III solar cells, and it was owning excellent Voc (0.6412, V) performance. The results indicated that we have the opportunity to further improve efficiency by optimizing the process. The next step is to adjust the proportion and composition of additives to improve the etched morphology, in order to get a lower reflectivity surface.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no known conflicts of interest or personal relationships that could have appeared to influence the work reported in this paper.

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