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Review Article

Quantum-Dot Cellular Automata-Based Full Adder Design: Comprehensive Review and Performance Comparison

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Being one of the promising techniques for future computing systems, quantum-dot cellular automata (QCA)-based circuit design has gained massive interest among researchers due to which numerous QCA-based full adder (FA) circuits have been designed. Due to numerous QCA FA circuits available in the existing literature, researchers find it difficult to invest the time to search, implement, simulate, and analyze QCA FAs to find the best-suited design according to their needs. Existing review articles do not present a complete overview and performance comparison of QCA FAs. Also, the existing articles do not include quite a number of QCA FA designs in the literature review. As a result, a detailed review including all possible QCA FAs becomes essential. Therefore, rather than going for a new QCA FA design, this research aims to aid researchers by providing an extensive literature review and comprehensive study on existing QCA FAs. A total of 47 QCA FAs have been considered for analysis. The QCA FA implementation method and performance parameters are summarized in a tabular manner to provide a quick overview and comparison of the QCA FAs.

1. Introduction

Due to short-channel effects, quantum effects [1], and power consumption, scaling down in the microscopic world is truly a challenging approach. Traditional CMOS and FinFET processes have their limits due to which they are unable to go deeper into the deep submicron level after a certain point is reached [2–4]. Therefore, researchers are seeking alternative robust solutions. Among all the latest emerging technologies, the quantum-dot cellular automata (QCA) is representing itself as the future of nanotechnology by surpassing and removing the barriers associated with the conventional transistor fabrication process [5–7].

QCA is a nanoscale level evaluating method that makes use of electron tunneling to represent binary information [8, 9]. It proposes a new perspective on data transmission, in which data are transmitted through polarization transmission between QCA cells. The most remarkable advantage of QCA devices is the easiest association between cells, with only adjacent cells obtaining a correlation [10]. As a consequence, the full connection is not essential [11, 12].

As QCA is among the potential candidates for upcoming computing systems, researchers are focusing on circuit design methods to represent binary data [13, 14]. The Arithmetic Logic Unit (ALU) is an essential part of modern microprocessors [15]. Therefore, a major focus has been given to QCA-based ALU component design [16]. In ALU design, addition is a fundamental operation [17, 18]. In binary addition, full adder (1-bit adder) is considered the basic unit cell [19, 20]. Moreover, wide word length adders are mainly implemented based on a 1-bit FA cell [21, 22]. In addition, different arithmetic functions need addition in their internal nodes. For these reasons, a major focus has been given to develop efficient FA cells in QCA [23–25].

Being one of the most frequently used blocks in ALU, numerous QCA FA circuits have been developed over the course of time. However, as more designs come in, it often becomes quite difficult and time-consuming task for circuit designers to search for QCA FA designs from existing literature. Also, it takes a lot of time for circuit designers and researchers to build, analyze, and simulate every circuit to determine the optimal QCA FA circuit based on their design constraints and requirements. Existing review papers only contain a handful number of circuits [25–27]. Also, they fail to provide a comprehensive performance comparison of QCA FAs based on various metrics. Moreover, existing review papers have not used all the important performance parameters of a QCA circuit to evaluate and compare QCA FAs. Therefore, a comprehensive study and performance comparison of existing QCA FAs is necessary to aid QCA circuit designers and researchers in selecting the suitable cell as per the system requirement. Moreover, it will reduce the time that researchers spend to find and simulate QCA FA cells to select their suitable designs. This research aims to fill up the research gaps of existing review papers by providing a comprehensive literature review and performance comparison of a wide number of QCA FA designs.

In this research, a comprehensive study on QCA FA cells has been conducted. All QCA FA cells are implemented and simulated using the QCA Designer software. Based on the simulated results, a summary table highlighting performance parameters of QCA FA cells has been provided which will aid QCA circuit designers and researchers.

2. QCA Overview

The QCA technology was firstly introduced in 1993 [24]. QCA circuits consist of an array of QCA cells. Each of the QCA cells contains nanoparticles or crystalline quantum dots. Basic information on QCA is provided in the following subsections.

2.1. Basic QCA Cell. As demonstrated in Figure 1(a), a QCA cell is like a square-shaped box that contains four quantum dots stationed at four individual corners [13]. Two electrons are present in each cell. Because of Coulombic interaction, the electrons of a cell are positioned diametrically into two opposite quantum dots (also called antipodal dots). As a result, electrons can occupy the quantum dots P_1 and P_3 or P_2 and P_4. Tunnel junctions link the dots through which the electrons can change their diagonal positions. Based on the position of charges (electrons), two distinct conditions or states are possible. In Figure 1(a), the state where electron pairs occupy quantum dots P_2 and P_4 is known as positive polarization (polarization = 1). This positive polarization state represents binary 1. On the other hand, the state where electron pairs occupying quantum dots P_1 and P_3 is known as negative polarization (polarization = −1). This negative polarization state represents binary 0. The QCA cells utilized in this research have length = 18 nm, width = 18 nm and dot diameter = 5 nm.

Based on the orientation of the quantum dots, QCA cells can be two types: 90° cells and 45° cells (Figure 2). The

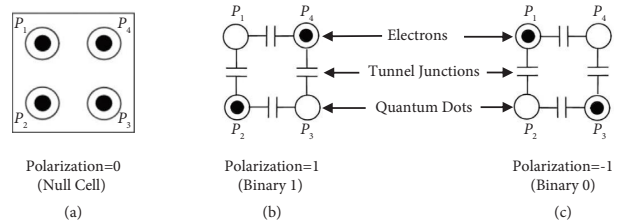

Figure 1: Basic QCA cells. (a) Null cell. (b) QCA cell with polarization = 1. (c) QCA cell with polarization = 0.

number of quantum dots and electrons is the same in both cells. The main difference is in the orientation of the quantum dots. Polarizations and their respective binary equivalent states of 90° cells, and 45° cells are shown by using Figure 2.

2.2. QCA Wire and Data Transmission. To transmit data in QCA configurations, an interconnection architecture among elements must exist. As per the orientation of the QCA cell, QCA wire or interconnect can be divided into two groups: 90° wire and 45° wire (Figure 3). From Figure 3(a), it can be perceived that the input provided is a binary 1 logic [13]. Coulombic repulsion force among the electrons in the input cell and the cell adjacent to the input cell enables the electrons to get arranged diagonally so that maximum distance can be maintained between two electrons in two adjacent cells. Since the binary state of the output cell is equivalent to the binary state of the input cell, it can be said that the QCA wire in Figure 3(a) is passing binary logic 1 from input to output. Exactly, in the same manner, binary logic 0 is passed in the QCA wire shown by Figure 2(b). Here, Figures 3(a) and 3(b) represent 90° wire. Now, in Figure 3(c), binary logic 1 is provided in the input cell. To maintain diagonal distance due to Coulombic repulsion, the electrons in the adjacent cell get arranged in the opposite manner to the input cell. In this way, data gets transmitted through a 45° wire. It can be observed from the output cell in Figure 3(c) that the electron pair position is exactly the same as the input cell. Therefore, the 45° wire in Figure 3(c) is passing binary logic 1. Using the same methodology, 45° wire in Figure 3(d) is passing binary logic 0.

As per wire crossing, QCA wire can be classified into two groups: single layer crossing and multilayer crossing [26]. Single-layer and multilayer QCA wire crossings are presented in Figure 4. As perceived from Figure 4(a), a single layer QCA wire crossover is realized using both 90° and 45° wires. On the other hand, a multilayer QCA wire crossing requires at least 3 layers of QCA cells to transmit data without interacting with the wire below it. In this type of wire crossing, a layer is added above or below another. This sort of wire crossing is quite identical to the conventional interconnect system in the CMOS process, where several metal layers are being used. In the case of two parallel wires/lines containing different signals, the spacing of one QCA cell is required [25, 27]. Therefore, the distance between two QCA wires/lines is equivalent to the length/width of a QCA cell (18 nm).

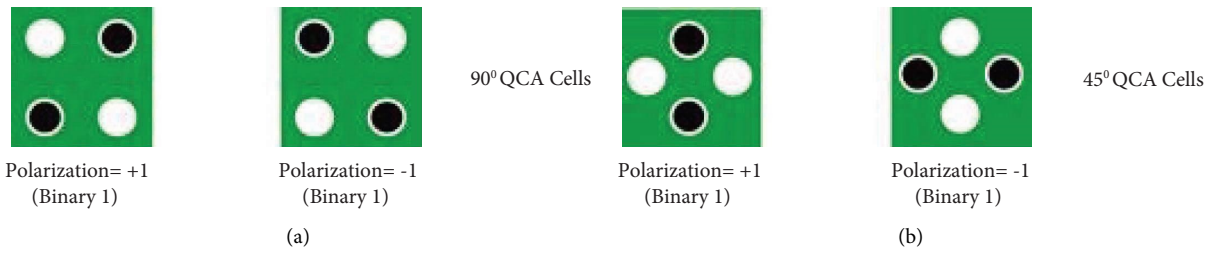

Figure 2: Basic QCA cells. (a) Null cell. (b) QCA cell with polarization = 1.

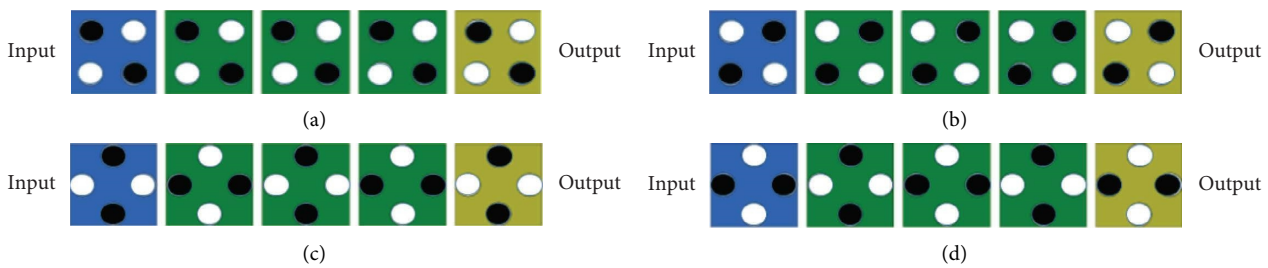

Figure 3: QCA wire. (a) Binary 1 logic transmission in 90° wire. (b) Binary 0 logic transmission in 90° wire. (c) Binary 1 logic transmission in 45° wire. (d) Binary 0 logic transmission in 45° wire.

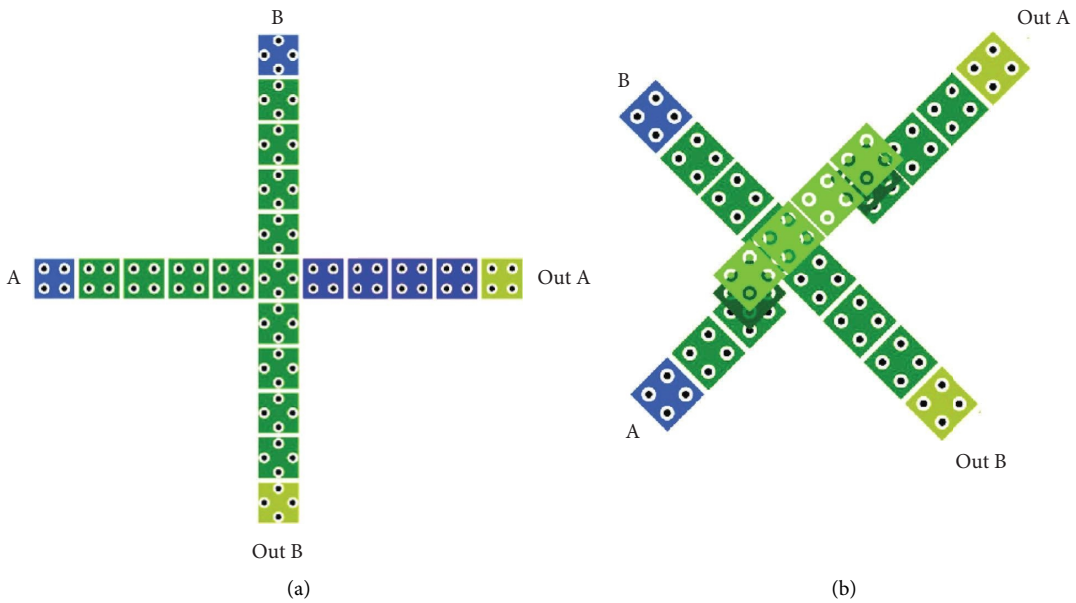

Figure 4: QCA wire crossings: (a) single layer QCA wire crossing and (b) multilayer QCA wire crossing.

2.3. QCA Logic Gates. To complete several computational instructions, QCA logic circuits are required. In the CMOS logic circuit, NOT, NAND, NOR, AND, OR, XOR, and XNOR are the major functions [11–13]. In the case of QCA logic design, majority gate, and inverter act as the basic logic function. A majority function provides logic 1 if more than half of the input signals are logic 1. For a 3-input majority gate, the logic function can be expressed as follows [21]:

$$M(A, B, C) = AB + BC + CA. \quad (1)$$

Schematic of two majority gates (3-input and 5-input) are shown in Figures 5(a) and 5(b). The design of a 2-input AND gate can be done by utilizing a 3-input Majority Gate. If a logic 0 is provided to any of the inputs of a 3-input majority gate, then it behaves like an AND function. Conversely, implementation of a 2-input OR function using a 3-input majority gate can be done by providing logic 1 in any of the inputs. In FA, the output carry circuit signal can be easily generated by using a 3-input majority gate. Two types of inverter circuits are possible in QCA logic design which is shown in Figures 5(c) and 5(d).

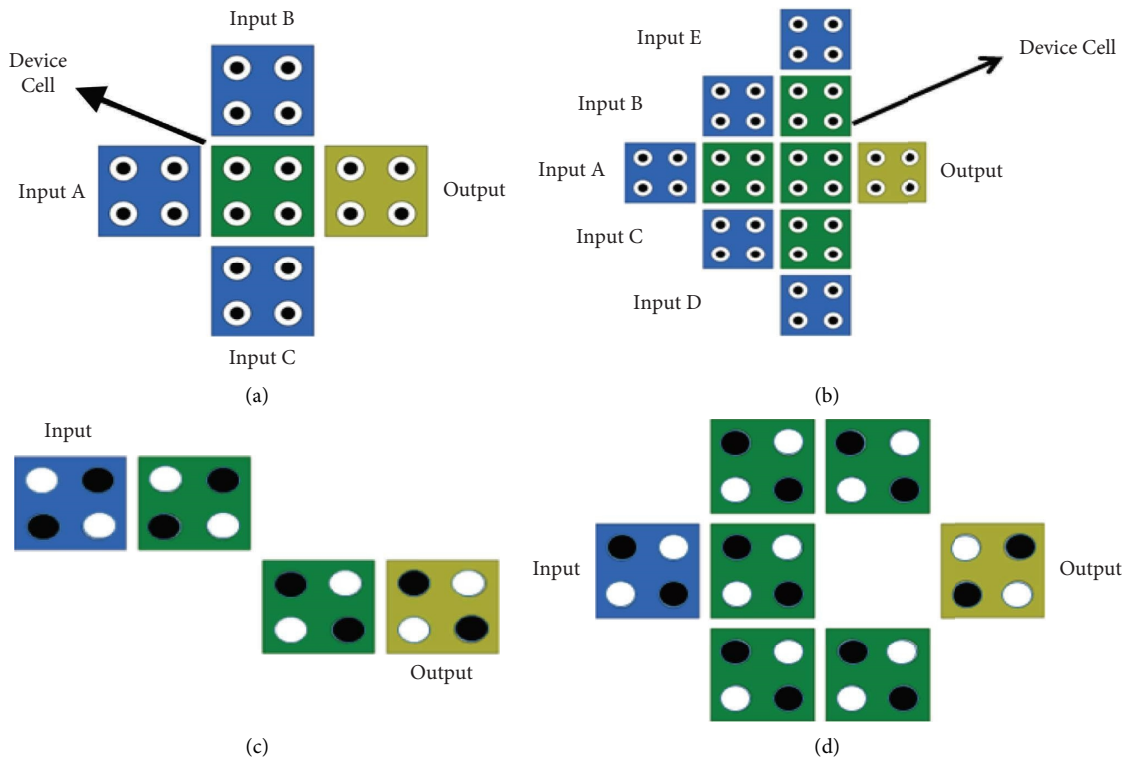

Figure 5: QCA logic circuits; (a) 3-input majority gate; (b) 5-input majority gate; (c) inverter circuit design 1; (d) inverter circuit design 2.

2.4. QCA Clocking. QCA circuits require clock pulses to operate. The clocking scheme of a QCA technology can be understood using Figure 6. QCA clocking is divided into four phases: switch, hold, release, and relax [13]. The switch process begins with unpolarized QCA cells having low potential barriers. However, the barriers get higher as the phase progresses. In the hold phase, the barriers are kept high. But in the release phase, the barriers are reduced. In the relax step (final step), the barriers are kept lowered which allows the cells to remain unpolarized. That inter-dot barrier inside a clocking zone and the activity of a QCA wire in separate clock zones are shown in Figure 6. A crucial distinction between QCA circuit architecture and traditional CMOS technology is that, unlike CMOS, QCA circuits have no control over the clocks [28]. As a result, information is only passed through each cell and therefore not stored. In every clock cycle, each cell erases its state.

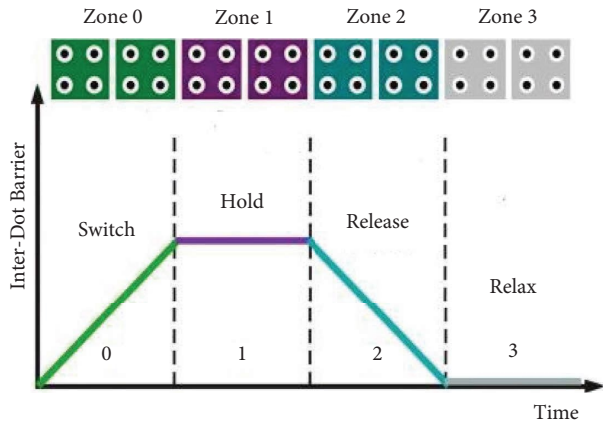

Figure 6: QCA clocking phases.

3. QCA-Based Full Adder (FA)

A literature review on QCA FAs and the general logic design aspects are presented in the following subsections.

3.1. Literature Review. A QCA-based FA is the fundamental unit to design a multibit adder. Therefore, numerous QCA full adders have been designed. Some of the full adders have low complexity, and some of them have high. Some of them require more or less time for the generation of output.

The QCA-based architectures can be divided into two major types: coplanar (single layer) and multilayer. Coplanar designs have only one layer, whereas multilayer designs can have three or more layers. The first QCA FA was presented by Tougaw and Lent [29]. They have used three inverters and five three-input majority logic gates. The designed FA was coplanar-type. However, this design is incompatible with implementing larger circuits. With three inverters and five 3-input majority gates, another coplanar FA design is proposed in [30]. With the implementation of five majority gates and six inverter gates, a QCA FA is designed in [31]. New architectures of QCA-based FAs are shown in [32–39]. These QCA FAs are coplanar-type designs. With the help of only three majority gates, another QCA FA is implemented in [40]. No inverter gate is used in this design [40]. By using one inverter and two majority function gates, two QCA FAs

are shown in [41, 42]. With one 5-input majority gate, two 3-input majority gates, and two inverters, another coplanar type FA is shown in [43].

A new design of FA using QCA reversible logics is implemented in [28]. Another schematic of QCA FA is shown in [44]. More designs are demonstrated in [45–47], where one XOR gate and one majority gate are used. By using only two XOR gates, another schematic of FA is presented in [48]. Another coplanar type FA with an inverter and a three-input majority gate is shown in [49]. Another new two FA schematic was presented in [50–52]. This coplanar type full adder was designed with a five-input majority gate, two inverters, and a three-input majority gate. By using reversible logic, another schematic of FA is presented in [52]. One inverter and three majority gates are used in this design. With one three input majority gate, one five-input majority gate, and one inverter, another coplanar type QCA full adder is presented in [53].

With the use of three majority gates and two inverter gates, multilayer crossover types QCA FAs are proposed [54, 55]. These designs have three layers. With three majority gates and two inverter gates, three more multilayer QCA FA are implemented in [56–58]. Further, with the help of three majority gates and one inverter circuit, three multilayer QCA FAs are designed in [59–61]. A new design for decreasing the delay with the combination of three 3-input majority gates is implemented in [62] without using any inverter gate.

In [63, 64], highly area-efficient multilayer crossover-type QCA FAs have been proposed. These designs utilized 3-input and 5-input majority function gates. A FA with the combination of a 3-input majority gate, inverter, and 5-input majority gate is proposed in [65]. This full adder is a multilayer-type design (three layers). Three more schematics of multilayer QCA FAs are presented in [66–68]. These schematics have been designed with a three-input majority gate, an inverter circuit, and a five-input majority gate. These multilayer designs do not incorporate more than three layers. Two QCA FAs are presented in [69, 70] which are implemented using one 5-input majority gate, one 3-input majority gate, and two inverter gates. The QCA FA presented [71] is implemented with only one 3-input majority gate and one XOR gate. With the combination of one conventional three input majority gate, one five-input majority gate, and one inverter, another multilayer type full adder is presented in [72].

3.2. General Logic Design Aspects of QCA FA. Truth table of a QCA FA is exactly the same as a CMOS-based FA. Also, unlike CMOS-based FA, there are three input bits and two output bits in QCA FA. Among the three input bits, two are addend bits, and the remaining one is the input carry bit. On the output side, sum and carry-out are the output bits.

As per the analysis conducted in Section 3.1, it can be observed that majority gate and inverter are the major components in the QCA FA design. As stated in [21], the carry-output bit of a 1-bit FA follows the logic characteristics of a 3-input Majority Gate. Hence, for the QCA FA design, the carry-out bit can be implemented with a single 3-input majority gate. Due to this reason, majority gate plays a major role in designing the QCA FA. Now, different implementation methods of majority gates result in different cell count and layout area. For example, in general, a coplanar type majority gate requires more area than a multilayer majority gate. Moreover, multiple designs of majority gate are possible due to which the QCA FAs have different levels of complexity. As a result, being a major part of QCA FA design, the number of majority gates used and their design method play a major role in the complexity of QCA FA.

4. Design and Performance Comparison Parameters of the QCA Full Adder

The main performance parameters for the QCA FA comparison are discussed in the following subsections. The parameters listed below are the key attributes of a QCA circuit due to which existing papers have extensively used these parameters to compare QCA FAs. Thus, this research compares the QCA FAs based on the same parameters, which are extensively used by researchers in existing papers for QCA circuit comparison.

4.1. Complexity. In QCA design, the complexity is measured by the number of cells required for implementing a circuit. There is a proportional relationship between the complexity and the cell of the circuit. If the complexity of the circuit increases, the cell numbers also increase.

4.2. Area. The area of a QCA FA can be calculated by the total area covered by the circuit. The area of the QCA circuits is usually measured in μm^2. The formula for area measurement is simply the length multiplied by the breadth.

4.3. Wire Crossing Type. For transmitting the data from input to output, QCA wires are the basic needs. Two types of wire crossings are used: one is the coplanar type wire crossing, and the other one is the multilayer type of wire crossing. In the coplanar type of wire crossings, only one layer is being used, whereas for designing the multilayer type wire crossing, at least three layers are needed.

4.4. Delay/Latency. Delay is the required number of total clock cycles required to transit the data from input to output in the critical path of a QCA circuit.

4.5. Cost. The cost functions of QCA FA designs are calculated using the effective cost function calculation process presented in [7].

5. Simulation Result, Comparison, and Discussion

Numerous QCA full-adders have been designed so far. In this section, these previously designed QCA full-adder circuits will be investigated based on their complexity,

wire crossing type, area requirement, delay, and quantum cost. To compare QCA FAs, the designs are implemented and simulated using QCADesigner software [28]. The result, discussion, and comparison of QCA FAs are presented in the following subsections. Latency, majority gate and crossover types may influence the full adder design. Power dissipation, latency what should be considered in choosing the ideal full adder for use in higher-order designs or other applications.

5.1. Design and Performance Parameters of QCA FAs. A coplanar type QCA full adder is designed in [29] that are consisting of 192 QCA cells. The circuit covered an area of $0.2\,\mu m^2$. This design requires 14 clock cycles for which the latency is 14. Another coplanar type full adder is presented in [30], which requires 105 QCA cells and $0.17\,\mu m^2$ area. This circuit also requires 4 clock cycles for the output of the design. The quantum cost required for that circuit is 0.17. A circuit with a high cell count is presented in [31]. This design required 292 QCA cells with a $0.62\,\mu m^2$ area and 14 clock cycles. The quantum cost required for that circuit is 2.17. Another QCA FA requiring 102 cells is proposed in [32], which covers a $0.1\,\mu m^2$ area with a latency of 8. The quantum cost required for that circuit is 0.4. FA in [33] requires only 145 QCA cells that cover $0.16\,\mu m^2$ area. This design also has a latency of 4 and a quantum cost of 0.16. Another 220-cell-based QCA FA is presented in [34], which requires $0.36\,\mu m^2$ area. This requires 3 clock cycles to compute output for which its latency is 3. The quantum cost required for that circuit is 0.27. QCA FA consisting of 108 cells is presented in [35]. This design covered $0.28\,\mu m^2$ area, required 4 clock cycles and had a 0.08 quantum cost. An area-efficient QCA FA is proposed in [36]. This design has 78 QCA cells covering $0.22\,\mu m^2$ area. Latency for the circuit is 3. The cost of the design is 0.0675. A 59-cell based QCA FA coveting $0.08\,\mu m^2$ area with 4 clock cycles latency is presented in [37]. This design has 0.043 quantum cost. Five clock cycles based QCA FA consisting 124 QCA cells is presented in [38]. This QCA FA circuit covers $0.4\,\mu m^2$, and the cost is 0.125. A low complexity QCA FA using 102 cells is proposed in [39]. The adder circuit covers $0.097\,\mu m^2$ area. QCA FA in [40] covers $0.154\,\mu m^2$ area and requires 4 clock cycles. The cost of the circuit is 0.07. A robust area-efficient QCA full adder is proposed in [41], which covers $0.087\,\mu m^2$ area with 95 QCA cells. This circuit also requires 16 clock cycles and the quantum cost is 0.35. QCA FA consisting 61 cells and $0.07\,\mu m^2$ area coverage is presented in [42]. This circuit requires 2 clock cycles and has a quantum cost of 0.035. In [43], a QCA FA with low complexity is presented. This circuit covers $0.31\,\mu m^2$ area, requires clock cycle 2, and has a quantum cost 0.05. A high cell count coplanar QCA FA is demonstrated in [28]. The required number of cells is 396. This circuit covers $0.65\,\mu m^2$ area. The latency is 16 clock cycles and cost are 10.2. In [44], an 86-cell-based QCA FA circuit is demonstrated which covers $0.08\,\mu m^2$ areas. The latency for this circuit is 4. The cost of the circuit is 0.08. A circuit presented in [45] consists 60 cells and covers $0.11\,\mu m^2$. This circuit with 4 clock cycle latency has a cost of 0.06. Another FA with high cell count is shown in [46]. This circuit requires 28 QCA cells. The latency of the circuit is 2 and area coverage is $0.02\,\mu m^2$. Also, the cost of the circuit is 0.01. A 61-cell-based QCA FA is further presented in [47]. This circuit covers $0.06\,\mu m^2$ area, requires 3 clock cycles for the output and the cost is 0.0225. A circuit having 124 cells, covering area $0.12\,\mu m^2$ and having 12 clock zone latency is presented in [48]. The cost of the circuit is 0.27. A 63-cell-based FA is presented in [49]. This circuit required 3 clock cycles for the output and covers $0.1\,\mu m^2$. The quantum cost of the circuit is 0.0375. A low complexity FA with 71 cells is presented in [50], which covers $0.12\,\mu m^2$ with a latency of 3. The cost of the circuit is 0.045. In [51], a QCA FA with low complexity is presented. This circuit covers $0.04\,\mu m^2$ area, requires clock cycle 4, and has the quantum cost 0.04. Another FA having high quantum cells is presented in [52]. This circuit requires 118 QCA cells. The latency of the circuit is 3 and area coverage is $0.4\,\mu m^2$. A 95-cell-based QCA FA is further presented in [73]. This circuit covers $0.037\,\mu m^2$ area, requires 4 clock cycles for the output, and the cost is 0.12. With 59 QCA cell, another design is presented in [53]. This design covers an area of $0.04\,\mu m^2$, having the latency 3, and the quantum cost is 0.03. All QCA FAs presented in [28–54, 73] are coplanar type.

A multilayer type QCA full adder is presented in [54], which consists 93 cells covering an area of $0.087\,\mu m^2$. This design requires 4 clock cycles at a cost of 0.087. Another efficient QCA FA is presented in [55], which requires 135 QCA cells with a latency of 5. This circuit covers $0.61\,\mu m^2$ area with 0.175 as quantum cost. The QCA FA design in [56] is implemented with 73 cells which cover $0.09\,\mu m^2$. The latency for the circuit is 3, and the cost is 0.03. In [57], the QCA FA proposed covers $0.14\,\mu m^2$ with a latency of 6. This calculated quantum cost for this circuit is 0.08. An 82-cell-based QCA FA is further presented in [58]. This circuit covers $0.24\,\mu m^2$ area, requires 3 clock cycles for the output and the cost is 0.0675. A low quantum cost based QCA FA schematic is presented in [59], which required 86 cells with an area of $0.17\,\mu m^2$. The quantum cost is 0.06. A design with a $0.16\,\mu m^2$ area is presented in [60]. Delay for this circuit is 1 and cost is 0.0175. An area-efficient design is presented in [61] that requires 38 QCA cells covering an area of $0.02\,\mu m^2$. The circuit is also efficient in terms of speed since its latency is 6. The quantum cost for this circuit is 0.011. QCA FA presented in [62] requires only 79 cell which accounts for $0.064\,\mu m^2$ area. The latency for the circuit is 4 and the cost is 0.064. A QCA FA having area $0.076\,\mu m^2$, is presented in [63]. This design required 58 QCA cells which produce a latency of 3. The cost of this QCA FA circuit is 0.03. The schematic of QCA FA presented in [64] has 23 QCA cells with an area of $0.01\,\mu m^2$ and latency 3. The cost of this design is 0.0075. A QCA FA having a low area ($0.03\,\mu m^2$) and low quantum cost (0.02) is presented in [65]. The cell count for this design is 51. The latency of the circuit is 3. Another 79-cell-based QCA

FA design is proposed in [65]. The 79 cells cover 0.05 μm^2 area. This circuit needs 5 clock cycles for the output generation. Therefore, the calculated cost is 0.08. The design in [66] 0.02 μm^2 area due to having 31 QCA cells. This design requires only 2 clock cycles for output generation. As a result, the calculated cost is 0.01. A QCA FA design having 33 cells and 0.02 μm^2 area covered is shown in [67]. The latency of the circuit is 3 and quantum cost is 0.015. QCA FA in [68] requires 30 QCA cell to implement which corresponds to an area of 0.004 μm^2. The latency of the circuit is 4 and the cost is 0.004. With 22 QCA cells and 0.01 μm^2 area, a QCA FA is presented in [69]. The latency of this design is 3 for which the cost becomes 0.0075. Another QCA FA circuit having 61 QCA cells and 0.06 μm^2 area is presented in [70]. This design requires 3 clock pulses from the input to the output data transition. As a result, the cost is 0.0225. A QCA FA implemented with 31 cells is presented in [71], which covers 0.02 μm^2. The latency for the design is 2 for which the calculated quantum cost becomes 0.01. Another low area covering QCA full adder is presented in [72]. The full adder requires 33 QCA cells [74], 0.01 μm^2 area, has a latency 2, and the quantum cost 0.005. The design [75] requires 28 QCA that cover a 0.01 μm^2 area. The delay of that FA is 3 and its quantum cost is 0.007. For designing a 0.02 μm^2 FA, only 18 QCA cells were required [76]. The latency of that design is 2, which requires a 0.01 quantum cost. A 128 QCA cell requiring FA is presented in [77], which covers 0.15 μm^2 area with a latency of 3. [78] requires 82 QCA cells for that FA design, which covers a 0.06 μm^2 area. The quantum cost for that design is 0.045. Another low cell requiring multilayer type FA is presented in [79], which covers only 0.01 μm^2 area and whose latency is 3 and quantum cost is 0.007. All QCA FAs presented in [55–72, 74–79] are multilayered.

In circuit design, it becomes necessary to have a comparison of the performance parameters [80–83]. Based on the performance comparison parameters of QCA FAs discussed above, a summary is provided in Table 1. Latency, majority gate, and crossover types may influence the full adder design. Power dissipation and latency should be considered when choosing the ideal full adder for use in higher order designs or other applications.

5.2. Discussion. Since there are several performance parameters of a QCA circuit, the application of a QCA circuit will depend on the system requirement.s For example, systems with space constraints will use QCA FAs with a low cell count and area. On the other hand, systems, where speed is the most crucial parameter will focus on using QCA FAs with low latency. In brief, a designer needs to pick up the most suitable circuit by considering tradeoffs among QCA circuit parameters to meet the design and system requirements.

Based on the design and performance parameters presented in Table 1, it can be observed that QCA FA in [69] has the lowest cell count (22). QCA FA in [81] utilized only 1 more cell than QCA FA in [64]. Moreover, QCA FAs in [66–68, 71, 72] have a low cell count. On the other hand, QCA FA design in [28] has the highest cell count (396). Moreover, the cell counts of the QCA FA designs in [29, 31, 34] are very high. For systems that require a low QCA cell count, QCA FAs in [66–69, 71, 72] can be considered.

In terms of area coverage, the QCA FA designs in [64, 69] jointly achieved the best result. Conversely, FA [28] accounted for the highest area coverage compared to the other designs. Thus, for systems having area constraints, researchers and circuit designers may consider using QA FAs [64, 69] because they have less area coverage due to their low number of QCA cell count.

In terms of latency, QCA FAs in [28, 29, 31, 41] achieved the foremost results. The latency of FAs in [42, 43, 46, 60, 66, 71, 72] are quite low. On the other hand, QCA FA in [28, 41] has the highest latency. The latency of designs presented in [39, 48] are also quite high. Thus, for systems where speed is the main concern, designers can consider using QCA FAs in [28, 29, 31, 41–43, 60, 66, 71, 72].

Implementation of a multiple-bit adder using 1-bit QCA FA can be realized by using C_{out} signal of one bit cell as the C_{in} signal of the next bit. This sort of approach is known as ripple carry adder (RCA) [74]. Research works conducted in [28, 30, 32, 38, 39, 41, 44, 47, 52, 54, 66, 73] used RCA style to implement 4-bit adder. FAs in [40, 67] were extended to 8-bits using RCA style. Moreover, some of the QCA FAs are extended to multiple bits using advanced adder topologies such as Carry Look-Ahead (CLA Adder [75, 76]. Research works in [36] showed an extension to a 4-bit CLA adder. Authors in [56] extended their QCA FA to a 16-bit CLA adder. 64-bit CLA adder extension using QCA FA is shown in [59]. Other than CLA, researchers in [60] showed QCA FA-based 8-bit adder extension process using Brent-Kung, Kogge Stone, Ladner Fischer, and Han-Carlson methods. In systems where scalable architectures are required, these mentioned QCA FAs are to be considered for implementing wide word-length QCA adders.

5.3. Future Research. Energy dissipation in circuits is a major concern for circuit designers. This research only focused on the physical parameters of QCA FA cells. As a part of future research, the energy dissipation of QCA FA cells can be considered. To measure energy dissipation, QCAPro can be utilized as a simulation tool [84]. The hamming distance technique explained in [85] can be considered as another way to estimate energy dissipation of QCA FA cells; however, QCADesigner Pro in [86] is used by most of the researchers.

Table 1: Performance parameter comparison of QCA full adder circuits.

Name of the author	Year of publication	QCA FA designs	No. of cell (complexity)	Wire crossing type	Area (μm^2)	Delay (clock cycles)	Cost
Tougaw and Lent	1994	[29]	192	Coplanar	0.2	14	0.70
Vetteth et al.	2002	[31]	292	Coplanar	0.62	14	2.17
Wang et al.	2003	[30]	105	Coplanar	0.17	4	0.17
Zhang et al.	2004	[33]	145	Coplanar	0.16	4	0.16
Zhang et al.	2005	[55]	93	Multilayer	0.087	4	0.087
Cho	2006	[59]	82	Multilayer	0.24	3	0.18
Kim et al.	2007	[34]	220	Coplanar	0.36	3	0.27
Hanninen and Takala	2007	[39]	102	Coplanar	0.097	8	0.194
Cho and Swartzlander	2007	[56]	135	Multilayer	0.61	5	0.762
Cho and Swartzlander	2009	[36]	78	Coplanar	0.22	3	0.165
Hänninen and Takala	2010	[32]	102	Coplanar	0.1	8	0.20
Navi et al.	2010	[57]	73	Multilayer	0.09	3	0.03
Navi et al.	2010	[71]	61	Multilayer	0.06	3	0.0225
Bishnoi et al.	2012	[41]	95	Coplanar	0.087	16	0.35
Pudi and Sridharan	2012	[63]	79	Multilayer	0.064	4	0.064
Hashemi et al.	2012	[66]	79	Multilayer	0.05	5	0.0625
Pudi and Sridharan	2012	[60]	86	Multilayer	0.17	4	0.085
Sen et al.	2013	[67]	31	Multilayer	0.02	2	0.01
Kianpour et al.	2014	[40]	69	Coplanar	0.154	4	0.154
Kunalan et al.	2014	[28]	396	Coplanar	0.65	16	2.60
Angizi et al.	2014	[47]	61	Coplanar	0.06	3	0.0225
Suresh and Ghosh	2014	[48]	124	Coplanar	0.12	12	0.36
Roohi et al.	2014	[64]	58	Multilayer	0.076	3	0.03
Abedi et al.	2015	[37]	59	Coplanar	0.08	4	0.08
Mohammadyan et al.	2015	[43]	96	Coplanar	0.31	2	0.155
Hashemi and Navi	2015	[50]	71	Coplanar	0.12	3	0.0450
Navi et al.	2015	[53]	59	Coplanar	0.04	3	0.03
Sayedsalehi et al.	2015	[58]	105	Multilayer	0.14	6	0.21
Roohi et al.	2015	[65]	23	Multilayer	0.01	3	0.0075
Roohi et al.	2015	[65]	51	Multilayer	0.03	3	0.0225
Angizi et al.	2015	[74]	33	Multilayer	0.01	2	0.005
Waje and Dakhole	2016	[35]	108	Coplanar	0.28	4	0.28
Kumar and Mitra	2016	[38]	124	Coplanar	0.4	5	0.50
Sen et al.	2016	[44]	86	Coplanar	0.08	4	0.08
Labrado and Thapliyal	2016	[49]	63	Coplanar	0.1	3	0.0375
Sasamal et al.	2016	[51]	49	Coplanar	0.04	4	0.04
Sonare and Meena	2016	[73]	95	Coplanar	0.037	4	0.12
Mohammadi et al.	2016	[62]	38	Multilayer	0.02	6	0.011
Sarmadi et al.	2016	[69]	30	Multilayer	0.004	4	0.004
Goswami et al.	2017	[45]	60	Coplanar	0.11	4	0.11
Safoev and Jeon	2017	[72]	31	Multilayer	0.02	2	0.01
Abdullah-Al-Shafi and Bahar	2018	[46]	28	Coplanar	0.02	2	0.01
Zhang et al.	2018	[52]	118	Coplanar	0.4	3	0.03

Table 1: Continued.

Name of the author	Year of publication	QCA FA designs	No. of cell (complexity)	Wire crossing type	Area (μm^2)	Delay (clock cycles)	Cost
Seyedi and Navimipour	2018	[70]	22	Multilayer	0.01	3	0.0075
Seyedi and Navimipour	2018	[70]	22	Multilayer	0.01	3	0.0075
Seyedi and Navimipour	2018	[78]	86	Multilayer	0.06	3	0.045
Maharaj and Muthurathinam	2020	[54]	13	Coplanar	0.009	2	0.018
Seyedi and Navimipour	2020	[77]	128	Multilayer	0.15	3	0.11
Joy et al.	2021	[42]	61	Coplanar	0.07	2	0.035
Seyedi and Navimipour	2021	[75]	28	Multilayer	0.01	3	0.007
Seyedi and Jafari Navimipour	2022	[76]	18	Multilayer	0.02	2	0.01

6. Conclusion

Since quite a number of QCA FA circuits have been developed over the course of time, it becomes quite essential to provide an extensive review of the designs. However, existing review articles on QCA FA provide only a little information on the overall circuits and their performance parameters. Therefore, a study to fill up the research gap of existing QCA FA review papers becomes the need of the day. Therefore, a comprehensive study on existing QCA FA circuits has been conducted in this research. A total of 47 QCA FA circuits have been chosen for analysis and comparison. A brief overview of the QCA-based logic design method has been provided to understand QCA-based FA design methodology. The circuit design methods of QCA FA circuits have been analyzed. Moreover, a summary table of all parameters related to QCA FA performance comparison has been provided to have a swift overview of QCA FA circuits. Above all, the extensive literature review and performance comparison summary table provided in this research will aid researchers by cutting off their time to search, implement, analyze, and compare the numerous QCA FA circuits to find the best possible cell as per the system requirements.

Data Availability

No data were used to support the findings of this study.

Conflicts of Interest

The authors declare that there are no conflicts of interest.

Authors' Contributions

Upal Barua Joy performed conceptualization, formal analysis, investigation, methodology, software, and writing of the original draft. Shourov Chakraborty was responsible for conceptualization, formal analysis, investigation, methodology, and writing of the original draft. Sharnali Islam performed conceptualization, supervision, writing, review, and editing. Hasan U. Zaman was responsible for conceptualization, supervision, writing, review, and editing. Mehedi Hasan was responsible for conceptualization, supervision, writing, review, and editing.

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