

# ON THE SENSITIVITY OF CANONICALLY EXTENDED RC-ACTIVE MULTILoop FILTERS

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A class of multiloop active filters based on a double RC ladder of simple recurrent structure, constrained by a single, positive gain, voltage-controlled voltage source has received recent attention in the literature.

Some design considerations are discussed in this paper and sensitivity results are presented which permit comparisons to be made between filter realizations with different types of capacitance spread constraints. It is shown that the common practice of constraining all capacitors to be equal leads to high sensitivity and that, by relaxing this zero-spread requirement, much more favourable sensitivity results can be obtained.

## 1. INTRODUCTION

This paper is concerned with sensitivity properties of a class of RC-active filters. The general form of these networks is shown in Figure 1 and consists of an RC double ladder constrained by a voltage-controlled voltage source (VCVS) to provide a multiloop-feedback structure. Figure 2 shows two well-known and extensively used special cases of this general form, the Rauch and Sallen and Key sections.

The present study considers filters developed by canonical extension of the Sallen and Key section to give single-amplifier networks realizing transfer functions of arbitrary order. (In the present context, 'canonical' implies that  $n$  capacitors are required to realize an  $n$ th-order transfer function.) Figure 3 shows the general form of these canonical networks. The filters share the attractive features of the basic Sallen and Key section: they are easy to cascade because of the voltage source output; they exhibit good dynamic range and can be designed for a low-valued, positive VCVS gain which can be realized easily and accurately by low-cost op.amps. The higher-order

sections have the additional benefits of low power consumption, low active and passive component count and a simple, recurrent, structure.

The network of Figure 3 realizes an  $n$ th-order all-pole voltage transfer function (VTF) of the form

$$\frac{V_{out}(s)}{V_{in}(s)} = K \left[ 1 + \sum_{i=1}^n a_i s^i \right]^{-1} \quad (1)$$

where  $K$  is the gain of the VCVS. Assuming that, at the design stage,  $K$  is specified and fixed, there are  $2n$  design variables (the passive components) for  $n$  design equations derived from consideration of the VTF coefficients, the  $a_i$  in Eq. (1). Hence the designer has  $n$  degrees of freedom at his disposal. A

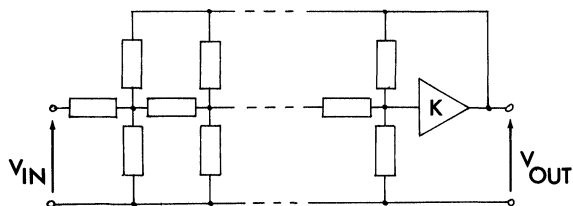


FIGURE 1 General form of multiloop network.

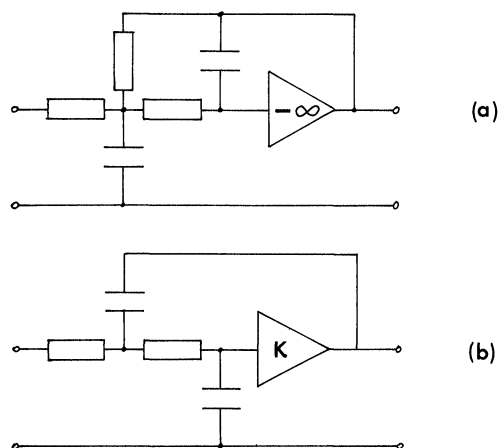
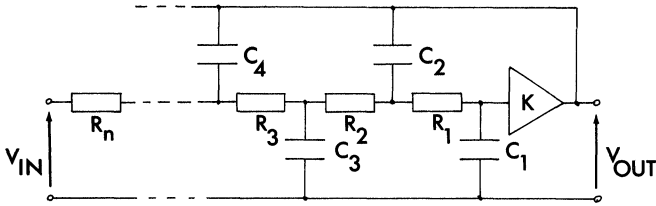


FIGURE 2 Rauch (a) and Sallen and Key (b) second-order, low pass sections.

FIGURE 3 *N*th-order canonical filter section.

number of workers have considered the design of this type of network (for summaries, see refs. 1 and 2) and a common response to the availability of design freedom is to constrain the capacitors to be equal.<sup>3,4</sup>

From results to be presented here, it will be shown that considerable care is needed in deploying these degrees of freedom and that, in particular, they may be more profitably used in reducing the sensitivity of the filter rather than in obtaining equal-value capacitors (EVC).

## 2. THE COMPUTER-AIDED DESIGN SCHEME

Before considering the results obtained during this study, it is proposed to outline the design procedure used in deriving them.

For low-order filters, and assuming equal-value capacitors, the design equations are sufficiently simple as to permit explicit coefficient matching.<sup>4,5</sup> This design simplicity provides a considerable motivation for the EVC approach. However, where a fully general scheme is required that allows the capacitors to be either constrained or free variables, such methods are inadequate and the approach adopted here is to use computer optimization to accomplish the design.

Figure 4 shows the organisation of a typical computer optimization scheme. The specification is formulated in terms of the complex frequency VTF by specifying the required values of the  $a_i$  and  $K$  in Eq. (1) above. A network of the correct order ( $n$ ) is input by the user and guess starting values for the passive components are proposed (usually unity for these normalized realizations). This 'guess network' is then analysed to determine the numerical values of the transfer function coefficients realized by the network in its current form. An error function,  $\epsilon$ , is now formulated by comparing the realized and specified coefficients,  $a_i$  and  $a_{si}$  respectively.

$$\epsilon = \sum_{i=1}^n (a_{si} - a_i)^2 \quad (2)$$

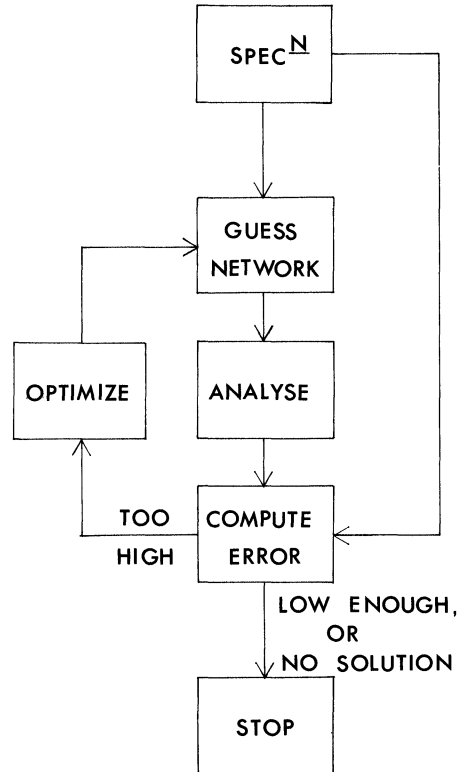


FIGURE 4 Computer optimization scheme.

Note that this formulation ensures zero error only when each of the realized coefficients has the desired value. Having thus quantified the error, the design process terminates if the error value is zero (or near-zero, having due regard for machine-generated rounding errors). If, as is usual in the early stage of the design, the error is too high, the optimization algorithm adjusts the component values so as to reduce it. The design process iterates until either a satisfactory solution is obtained, or indications that no solution is possible are detected.

Because of the iterative nature of the design scheme, the algorithms used must be as efficient as possible: in particular, effective optimization and analysis strategies are required if design cost is to be low.

The optimization algorithm used here is based on a damped least squares scheme<sup>1,6</sup> and fully exploits the comparatively simple form of the error function, Eq. (2).

The analysis scheme is a special-purpose one developed for networks of the particular topology considered here so as to provide minimum analysis

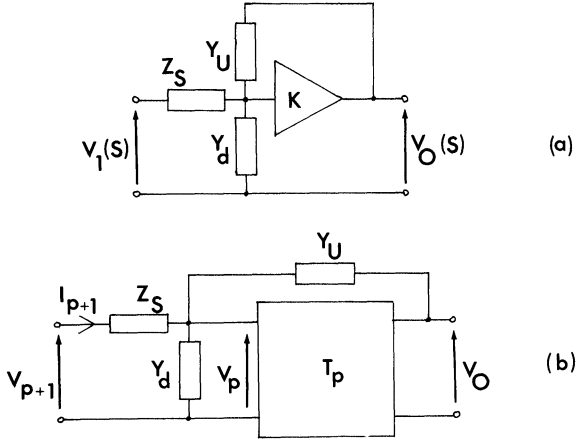


FIGURE 5 Recursive structure of general network for analysis.

times. The scheme is discussed in detail elsewhere,<sup>1</sup> but the main results are reviewed here.

Assuming a network of the form of Figure 1, note that the first section, counting from the VCVS, can be represented as in Figure 5a. The transmission matrix for this structure can be determined and the next passive section can be added as shown in Figure 5b. Thus the circuit of Figure 5b provides a recursive model for the analysis of the complete network. Assuming that the first  $p$  sections of the network have been so assembled to yield the transmission matrix  $T_p$ , where

$$T_p = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} \quad (3)$$

Regarding the VCVS as the zeroth section,

$$A_0 = \frac{1}{K}, \quad B_0 = C_0 = D_0 = 0 \quad (4)$$

it can then be shown [op.cit.] that  $B_p = D_p = 0$  and

$$\begin{aligned} A_{p+1} &= A_p + Z_s C_{p+1} \\ C_{p+1} &= A_p (Y_u + Y_d) + (C_p - Y_u). \end{aligned} \quad (5)$$

When all  $n$  sections of the network have been added, the overall network realizes the equations:

$$\begin{bmatrix} V_n \\ I_n \end{bmatrix} = \begin{bmatrix} A_n \\ C_n \end{bmatrix} \cdot V_0, \quad (6)$$

so that the VTF is found as

$$\frac{V_0(s)}{V_n(s)} = \frac{1}{A_n(s)} \quad (7)$$

Eqs. (4), (5) and (7) constitute the special-purpose

analysis procedure used in the present scheme.

Overall CPU run times (including sensitivity analysis) are typically in the order of 1 s to 2 s for networks of order 3, up to about 10 s for 9th-order networks when the scheme is implemented on a PDP-10 time-sharing system.

### 3. SENSITIVITY RESULTS

In the foregoing section, an efficient computer-aided design scheme for the synthesis of canonically-extended Sallen and Key-type filters has been described. It is now intended to present sensitivity results for the realizations of common filter specifications so derived. Since the purpose of this paper is to indicate the general effects of different capacitance constraint strategies on the sensitivity of the filters, it is not intended to present extensive tabulations of component values. The interested reader will find such tabulations in a paper by Massara and Fidler<sup>1</sup> from which the networks considered below have been derived.

In the graphs that follow, two sensitivity criteria are plotted, the maximum gain sensitivity,  $S_K$ , and the maximum worst-case passive component sensitivity,  $S_p$ . These criteria are defined as follows:

$$S_K \triangleq \max_i \left| \frac{K}{M(\omega_i)} \cdot \frac{\partial M(\omega_i)}{\partial K} \right|, \quad 0 \leq \omega_i \leq 1 \text{ rad/s} \quad (8)$$

$$S_p \triangleq \max_{ij} \left| \frac{x_j}{M(\omega_i)} \cdot \frac{\partial M(\omega_i)}{\partial x_j} \right|, \quad 0 \leq \omega_i \leq 1 \text{ rad/s} \quad (9)$$

$j = 1, 2, \dots, m$

where the  $\omega_i$  are the discrete angular frequency points chosen to lie in the normalized passband, the  $x_j$  are the  $m$  passive components and  $M(\omega_i)$  is the amplitude response function evaluated at  $\omega_i$ :

$$M(\omega_i) = \left| \frac{V_0(j\omega_i)}{V_n(j\omega_i)} \right|. \quad (10)$$

These practical sensitivity measurements register respectively the maximum modulus values of 1) the gain sensitivity and, 2) the most sensitive passive component's sensitivity, over the normalized passband.

To establish a basis for comparison, EVC realizations are considered first. Figure 6 shows  $S_K$  and  $S_p$  plotted as functions of filter order for Butterworth and Chebyshev (1dB passband ripple) filters for the case  $K = 2.2$ . This value of VCVS gain was selected because higher-order EVC realizations are possible only for a very limited range of gain

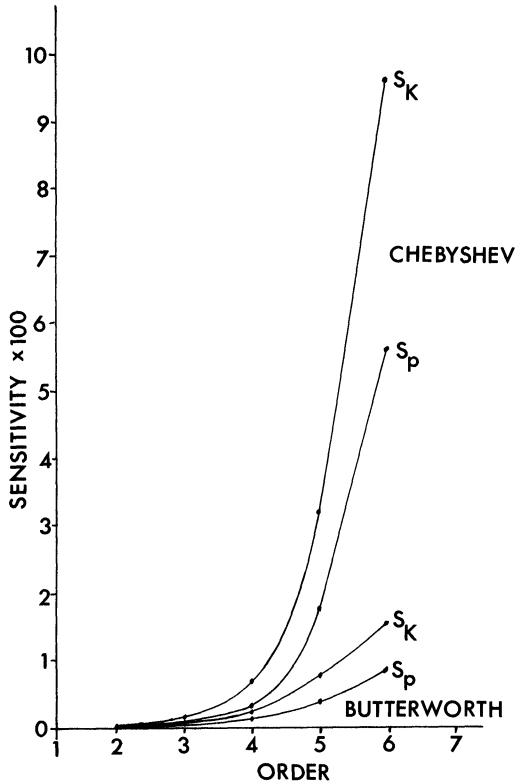


FIGURE 6 Plot of  $S_K$  and  $S_p$  against order for EVC filters.

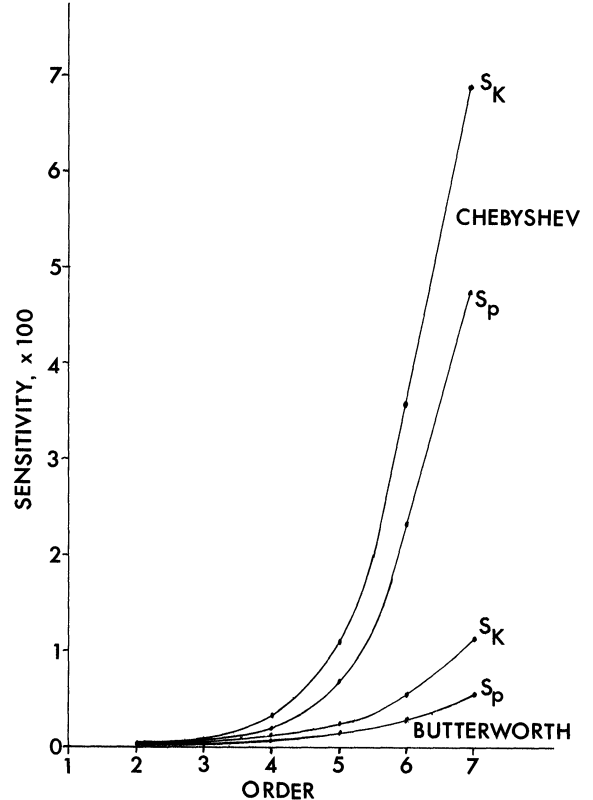


FIGURE 7 Plot of  $S_K$  and  $S_p$  against order for unconstrained-capacitor filters.

values<sup>1</sup>: in fact, for given order,  $S_K$  and  $S_p$  do not vary markedly with  $K$ . As might be anticipated, the Chebyshev filters are seen to be conspicuously more sensitive than Butterworth types for given order, and sensitivity is strongly dependent on order. Practical experience suggests that feasibility levels be set at approximately 30 and 20 for  $S_K$  and  $S_p$  respectively. Hence, the Butterworth realizations can be regarded as infeasible for orders greater than 4 and the Chebyshev filters for orders greater than 3.

Since the design scheme described above allows for a more general approach, realizations are considered next in which the capacitors are allowed to vary freely during the design process resulting in what will be termed unconstrained-capacitor filters. Figure 7 shows sensitivity results as before for the Butterworth and 1dB Chebyshev cases. VCVS gain is again set at 2.2 for comparability with the results of Figure 6. It can be seen that the overall sensitivity levels are now reduced very significantly and this leads to improved realization feasibilities: Butterworth and 1dB Chebyshev filters are realizable for orders up to and including the 5th and 4th respectively. A further practical point is that the unconstrained-capacitor

approach makes available a much wider range of VCVS gain realizations.<sup>1</sup>

It has been stated that the sensitivity indices used are most significantly functions of filter order rather than gain. To demonstrate this, Figure 8 shows the variation of  $S_K$  with VCVS gain  $K$  for unconstrained Butterworth filters of orders 2 to 6. Note that  $S_K$  does not show marked variation for given order over the range of  $K$  values usually chosen,  $1 \leq K \leq 3$ . It is inadvisable to choose high  $K$  values since passive and active sensitivities increase significantly for  $K > 4$ , particularly for the higher-order cases.

Finally, results are presented for an intermediate type of realization in which the capacitors are regarded as variables but are constrained to approach a specified level, usually unity. This leads to a reduction in capacitance spread compared with the totally unconstrained filters, but avoids the problem of limited range of VCVS gain values associated with EVC filters. These networks have been termed constrained-capacitor filters.<sup>1</sup>

Figure 9 compares  $S_K$  and  $S_p$  against order for

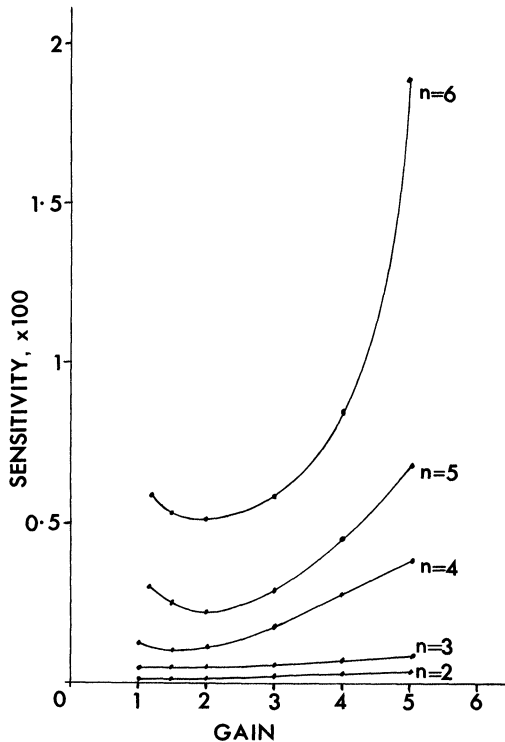


FIGURE 8 Plot of  $S_K$  against  $K$  for unconstrained-capacitor Butterworth filters of various orders,  $n$ .

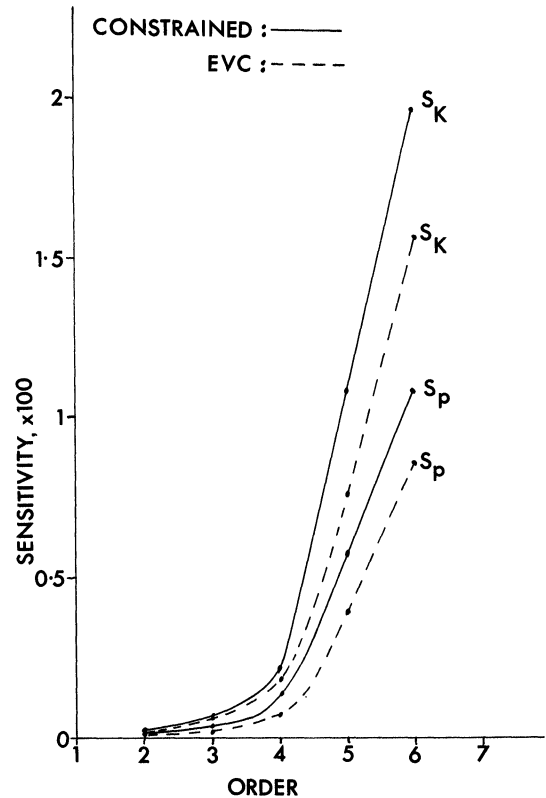


FIGURE 9 Plot of  $S_K$  and  $S_P$  against order for EVC and constrained-capacitor Butterworth filters.

EVC and constrained realizations, again for the case  $K = 2.2$ . Notice that the results for the constrained filters are worse than those for the EVC filters. This final result suggests that, by incorporating suitable sensitivity minimization into the design scheme based on the constrained-capacitor approach, it should be possible to obtain realizations that offer low capacitor spread together with minimum active and passive sensitivities.

#### 4. CONCLUSIONS

A computer-oriented optimization scheme for the design of a class of active filters of arbitrary order has been described. It has been shown that sensitivity considerations render infeasible the higher-order structures, and that the type of capacitance constraint applied in the design also has significant sensitivity implications. The results presented show that the relationship between capacitance spread and sensitivity is not completely inverse and current work is directed towards the design of optimal low-spread, low-sensitivity realizations.

A further area of study is the synthesis of cascaded

high-order filter realizations in which the separate sections are of orders higher than the 1st or 2nd-order sections usually encountered. Capacitor spread and sensitivity minimization can be applied as discussed above in connection with single-stage realizations: the resulting filters should offer improved overall sensitivities and capacitance spread with low power consumption and low active component count.

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