*Electrocomponent Science and Technology*, 1981, Vol. 9, pp. 139–145
0305-3091/81/0902-0139 $06.50/0


# PERMANENT INTERCONNECTION TECHNOLOGY ELECTRONIC INTERCONNECTIONS – THE PRINTED WIRING BOARD†

I. G. LANG
*Exacta Circuits Limited – Selkirk, Scotland, U.K.*

(*Received November 21, 1980; in final form June 8, 1981*)

Modern manufacturing techniques which have been developed in respect of interconnection and packaging systems using printed circuit boards, are outlined. It is shown that these systems are capable of meeting present and future requirements for component mounting, including VLSI.

## 1. INTRODUCTION

Faced with the bewildering proliferation of alternative interconnection solutions it might be possible to underestimate the advantages of the high volume, high yield PCB industry. However, contrary to popular belief, the PCB Industry is already meeting the changing requirements of electronic packaging brought about by the impact of LSI and VLSI technology.

It is not the intention of this paper to give an in-depth review of silicon devices, but it is necessary to highlight some of the significant trends in micro-electronics technology in order to relate adequately to the macro-electronics packaging technology of the PCB substrate.

## 2. INTERCONNECTION TRENDS

In 1980 the Dual In-line package (DIP) was the dominant and standard IC Package. A recent survey by Mackintosh Consultants on behalf of Exacta, however, has indicated that chip carriers (CC) and spider bonding (TAB) will rapidly grow in application. The most likely scenario is as shown in Figure 1.

## 3. FACTORS INFLUENCING CHANGE

Considerations behind the packaging change shown in Figure 1 include the following factors:

a) *Packaging Density*, where product or equipment size is a major design criteria.

b) *Cost Reduction*, to be achieved by space and/or size saving.

c) *Performance*, as defined in terms of the signal speed in the circuit system. The over-all length of the internal wiring is significant in this respect.

d) *DIP Packaging Constraints*, particularly with regard to heat dissipation and of the numbers of input/output pins required.

## 4. IMPACT OF INTEGRATION

The IC is the driving force behind electronics development, and integration at chip level will continue to grow. It will become less possible to treat component and system/equipment design as separate exercises and there is an increasing realisation that design should not be partitioned too early and without reference to anticipated technological advances. For example, the optimum system design for, say, a 1983 product should predict and utilise a 1983 component or system architecture technology.

It might be thought that as integration grows at chip level the macro-packaging would become simplified. This has not been the case in the past and it is unlikely to be the case in the future as human ingenuity and market demands continue to encourage products which can have higher performance or cost less. A range of macro packaging technologies is and will continue to be available but the correct combination to be selected will vary with the industry sector and application, e.g. whether it is a consumer product, an aerospace

†Paper originally given in the Technical Papers programme of Electronica, Munich, November, 1980.

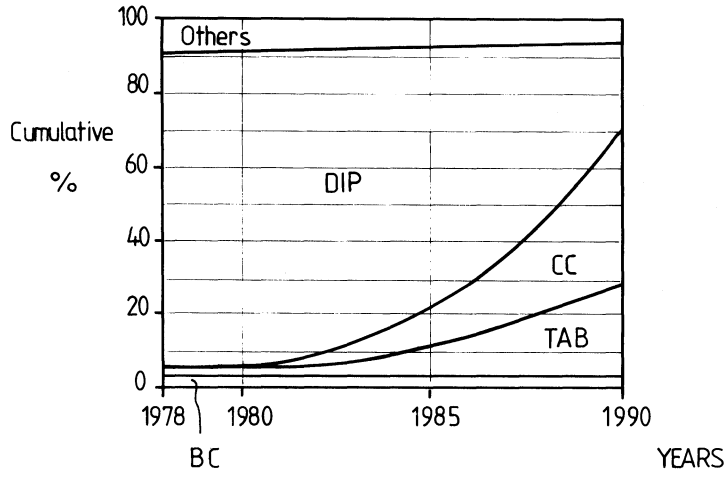



FIGURE 1 Worldwide I.C. Package usage. (Cumulative % for various technologies).

application, a computer mainframe requirement, or an electronic toy.

The impact of integration on the substrate requirement can be summarized as follows:

a) Increased interconnection density is required with the increase in number of input/output pins per chip.

b) Earth and voltage planes at precisely controlled distances from conductors may be required to provide impedance control and reduce cross talk.

c) Tracks will become smaller to minimise capacitance and maximise density and yet will have to retain high conductivity to minimise any voltage drop in the track.

d) Thermal management will become a major consideration.

Given the above considerations, at a recent interconnection seminar held in conjunction with BPA and Exacta, the following optimum substrate specification shown in Table I was evolved.

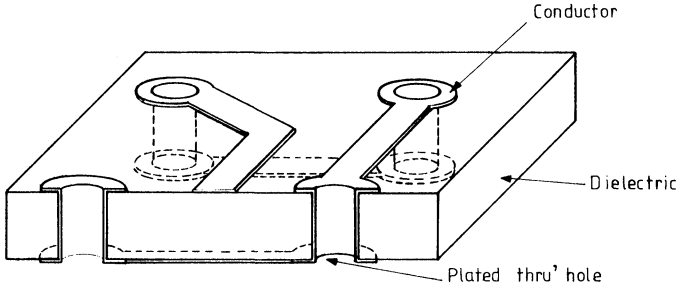
TABLE I
Optimum substrate specification.

| | |
|---|---|
| Design/modification turnround | 7 days |
| Thermal dissipation | 2 watts $in^{-2}$ (645 $mm^2$) |
| Interconnection density | 0.25 mm grid |
| Assembly yield | 90% using electrically pretested components and substrates |
| Substrate access | Space for hard wired modification during development |
| Component attachment | By solder. Joints to withstand 5 changes. Offer surface mounting as well as through hole mounting capability |
| Substrate test | Access to 0.25 mm grid |
| Reliability | $10^{-9}$ failures/joint/hour |
| Environmental performance | −50°C to +125°C. Withstand 40 g shock. Withstand 2 g vibration in range 5 to 500 Hz |
| Substrate size | Determined by optimum replacement unit or functional building block |
| Electrical characteristics | Controlled impedance for interconnection lengths greater than 2 inches. Ground plane screening |
| Assembly and test | Automatic |
| Cost | Provide reduction of overall system cost |

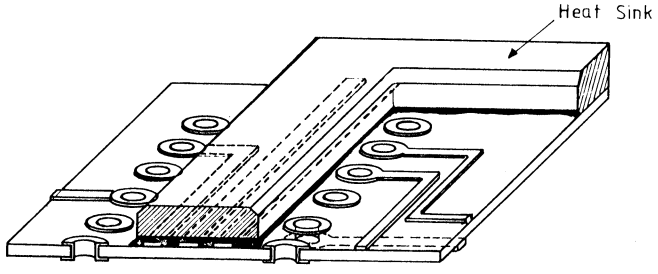
Can PCB manufacturing develop to meet the demands given in Table I? In fact many of the larger manufacturers who carry their own R & D teams and who operate at the higher technology end of the market can already fulfill most of this specification.

## 5. A PCB SUBSTRATE SOLUTION

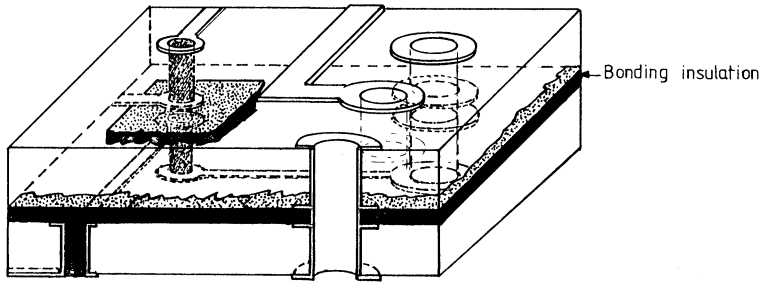
Generally, a fine line, controlled dielectric, copper conductor substrate can meet the specification of Table I, and an extensive range of interconnection possibilities can be available at typically printed wiring board costs. There is a broad relationship between overall system packing density and the probability of electrical success. Some existing varieties of PCB systems are shown in Figure 2(a)–(h). The relationship between these existing PCB systems and achievable packing densities against broad PCB costs is shown in Figure 3 and a curve showing the probability of electrical malfunction vs Packing density has been superimposed on the diagram.




(a) Double sided plated thru- hole printed circuit board.

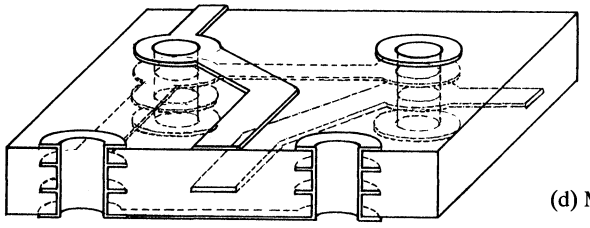



(b) Thin laminate (0.008″) with surface mounted heat sink.

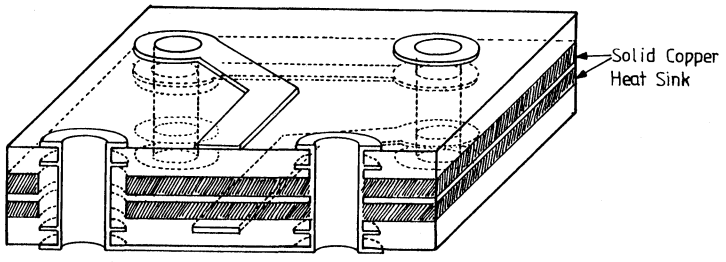



(c) Double double sided plated thru' hole printed circuit board.

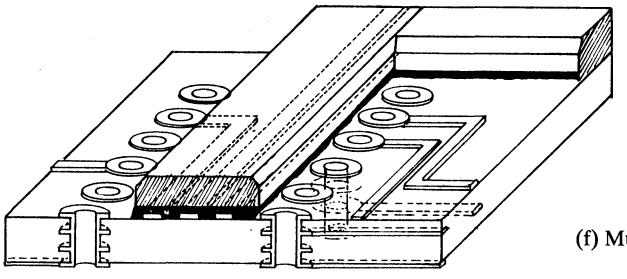
FIGURE 2 (*Continued overleaf*)



(d) Multilayer printed circuit board. (Intermediate layers not shown).

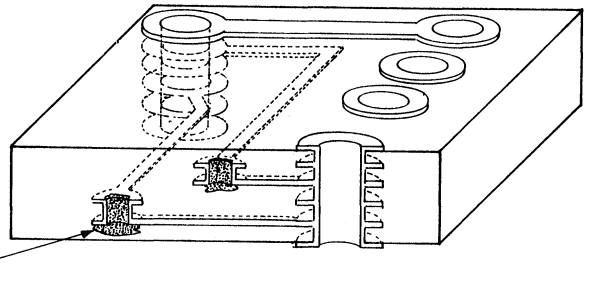


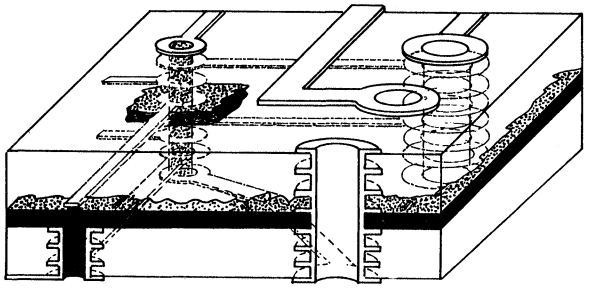

(e) Multilayer printed circuit board with internal heat sink.



(f) Multilayer printed circuit board with surface mounted heat sink.

(g) Buried via hole multilayer printed circuit board.



(h) Double multilayer printed circuit board.

FIGURE 2 Varieties of PCB systems (The dimensions can be appreciated by realising that the closest centre to centre distance between the holes in the dielectric is 0.1 inch).

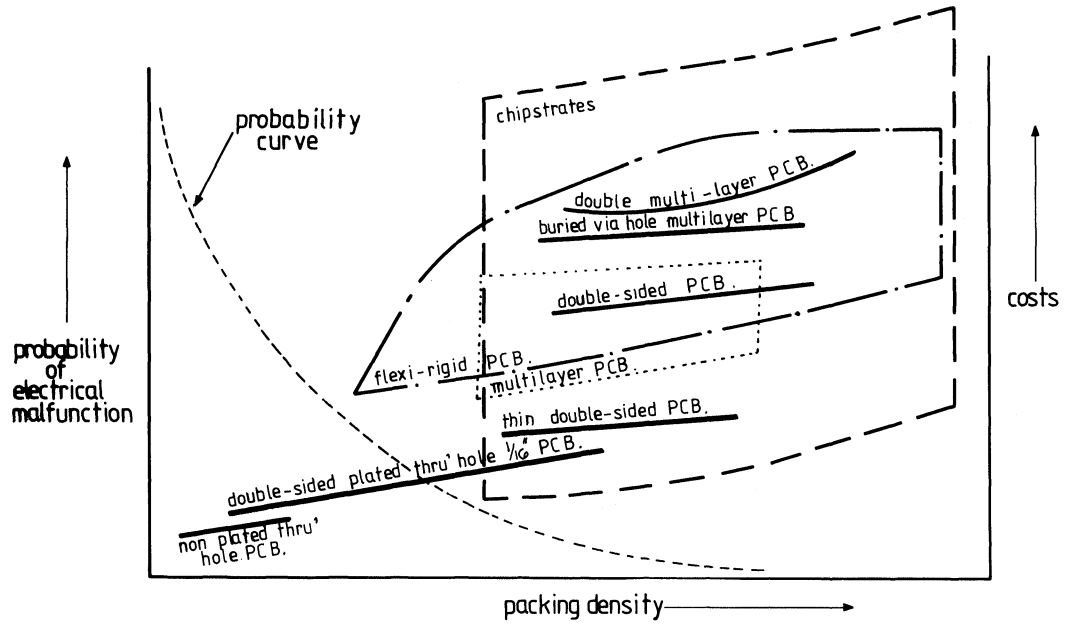



FIGURE 3 Costs vs Packing density for various PCB techniques. (Probability of electrical malfunction vs Packing density super-imposed).

Included in Figure 3 is reference to the substrate known as a CHIPSTRATE† which is the furtherance of methods of placing conductors and a large variety of insulators in similar three dimensional orientations to those shown in Figure 2 to provide a finished substrate which is suitable for the surface mounting of lead-less components.

The higher technology end of the packaging spectrum will be covered by fine line pillar plated, sequentially produced multilayer boards using as low a permittivity material as possible. Such a system is shown in Figure 4.

## 6. PCB DIELECTRICS

From a study of properties, processability and costs a list of the most promising resins and reinforcement can be made. This is shown in Table II.

Further work in this area will doubtless produce improved polymers and reinforcements.

For fine line, thin boards the characteristics required are:

a) as low a dielectric constant as possible.

b) as high a continuous service temperature as possible.

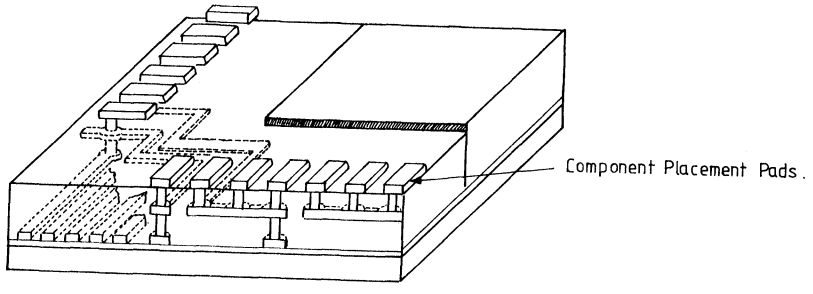



FIGURE 4 Pillar plated printed circuit board (distance between component placement pads ≥ 0.020 inch).

†CHIPSTRATE – a trade mark of Exacta Circuits, Ltd

TABLE II
Properties of useful PCB dielectrics.

| Material | Dielectric constant | Temp. limit (°C) | Coeff of expansion in $x$–$y$ plane (ppm/°C) |
|---|---|---|---|
| *Resin* | | | |
| Epoxy | 3.5 | 150 | 60–90 |
| Polyimide | 5.4 | 260 | 40–70 |
| PTFE | 2.1 | | 130–190 |
| Acrylonitrite butadiene | 5.3 | | 120–200 |
| Polysulphone | 3.0 | 150 | 54 |
| *Resin/Woven glass* | | | |
| Epoxy | 4.6 | 160 | 10–15 |
| Polyimide | 4.6 | 260 | 9–13 |
| PTFE | 2.4–2.6 | 260 | 10–15 |
| Triazine | 4.5 | 260 | 9–14 |
| *Resin/Kevlar reinforcement* | | | |
| Polyimide | 4.7 | 260 | 0–10 |

c) a coefficient of expansion as near as possible to ceramic (8ppm/°C) for leadless chip carrier attachment.

Whilst not critical for leaded components the coefficient of expansion characteristic should be met as closely as practical to provide maximum in-service reliability through thermal cycling. In practice the reliability achieved with epoxy glass when coupled with modern electroplating practices is satisfactory.

## 7. CURRENT PCB INDUSTRY EXPERIENCE

The industry has current high volume processing experience with epoxy, polyimide, PTFE and acrylonitrile butadiene and it is significant that it is only in the wet chemical processing area where slight variations occur, whereas mechanical, photolithographic and handling processes are common regardless of substrate material.

Generally with current products, mixtures of polymers are encountered within one substrate, e.g. with a flexirigid multilayer board there can be found polyimide, acrylic adhesive, modified epoxy adhesive and epoxy, or with a high frequency microwave multilayer circuit board there can be PTFE, FEP, modified epoxy and epoxy. These polymer mixtures witin one substrate have provided the impetus to establish processing methods which can accommodate a range of dielectric materials.

The PCB industry already has available a wide range of processing methods such as photolithography; plasma etching systems; electroless deposition; precision mechanical feature generation and electroplating. There are also capabilities in numerically controlled lasers to provide features such as edges, and through blind holes in non-reinforced dielectrics. Also wet polymer application and curing methods are used so that all the necessary ingredients can be available for the economic production of fine line, controlled dielectric, polymer substrates.

### 7.1 DESIGN/MODIFICATION TURNROUND

Using currently available computer aided design and manufacturing techniques it is quite possible to transmit a design change digitally along with other key data to the manufacturer who then uses the data directly in key processes such as: Photoplotting, NC drilling, profiling and laser scribing and automatic electrical test; i.e. those areas in substrate manufacture which are unique to the type and which traditionally take most of the time in the manufacturing cycle.

## 8. PCB INTERCONNECTION DENSITY

One of the important requirements given in the specification of Table 1 was that of PCB Interconnection Density. Currently a 0.50 mm grid is common with an increasing use of a 0.35 mm grid. Many larger manufacturers produce high volumes of work on a 0.25 mm grid, i.e. 4 tracks between a conventional 0.254 mm grid encompassing the standard DIP. This demands a satisfactory

photoprinting process with adequate resolution and a high standard of maintained cleanliness, i.e. managerial and process controls coupled with the operational techniques required to provide the high yield. The photoprinting processes used already typically takes place in a class 100 clean room with controlled temperature/humidity, and the refinement of operational/management/process controls in such areas will be required in order to maintain the existing high yields as line widths become smaller. Current dry resists are used to provide a 0.2 mm grid whereas wet resists are certainly capable of much finer work.

## 9. PCB CONDUCTOR/FINISHES

Currently copper, tin, nickel, gold, tin/lead are in general use, deposited by electroplating, electroless or vacuum techniques. These have the appropriate satisfactory properties of high conductivity, high thermal distribution and easy component attachment.

## 10. COMPONENT ATTACHMENT

As stated earlier, the coefficient of expanasion of the substrate should be in the range 5–10 ppm to match the possible use of ceramic leadless chip carriers. (This is not an important consideration with plastic or compliant leaded chip carriers and TAB, where the bare but hermetically passivated chip is used directly or when leadless chip carriers are used with sockets.) There are mixed feeling concerning the attachment of leadless chip carriers to PCB's with the more conservative companies pointing to the thermal mismatch as a potential problem. However, others have appreciated the potential yielding plasticity of the substrate dielectric and of the solder joint. As an example, Martin Marietta and the USAF 2 have published work indicating that leadless chip carriers can be attached to epoxy glass, polyimide or triazine PCB's and that this approach is adequate for benign to moderately severe environments and that the reliability of such a system is at least equal to that of conventional PCB packaging. Much more published work is required here to increase the acceptance of such a system and there are many in the industry who are evaluating the relative performances. It is probable that the currently used resin systems will prove to be satisfactory but work will continue on types such as Kevlar reinforced polymers following the published work of Stewart Greer of IBM[3] defining which low expansivity organic substrates can be fabricated and used.

## 11. CONCLUSIONS

An optimised packaging solution for many system applications using modern components such as LSI and VLSI chips, will remain with printed circuit boards. PCBs have already been modified to provide finer lines, reduced dielectric, reduced dielectric constants and increased interconnection chemistry, and can be manufactured using existing technology. The long established technology of pillar plating will increase in importance. Perhaps in future the PCB initials may stand for Polymeric Chipstrate Build.

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3. S. E. Greer, "Low Expansivity Organic Substrate for Flip-Chip Bonding" – IEEE Trans. Components, Hybrids and Manufacturing Technology. *CHMT 2*. pp 140–144, 1979.