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MULTI-LAYER 2 MIL LINE TECHNOLOGY

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Multi-layer 2 mil line technology has been increasingly required for VLSI and very high speed logic devices. This technology makes it possible to shorten the length of interconnection lines between VLSI silicon chips. Thus the signal propagation delay on the transmission lines can be minimized.

Multi-layer 2 mil line technology research history, the new method and usages are discussed in this paper.

1. INTRODUCTION

The purpose of modern VLSI manufacturing industry is achieving high speed operation, high density integration and economy. VLSIs have been developed for all of these purposes. The Ga-As MES FET, for example, was developed for high speed operation. The physical size of VLSI chips will not increase proportionally as the number of the gates increases owing to super fine line interconnection on the silicon chip. The number of VLSI output pads is proportional to the square root of the total gates contained within the random logic device. This stipulation is known as Rent's Rule. This means a VLSI has many more pins than an MSI or an LSI.

The number of VLSI pins could be considered as being over 120. The occupied area for several package categories vs. the number of output pins is shown in Figure 1. In Figure 1, A shows the area of a single silicon chip. H indicates DIP package area. I represents the area for QUIP whose four sides have 0.1″ pitch pins. G corresponds to a 0.05″ pitch pad flat package. E shows the area of a chip carrier with 0.05″ pitch I/O pins on four sides. D represents the area of a 5 mil line

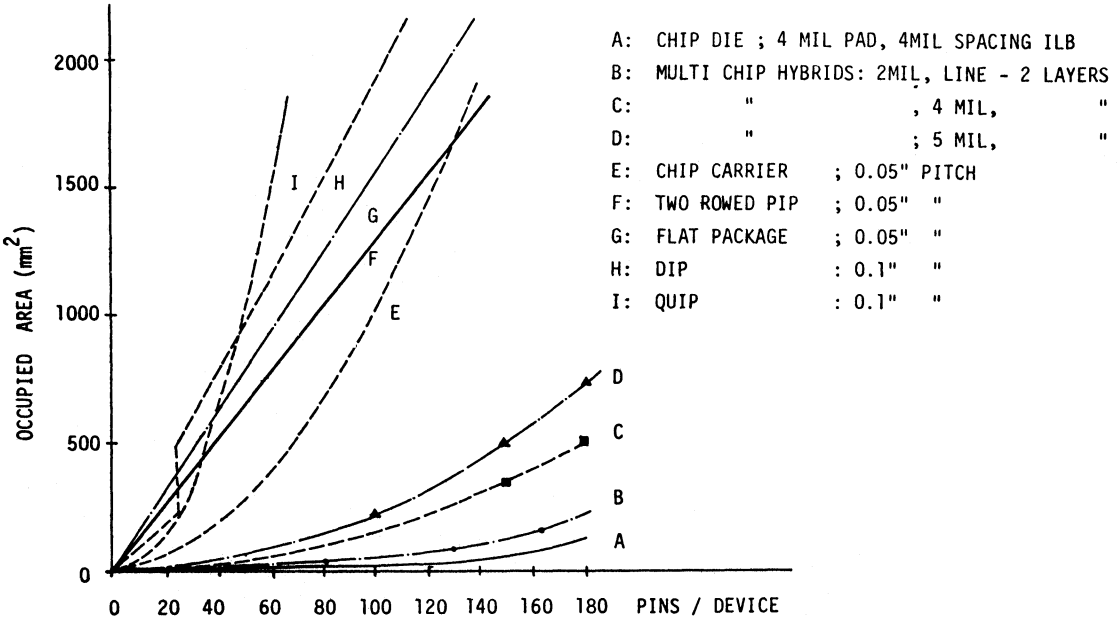


FIGURE 1 Occupied area by different types of chip dice containers.

2 signal layer multi chip hybrids, C represents the area of 4 mil line 2 signal layer hybrids. B indicates the area of 2 mil line 2 signal layer hybrids.

Even in the range from 30 to 60 pins, the H area is much larger than that of A, B, C or D. E area is smaller than H, I, G or F areas. Furthermore, D and C areas are smaller than E. However, A and B areas don't differ too much from C and D areas. So, in this pin number range, E, D and C categories have adequately high population densities.

In the consecutive range between 60 to 120 pins, E loses its advantage, because E is close in size to F, but F has the advantage of being easily handled. Now D and C are much smaller than E or F. Furthermore, B is smaller than C or D.

In the range from 120 to 180, B is distinctly smaller than C or D and very close to A. The length of interconnections between chips which occupy the smallest area can be minimized. Thus the propagation delay can be also minimized. Two mil line 2 layers hybrid, referring to B, thus can minimize the propagation delay on interconnections between silicon chip. This becomes most evident in the pin number range over 120, referring to VLSI. Figure 1 shows that interconnection density of 2 mil line 2 layers hybrid is distinctively the highest in the pin number range over 120.

1.1 2 Mil Line History

The practical limitation of screen printed fine line can be noticed to be 4 mils. In order to establish a method for lines whose width are less than 4 mils, several kinds of method have been examined. Especially analogous technology to interconnection on IC devices, namely the total thin film method, has been discussed. The advantage of thin film is the capability of resolving the pattern finely and the inverse of it is the inability to repair a faulty unit. In the semiconductor industry "yield" of very small chips has been emancipating them from the necessity of repair.

However hybrids require large expensive areas which cannot be thrown away even if they have several defects. This is why total thin film hybrid is not economical. Furthermore thin film dielectric involves several technical problems, for example the discrepancy in sputtered dielectric film thickness at the edge of a several micron thick gold line or a thermal expansion mismatching between sputtered dielectric layer and metal on a ceramic substrate. Multi layer total thin film hybrid thus has not become popular.

The first challenge to 2 mil line system using thick film material may be FODEL (DuPont). 2 mil line and 4 mil via system can undoubtedly be achieved with this technology. This system would become popular, if FODEL were inexpensive and material selection were flexible. However, the basic idea of FODEL, which is to make a thick film pattern by the photolithographical method, is now becoming popular.

The new photolithographical method, which is different from FODEL, has been invented by Y. Nishi of Toshiba.[1] There are two methods. One is as follows.

1) Depositing a paste material all over the effective surface area.

2) Drying the paste.

3) Depositing a photosensitive resin on the paste.

4) Exposing said photosensitivity resin selectively to light.

5) Removing the unnecessary parts of the photosensitive resin and of the paste.

6) Firing the paste material attached to the substrate. Examination of this method was reported.[2]

Another method is as follows.

1) Depositing a photosensitive resin on a substrate.

2) Exposing said photosensitive resin selectively to light.

3) Removing the unneccessary parts of the photosensitive resin.

4) Filling a paste for thick-film circuit use into the openings from which the photosensitive resin was removed.

5) Removing the remaining photosensitive resin.

6) Firing the filled paste material. The tests on this method have been made.[3]

Besides the photolithographic thick film process, another technology, based on a different idea, which is the use of thick film compatible thin film, namely fireable thin film, is reported. The basic idea of fireable thin film is that even the evaporated metals can be compatible with firing process, since the screen printed metals are compatible with the firing process. If the metals combination of evaporated thin film is very similar to that of screen printed thick film, the thin film can be fired.

The first fireable thin film report is concerned with the Cu-Au conductor. Its adhesion mechanisms involves forming copper alminate. The pertinent theory is similar to the chemical bond for thick film.[4] The two metal system, such as chromium and gold, annealed at 900°C in Ar is reported.[5] Gold selective plating over Ti/Ni evaporated film was reported to be fireable. These are aggressive researchers and they are pioneers in this field.

2. PROCESSING AND APPLICATIONS

Two kinds of 2 mil line technology are introduced here. One involves etching fired thick film. Another involves fireable thin film.

2.1 Etching Fired Thick Film

Fired thick film can be considered as a bulk metal on a substrate. Photo resist deposited over it, exposing and developing the photo resist and etching off unneccessary parts of it makes it possible to fabricate a 2 mil line device. Figure 2 shows the etched Au or Ag/Pd 2 mil line thick film using etchants A, B, C and D.

The present limitation to this technology is the 2 mil line. Even in this case, printing conditions must be optimized for successful device configurations using the 2 mil line interconnections.

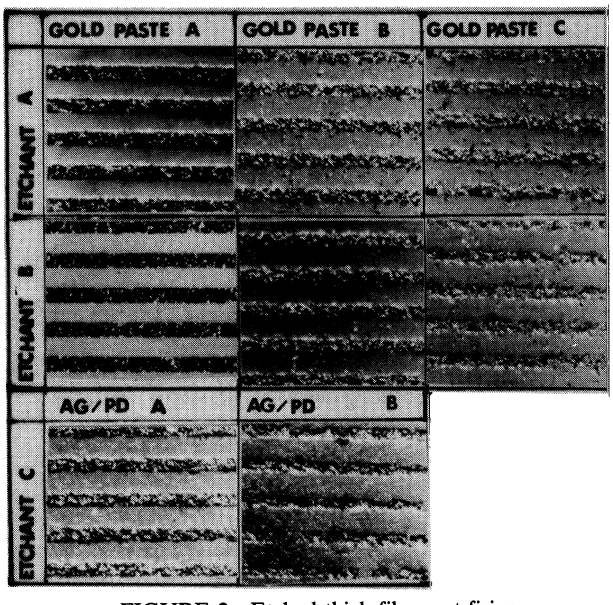


FIGURE 2 Etched thick film post firing.

2.2 Fireable Thin Film

In order to obtain narrower conductor lines, the thinner film is necessary. The printed and fired thickness of thick film conductor is limited in thickness to half mils so the width of thick film is limited to 2 mils. Since the thickness of evaporated thin film can be reduced to several microns, then the thin film can be more finely resolved than thick film by etching.

If the thin film is compatible with firing process, multilayer very fine line substrate (line width is less than 2 mils) is obtainable by employing thick film dielectric paste. The thin film being compatible with firing is defined as fireable thin film here. The fireable thin film process is

1) evaporating at least two metals, one of which must have high oxidization free energy to obtain high adhesion strength to a substrate and the other which must be noble to prevent the metal by oxidization;

2) depositing photosensitive resin over it;

3) exposing and developing with the desired pattern;

4) etching it and then firing it.

It can be very finely resolved with the photolithographic method. The film is repairable with thick film conductor or metal-organic paste. The film is compatible with thick film dielectric paste, thus the fired film system becomes water-proof.

On the other hand, the film must meet the following requirements:

1) The conductivity shall not change after several firings;

2) The film shall have sufficient adhesion strength to the foundation;

3) The film shall not form any bubble nor cause any conductivity change after being covered with dielectric paste.

The parameters to meet these requirements are kinds of metal, metal thickness, ceramic substrate, dielectric paste material, via fill material, firing temperature and firing time.

All the data cannot be described here, only characteristic data are shown in this paper.

First fired film conductivity is discussed. Metals which have high oxidization free energy and have some possibility to form crystal structure with Al_2O_3 or SiO_2 are listed in Figure 3. The best conductive oxide is CrOx, next is CuOx, FeOx and so on. The worst two are Ti and Mo. It is anticipated that fired film has the high oxide resistivity. $Cr^{1000A^\circ}/Au^{3000A^\circ}$ are compared to show the resistivity change trend caused by firing. The former was formed to have 18.7 Ω/cm (length) ·100μ (width) resistivity and the latter has infinite resistivity The trend seems to meet the theoretical prediction by rule of thumb. However, Figure 4 shows that, even in the Ti/Au case, if the gold is sufficiently thick, resistivity decreases after firing. This means fired thin film is more promising than was anticipated.

Next, a check was made to determine how the adhesive metal difference influences conductivity.

	Conductivity $(\Omega cm)^{-1}$	Oxidization free energy (K cal 900°C)
CrOx	$10^{-1} \sim 10^{7}$	-130 (Cr_2O_2)
CuOx	$10^{-3} \sim 10^{5}$	-40 (Cu_2O)
FeOx	$10^{-14} \sim 10^{5}$	-80 (Fe_3O_4)
CdOx	$10^{1} \sim 10^{4}$	-47 (CdO)
VOx	$10^{-2} \sim 10^{4}$	-165 (VO_2)
ZnOx	$10^{-2} \sim 10^{4}$	-115 (ZnO)
NiOx	$10^{-1} \sim 10^{3}$	-65 (NiO)
TiOx	$10^{-12} \sim 10^{0}$	-195 (TiO)

FIGURE 3 Electrical conductivity and oxidization free energy of adhesion metal oxide.

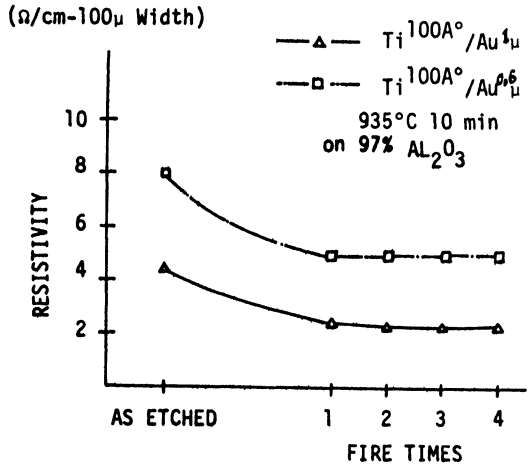


FIGURE 4 Conductivity change by firing.

Figure 5 shows the resistivity of Ni/Au, Mo/Au, Mn/Au on 97% alumina after 935°C firing for 10 minutes. The resistivity of all metal in Figure 5 is extremely stable.

However, as shown in Figure 6, once metals are covered with dielectric paste, the trend completely changes. Not only covering dielectric but also ceramic material influences the conductivity (Figure 7). In this case, ceramic B can be recognized as being stabler than ceramic A. Figure 8 shows how the firing temperature influences the resistivity. The resistivity is inversely in proportion to firing temperature. Sintering effect seems to reduce the resistivity, since the evaporated film is microscopically porous. However, the intrinsic cause has not been established. Another important consideration is the fired film adhesion strength. Figure 9 shows that adhesion strength depends on firing temperature and the ceramic material employed.

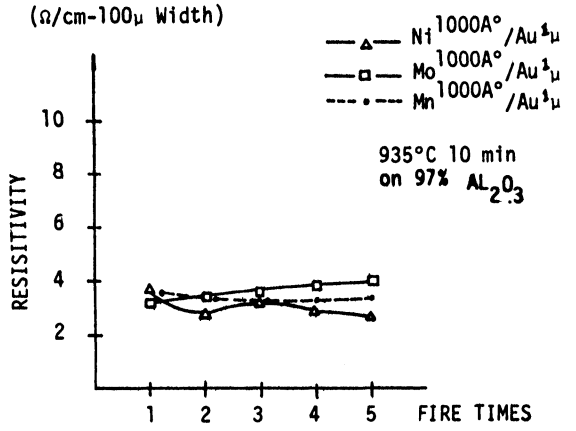


FIGURE 5 Conductivity change of different adhesive metal.

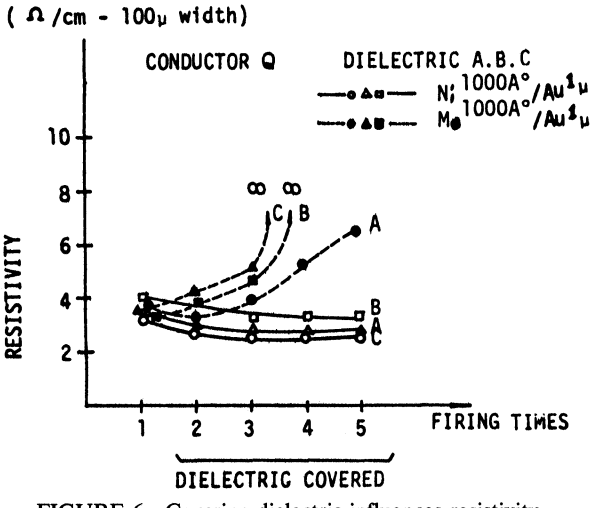


FIGURE 6 Covering dielectric influences resistivity.

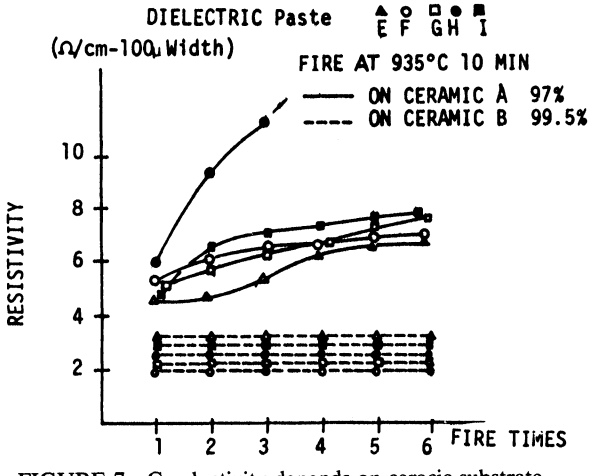


FIGURE 7 Conductivity depends on ceracic substrate, covering dielectric and firing times.

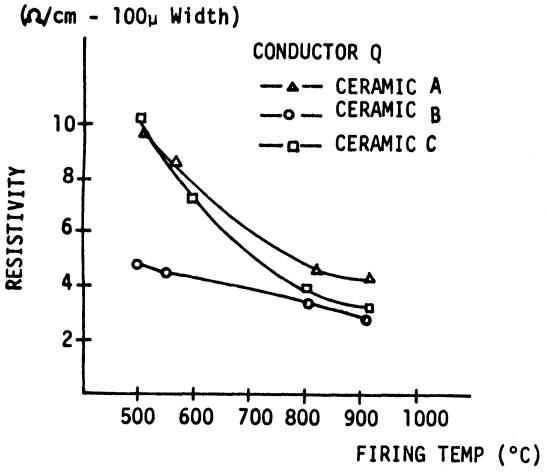


FIGURE 8 Conductivity change vs. firing temperature.

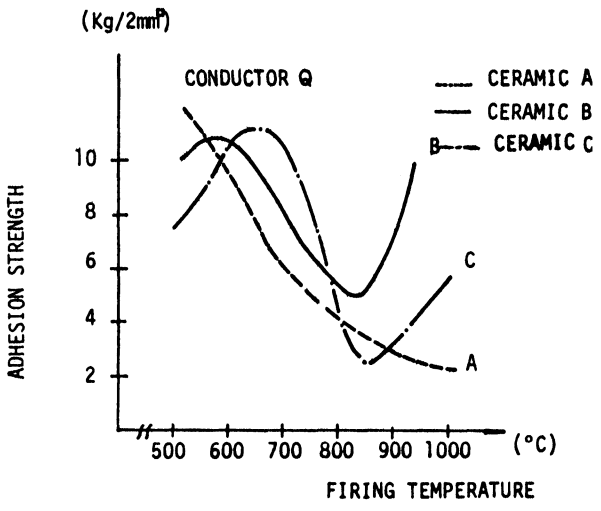


FIGURE 9 Adhesion strength depends on firing temperature.

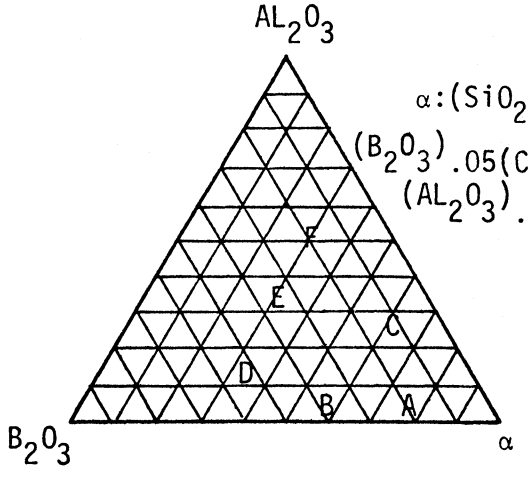


FIGURE 10 Dielectric material composition.

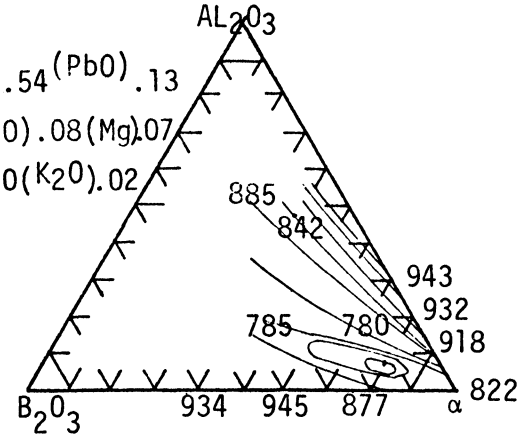
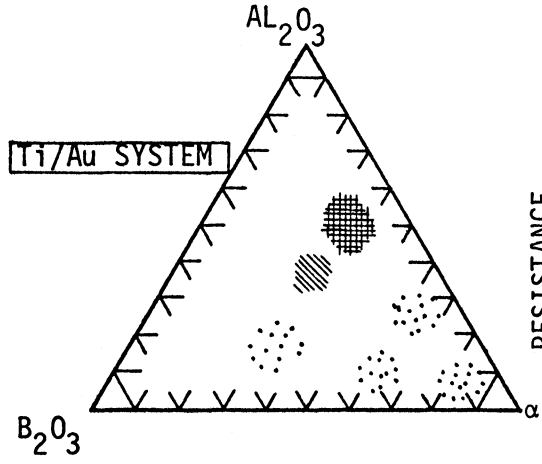


FIGURE 11 Softening temperature of materials.

The last consideration concerns the second conductor on the dielectric layer. The requirement for this film is similar to that on ceramic substrate. However, its physical or chemical reaction is much more complex. The dielectric foundation reacts on the film. Thus, resistivity changes easily.

In order to clarify the relationship among Ti, Cr, Ni, Au and dielectric materials, an inhouse paste, whose composition is known, was used. Figure 10 shows the dielectric material composition. Softening temperatures are shown in Figure 11. Results are shown in Figure 12. This shows that the resistivity change does not depend on softening temperature, but primarily depends on dielectric material, especially Al_2O_3 content. Second resistivity change also depends on adhesive material. For example, Cr is most stable and Ti is the worst.

What is the cause of resistivity increase? Figure 13 shows the Ti/Au conductor after being fired 5 times. The conductor in Figure 13 is very porous. Adhesion metal diffusion to Al_2O_3 particle surface weakens the Au adhesion to the dielectric. This adhesion loss causes Au film condensation during firing, then causes the Au path to break. In these cases all of the conductor



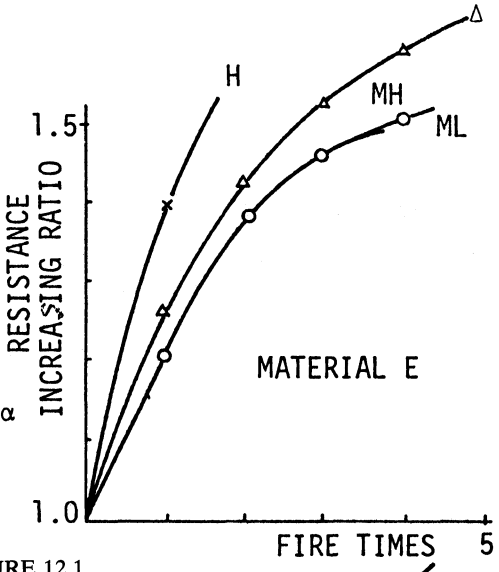
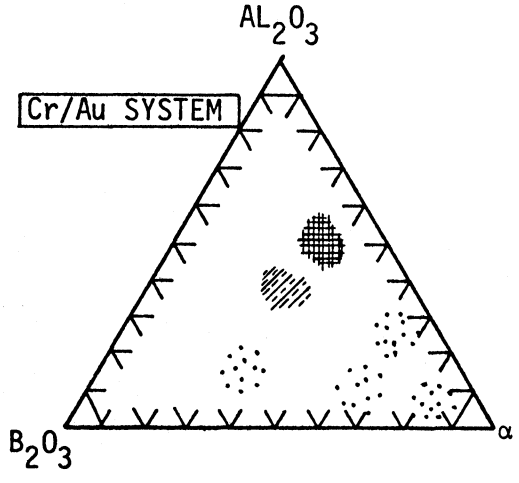


FIGURE 12.1



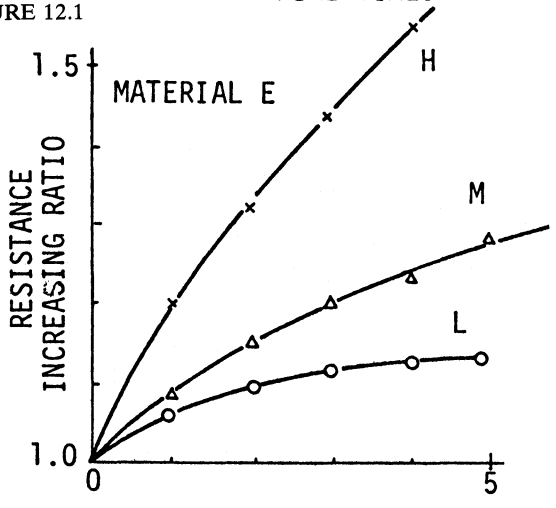
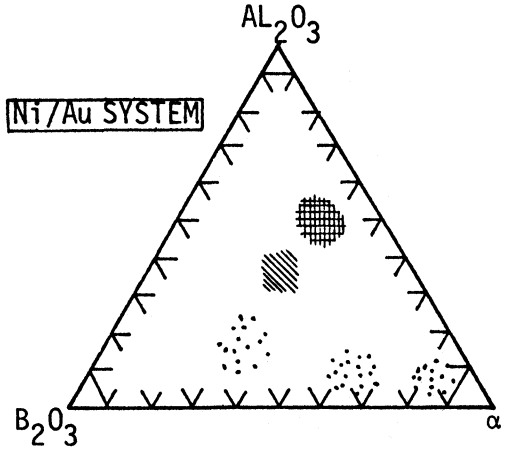


FIGURE 12.2



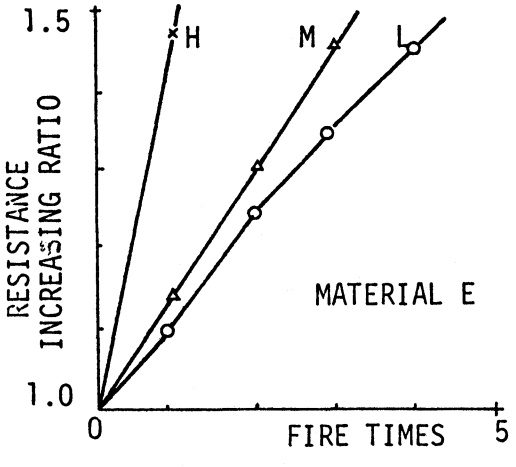
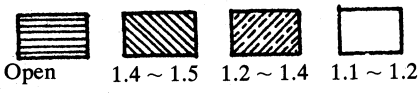


FIGURE 12.3

(3) Resistance change post 3 times fire.



(6) Resistance increasing ratio vs. fire times.
H: 930°C; MH: 915°C; M: 900°C; ML: 885°C; L: 870°C.

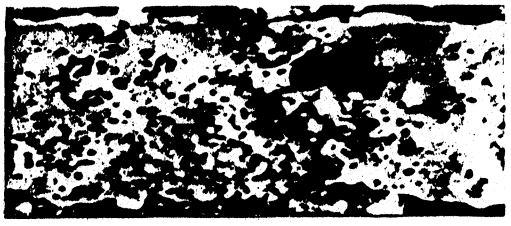


FIGURE 13 Fired porous conductor.

conductivity changes. However, a good combination of dielectric and conductor, which causes no change in conductivity, has been discovered and has been applied to practical use.

2.3 *Dielectric Layer (via Hole) and via Fill*

Dielectric material should be selected according to its compatibility with conductivity. Via hole and fill size is expected to be 3 mil to 4 mil for a 2 mil line. FODEL is fine for via hole processing, but not for via fill processing, since the large quantity of unexposed expensive gold paste has to be washed off. Thin film second conductor requires via fill, because if via fill were eliminated, a serious discrepancy in the film at the edge of the via hole would appear (Figure 14).

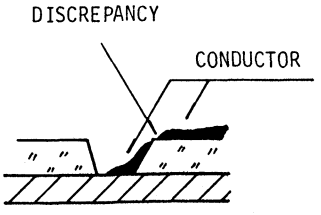


FIGURE 14 Open at the edge via hole.

A self aligned via hole-fill process has been developed. Figure 15 shows the following sequence. That is:

1) Printing and drying dielectric paste.

2) Depositing liquid photosensitive resin and drying it.

3) Laminating photosensitive dry film.

4) Exposing and developing which forms via hole.

5) Squeezing conductive paste into via hole.

6) Removing dry film and firing the paste.

In this case, liquid photosensitive resin and dry film should be solvent compatible. If the photo-sensitive resin is watersoluble, a surface activator is required to

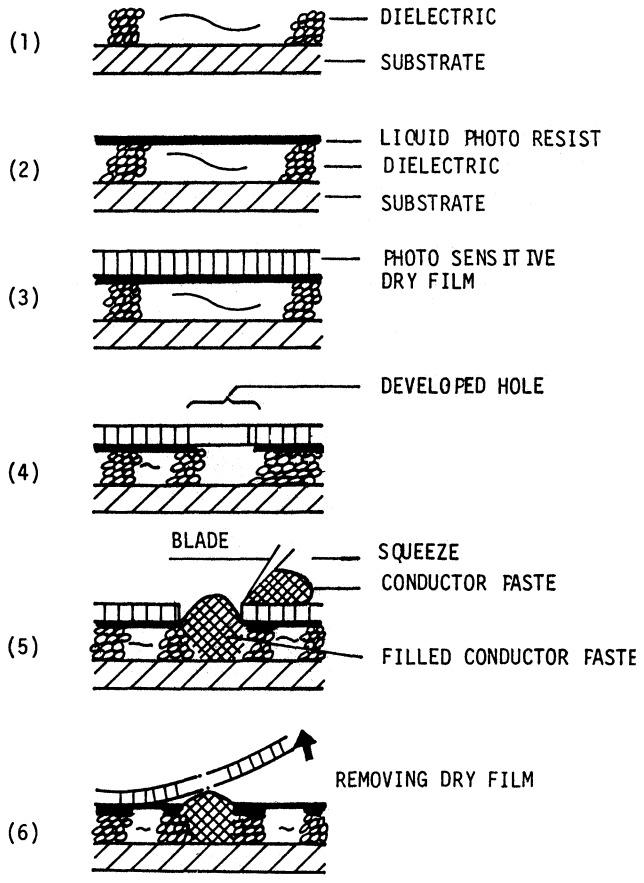


FIGURE 15 Self-aligned via hole/fill process.

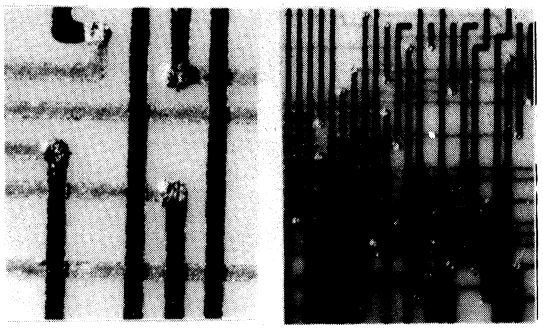


FIGURE 16 3 mil via connections between 2 mil lines.

tightly bond photosensitive resin to paste solvent compatible resin. The dry film should be selected to have adequate adhesion to dried liquid photosensitive resin, because the film must not be peeled during developing, and should be easily removed in process 6. Unsqueezed gold paste can be easily removed in process 6. Via fill paste should be carefully selected to

match dielectric paste, some dielectric material diffusion into via fill material during the firing.

A via connection photograph is shown in Figure 16.

2.4 *Practical 2 Mil Line System Usage*

The population density of the 12 bits microcomputer family is compared with printed circuit board, chip carrier 4 mil line hybrids and 2 mil line hybrids (Figure 17). Seventy-two 42 pin LSI and seventy-two 36 pin

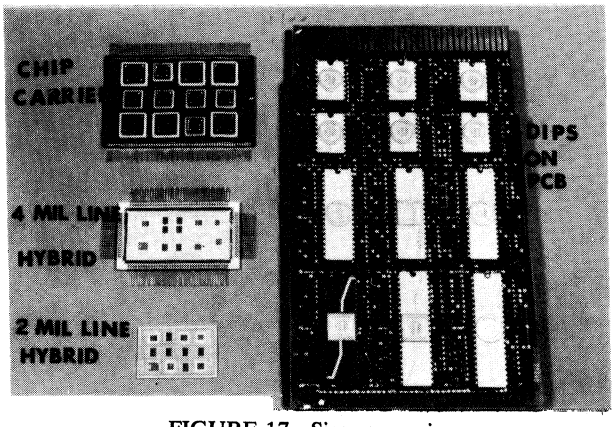


FIGURE 17 Size comparison.

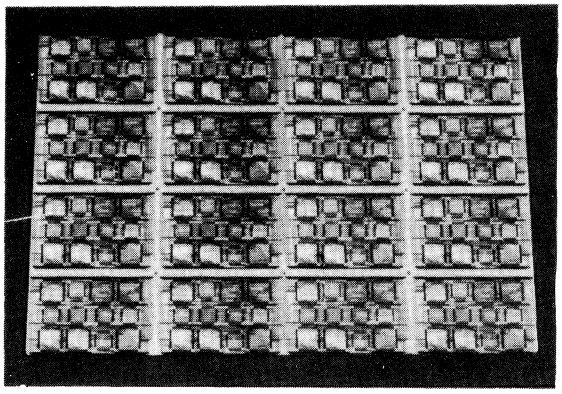


FIGURE 18 Multi-layer 2 mil line substrate.

LSIs can be easily constructed on a 100 mm × 150 mm alumina substrate with 2 mil line technology (Figure 18).

The most practical usage of eight and one half inch long 8 dots/mm thermal print head is shown in Figure 19. Using 2 mil line width with 2 mil space between

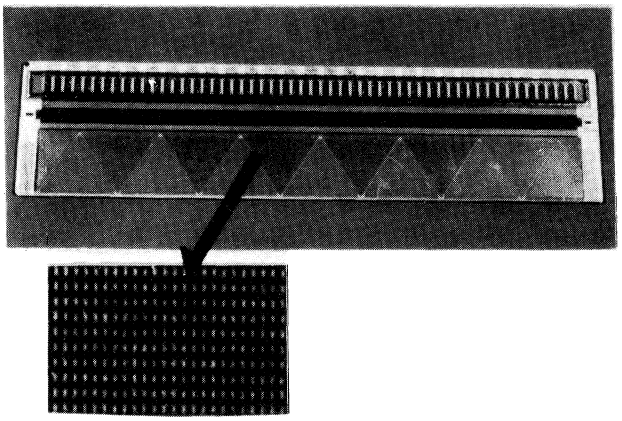


FIGURE 19 Multi-layer 2 mil lines in 8½ in long 8 dots/mm thermal print head.

lines, 1728 lines can be formed on a 233 mm × 55 mm substrate. These lines are covered with dielectric thick film. The product is waterproof.

CONCLUSION

Fireable thin film technology and via forming technology has made the 2 mil line system feasible. The multilayer 2 mil line system has been accomplished. This technology will be extremely useful in the coming VLSI era.

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