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SURFACE MOUNTING OF LEADLESS CHIP CARRIERS ON VARIOUS PRINTED CIRCUIT BOARD TYPE SUBSTRATES*

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The effect of extended thermal cycling on the reliability of joints between ceramic leadless chip carriers and various printed circuit board type substrates is examined. Test results indicate success in using ceramic leadless chip carriers on some styles of PCB.

INTRODUCTION

It is increasingly well accepted that the chip packaging revolution from dual in line to chip carrier (CC), tape automated bonding (TAB) and bare chip (BC) is under way, brought about by integration at chip level.

This change prompts the need for change, in turn, on the next level of interconnection. Broadly a need is seen for:-

– increased packing density of components.

– more control of electrical and other performance requirements.

Some previous work has indicated that PCB technology is capable of meeting the challenge of the new interconnection requirement at typically printed wiring board type costs.

PCB TECHNOLOGY

Conventional high volume technology will produce the following:-

Smallest Hole (min)	0.013"
Ratio – Board Thickness to Hole size (max)	5.4:1
Number of layers	14
Size (max)	Ca 24" x 24"
Dielectric Separation	0.0025" to 0.004"
Conductor Width (min)	0.006"
Gap width (min)	0.006"
Conductor Thickness (min)	0.0005"
Thermal resistance	Fair
Dielectric properties	2 to 5

Slight modification to manufacturing methods are required to better these figures – See Figure 1, but it is not the intention of this paper to elaborate further on these products rather just to draw attention to the dimensions and properties available which match the changing needs of interconnection.

*Paper originally given at the Technical Sessions Programme at Productronica, Munich, November, 1981.

TABLE I
Developing technology for PCBs

Smallest Hole (min)	0.004"
Ratio-Board Thickness to Hole Size (max)	3:1
Number of layers	6
Size (min)	6" X 8"
Dielectric Separation	.002"
Conductor Width (min)	.004"
Gap Width (min)	.004"
Conductor Thickness (min)	.0002"
Thermal Resistance	Good
Dielectric Properties	2 to 5

FIGURE 1 (Table) Developing Technology for PCBs.

DISCUSSION OF COEFFICIENT OF EXPANSION MISMATCH

One area however where there has been debate is the use of components with a particular coefficient of expansion on a substrate which has a different value for the coefficient. It is expected that you can accept the long term proven reliability of the PCB when dealing with leaded or socketed components and a great deal of activity is current in producing leaded or leadless plastic chip carriers which will similarly match the PCB. If however, continuing greater use of ceramic leadless chip carriers is made then it needs to be demonstrated that high joint reliability can be achieved.

The published work of Fennimore[1,2] Settle[3] Minnetti[4] and Lassen[5] are all reports of varying success on this subject. No one has attempted to explain why these empirical experiments should have been successful.

In practice the joint area is complex and multiple. The stress relieving properties of metallic leads or of solder pillars are well understood. Ductility. hardness, toughness and creep effects also play a part – See Figure 2.

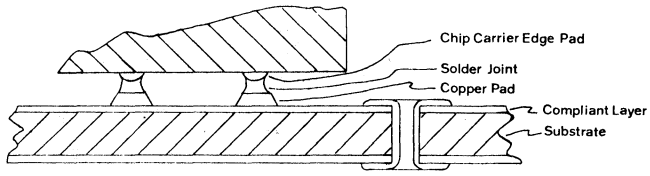
The joint may however be looked at in a more simplistic model; and the expected stress resulting from the thermally introduced strain may be considered as being proportional to the area of the joint, the difference in the coefficients of expansion, the temperature difference from the stable, no stress state, and an elasticity factor.

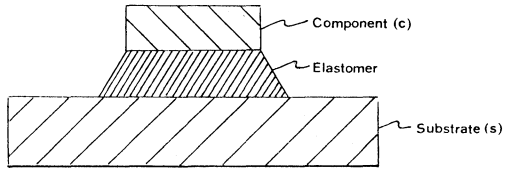
One ready way to ensure minimum stress is therefore to match the coefficients of expansion. Another is to limit the thermal excursions.

M. El Refaie[6] has demonstrated that the stress relieving effect of having an elastomer as part of the system will reduce the effective modules of elasticity for the combined system to a very low figure.

Additionally modern PCB substrates are not necessarily totally homogenous and many properties, including the linear coefficient of expansion (C.O.E.) can vary in the X, Y or Z directions in any plane.

If one considers the common woven glass reinforced epoxy resin substrate, (See Figure 3), then the glass reinforcement normally controls the *bulk* coefficient of expansion in the X and Y axes, being different in X and Y unless there is a perfectly balanced weave. However in the Z axis the C.O.E. tends to be nearer to that of the epoxy resin part of the substrate. If then one were to consider a resin free surface to such a substrate then the C.O.E. at the *surface* in the X and Y plane would relate more to the glass properties. If however there was to be a resin rich layer on the surface of the substrate then the C.O.E. of the surface would be nearer that of the resin.





$$\text{Force} \propto \text{Area} \times (\text{Coeff of Exp Diff}) \times \Delta T \times \frac{\varepsilon_s}{\frac{\varepsilon_s}{\varepsilon_c} + 1}$$

TYPICAL Coeff of Exp $10 \text{ to } 20 \times 10^{-6}$

$5 \text{ to } 7 \times 10^{-6}$

$\varepsilon_s \triangleq 0{\cdot}02 \text{ to } 0{\cdot}2 \times 10^{6}$

$\varepsilon_c \triangleq 10 \times 10^{6}$

FIGURE 2 Attachment Systems and Stress Module for Joining Components to PCBs.

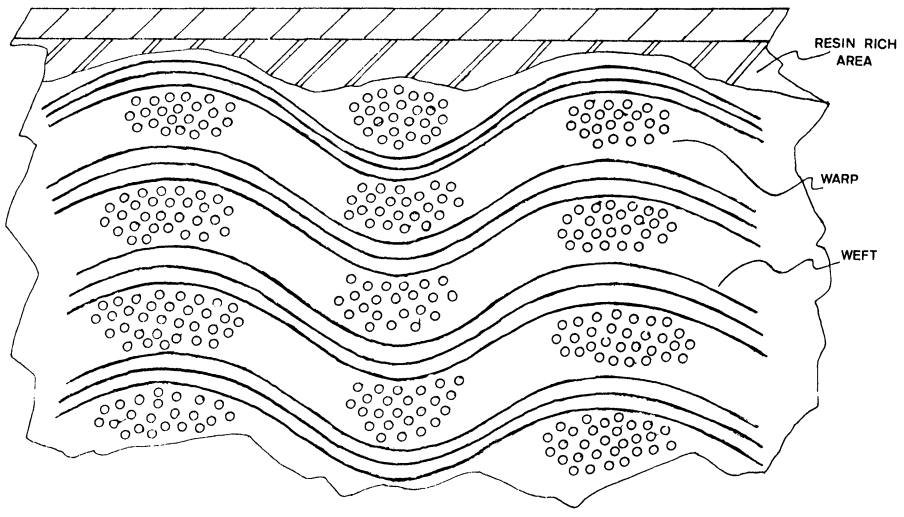


FIGURE 3 Typical Substrate Construction.

TABLE II

Chip Carrier Type					Cup Lid	Total Weight gms
Pads	Layers	Supplier	Part No.	Dimensions mm (excluding lid)		
16	1	3M	ST88-16CN	7.62 SQ x 0.51	Kyocera KKC-10180	0.26
28	1	Kyocera	CS52811	11.43 SQ x 0.56	Kyocera KKC-10188	0.65
44	1	Kyocera	CS54402	16.51 SQ x 0.81	Kyocera KKC-10183	1.36
52	5	3M	SR88-52BA	19.05 SQ x 1.91	STL flat lid	2.60

Lids sealed with Kyocera LTS (Low Temperature Sealant) Epoxy

FIGURE 4 Chip Carrier Details (Table).

Similarly however the modulus of elasticity of the combined system in bulk will not be the same as that obtained at the surface given either a resin free or resin rich zone.

Do such considerations work out in practice? Will a leadless ceramic chip carrier effectively float on the shock absorbing elastomeric layer? Does this concept help to explain some of the previously published results?

TABLE III

Type No.	Type	Suppliers Designation	Build Up	TEC PPM/°C
1	FR2 Phenol/Paper	Isola Supra-Carta 96 VO-350	1.6 mm Double Clad 1 oz copper	20 (80°C) (50/100 shrinkage at 120°C)
2	FR4 Epoxy/Glass	Double Clad Micaply EC818T/FR-4/GFN		10 warp 15 weft
3	Polyimide/ Glass	Double-Clad Micaply PG-418-T		9 (warp and weft close)
4	Modified Polyimide Kevlar	Howe HI-6938/120 Kevlar		5 to 5.5
5	Polyimide coated epoxy/ glass	Exacta Elastomer coated substrate-1 (ECS-1)	1.6 mm epoxy/glass clad one side 1 oz copper. Polyimide flexible coated other side and clad 2 oz copper	
6	Adhesive coated epoxy/ glass	Exacta Elastomer coated substrate-2 (ECS-2)	1.6 mm epoxy/glass adhesive coated both sides. Double clad 1 oz copper	
7	96% alumina ceramic	Coors ADS-95F	0.62 mm	6.0 (25-200°C)

FIGURE 5 Substrate Construction Details (Table).

MATERIALS ON TEST

Chip Carriers

Single layer construction ceramic leadless chip carriers were used. Four sizes, 16, 28, 44 and 52 pad varieties were obtained from 3M Co. and Kyocera, complying generally to JEDEC standard type MS004 0.050" centre leadless type C (See Figure 4).

Printed Circuits

Six different card materials were used together with an alumina ceramic control with matched expansion (See Figure 5).

TEST METHODS

Test Coupon Design

This was based upon the minimum size on which at least one of each size of carrier could be mounted. This also provided for ease of microscopic inspection of the solder joints from all angles. Carrier failure was defined as failure of a single joint. The coupon size was 95 x 50 mm and on the basis of equalising the total number of joints on test per carrier size, 3 x 16 pads, 2 x 28 pads, 1 x 44 pad and 1 x 52 pad carriers were used per coupon (pad sizes). (See Figure 6).

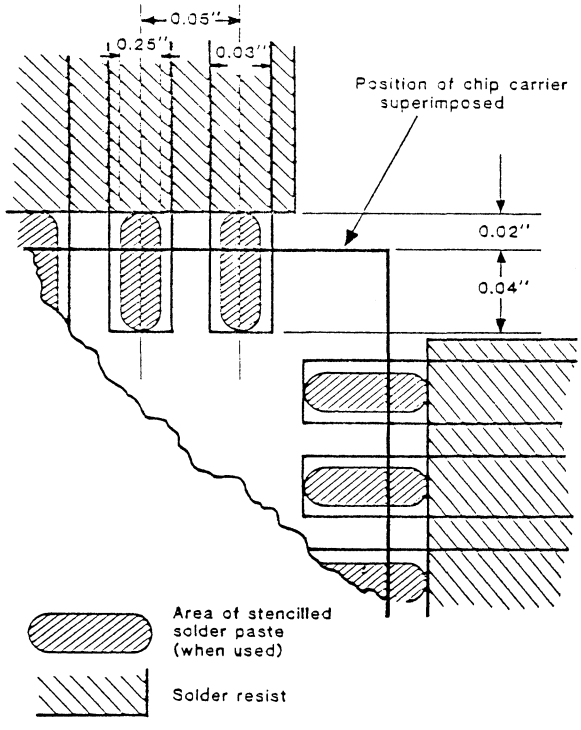


FIGURE 6 Solder Pad and Solder Resistor Dimensions showing one corner of foot print.

Thermal Cycling

There is much discussion as to the relevance of thermal cycling to real life conditions. The tests were conducted in a Montfort oven equipped with circulating fan and boost heater, the cooling being effected by liquid carbon dioxide. To ensure adequate temperature uniformity the area used within the chamber was restricted to one third of a square metre. The tests were conducted in accordance with MIL STD 833B method 1010.2 Condition B

i.e. – 55°C 10 minutes min
–125°C 10 minutes min
Time between extremes 5 minutes max.

In practice 2 cycles per hour were used.

Inspection

80 test coupons were mounted in 20 x 75 pin edge connectors in a frame. In operation a voltage was applied to each coupon in turn. Individual carrier selection was possible by a rotary switch leading to a LED display monitor. Joints were monitored and recorded at intervals, both electrically and by visual microscopic examination. Visual cracks in the solder were always preceded by surface crazing and no visually good joints were found be electrical failures.

SOLDERING

Soldering Equipment

Two varieties of soldering techniques were used, wave and reflow. A Schleuniger 'Jet' soldering machine – Type 6TF160 was used for the wave samples. The reflow soldering was performed in a Hedinaire VPD1 tank using a 3M Fluorinert 70 vapour.

Soldering Conditions

The finish on all the PCB style substrates was a fused layer of 63/37 tin/lead alloy which had previously been electroplated to 8 to 12 microns thick.

The ceramic control coupons were printed with Pd/Ag conductors and pads.

Reflow soldering After lid sealing the carriers were dipped in molten 60/40 tin/lead solder at 230°C for 1 second using an organic water soluble flux (Superior 30) and were subsequently washed, checked for leakage and for continuity of internal wire bonds.

Solder paste was added to half the coupons for reflow soldering stenciling and drying at 85° to 100°C. The carriers were brushed with Frys FR8/500B MA flux and dried.

Solder resist was applied to all coupons with the extra solder paste and half the coupons without the extra solder paste.

Wave soldering Fry's GR8/500B MA flux was brushed on the coupons with a soldering time of about 3 seconds and belt speed of 0.25 metres/second. The coupons were cleaned to remove flux residues.

Component attachment Before soldering all carriers were held in place by Eccobond 285 adhesive which had been applied using a DEK printing screen.

Solder thickness In practice the spacing between the carrier and the coupon was unaffected by the quantity of solder used or by the use of the solder resist pattern, being 0.125 mm of which 0.035 mm was due to copper tracking. Any extra solder at the joint formed a build up at the side channels of the carrier.

RESULTS

Visual

The results of the testing are summarized in Figures 7 and 8. Figure 7 gives the data obtained for different substrate materials and soldering method, using different pad sizes. Fig. 8 simplifies the data for one pad size.

The common sequence of failure was along one side of a carrier followed by the joints on adjacent sides beginning with those nearest the failed row. Individual joint failure was unusual. The coupons were inspected after 99, 135, 224, 270 and 432 cycles are displayed in Figure 6.

Discussion

(i) Of the conventional materials FR2 is relatively bad, whereas FR4 provides poor yet not exactly unuseable performance results particularly if more work were to be performed on soldering techniques etc. Polyimide/glass is marginally better than FR4.

(ii) There were no failures of connection for the matched expansion materials, i.e. the ceramic control batch or the Kevlar reinforced polyimide.

(iii) The two elastomer coated substrates demonstrates good results with no failures for the wave soldered samples.

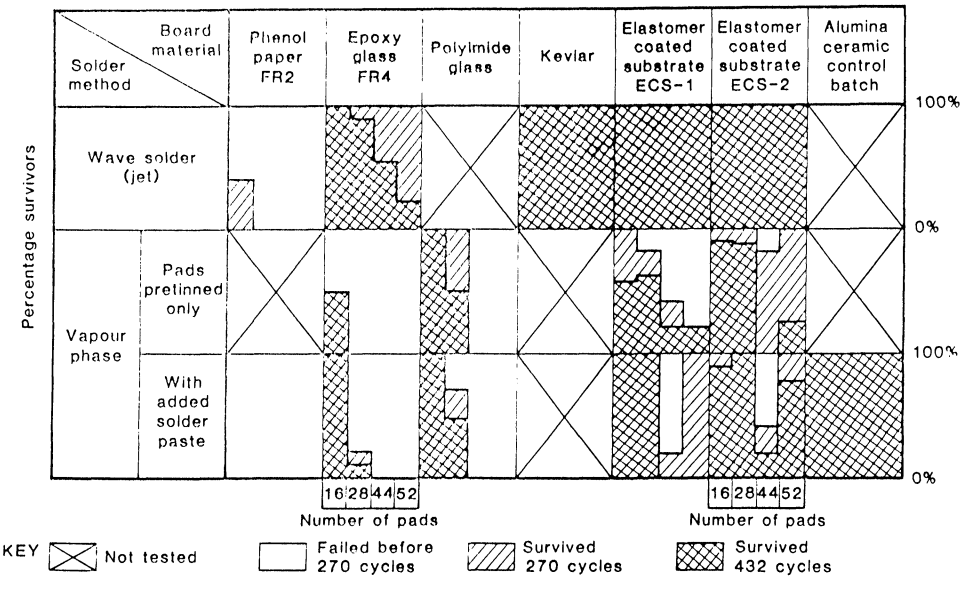


FIGURE 7 Thermal Cycling Performance – Variation with Substrate Material and carrier size (Temperature cycles –55°C to +125°C).

Percentage survivors

Solder method \ Board material		Phenol paper FR2	Epoxy glass FR4	Polyimide glass	Kevlar	Elastomer coated substrate ECS-1	Elastomer coated substrate ECS-2	Alumina ceramic control batch
Wave solder (jet)		0	87	☒	100	100	100	☒
Vapour phase	Pads pretinned only	☒	0	50	☒	60	85	☒
	With added solder paste	0	14	50	☒	100	100	100
Total percentage surviving		0	38	50	100	91	96	100

☒ Not tested

FIGURE 8 Thermal Cycling Performance of 28 Pad Carriers (432 cycles –55°C to +125°C).

(iv) Earlier failure of the larger carrier sizes confirms publishing work on fatigue and was noticeable particularly on the soldering techniques/materials which general gave the poorer results.

(v) The 28 pad size was less critically effected by process variations.

(vi) The 55 pad carrier fared relatively badly compared to other carrier sizes. It was noted that these particular carriers had a smaller metallised edge radius which effectively reduced the volume of solder related to each individual pad.

(vii) Wave soldering gave better and more consistent results.

(viii) Reflow soldering gave relatively poorer results particularly when there was no added solder paste.

CONCLUSION

Leadless chip carrier mounting on to various substrates was performed and thermally stressed to simulate life conditions.

The following conclusions were reached.

(i) Limited life is possible on conventional printed circuit board materials and this solution will be within normal price and availability.

(ii) Excellent life is possible on certain expansion matched substrates but these may be expensive solutions.

(iii) Excellent life is also possible using certain elastomer coated substrates manufactured using relatively conventional methods and materials and within the normal price range and availability.

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