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# DENSITY UPGRADING IN TAPE AUTOMATED BONDING†

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Bonding technique developed by CII-Honeywell Bull. The paper describes the geometry of bonding pads at the chip level, the design and realization of the corresponding high density 35 mm tape and the interconnection of the chips on the tape (inner lead bonding – ILB). Two alternatives of chip mounting on the substrate are also mentioned.

## DENSER PACKAGING

The continuous progress of microlithography techniques allows one to put more and more active elements into a given silicon real estate. The increased internal complexity of the very large scale integrated devices requires an increasing number of communication paths with the external world. Thus a new challenge is arising because of VLSI packaging techniques. Today requirements for bonding dozens of connections onto a single chip on advanced parts are rapidly being turned into a requirement for bonding hundreds of connections onto a single device in the very near future. The availability of interconnection techniques capable of a high density at the first packaging level, i.e. between the chip and its immediate surrounding is becoming a key issue in the construction of complex electronic assemblies.

Consider as an example a chip design where all the logic content is contained in a given active area, communicating witht the outside through a fixed number of pads (Fig. 1).

From figure 1 it can be readily seen that in the case 1A the total chip size is dominently determined by the density of bonding pads. In case 1B the pad density is increased, resulting thus in a total chip size better tailored to the active area. When considering devices with a number of interconnection pads around 200, a peripheral pad arrangement with a 120 micron pitch around an active area of 6.6 x 6.5 mm will result in a device of about 50 $mm^2$; the same case with a 180 micron pitch would lead to a device exceeding 100 $mm^2$. It is obvious that using more than twice the silicon area would have a dramatic effect on device cost and performance.

## HIGHER DENSITY BONDING

Recognizing the need, for higher density at the first level of packaging, each of the bonding techniques in industrial applications is involved in the effort to push further the present state of the art.

The flip chip concept extended by IBM on the whole chip surface[1] is capable of achieving a very dense first level packaging. To be employed to its full capability in

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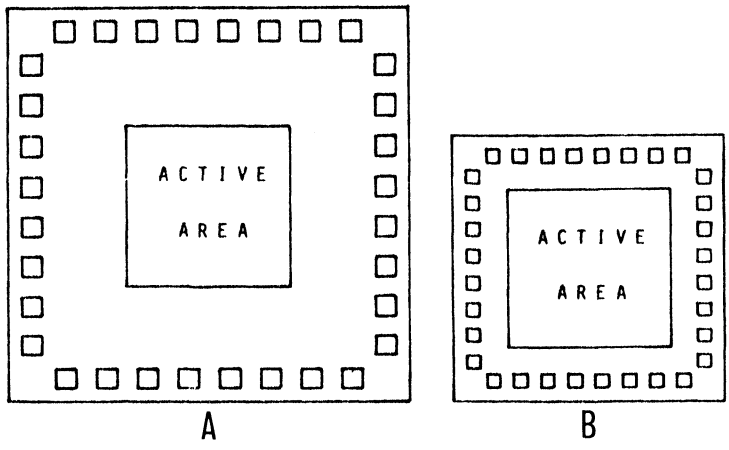



FIGURE 1 Bonding pad density impact on chip size.

terms of interconnections and thermal efficiency it has to be used in the complex environment of the thermal conduction module.[2]

The wire bonding technology is also achieving a very significant progress in density increase through development of sophisticated automatic bonders. Although a 180 micron pitch between chip pads is considered as a practical limit in the case of gold wire thermo-compression bonding, HITACHI is currently using in production, the 135 micron pitch aluminium wire ultrasonic bonding.[3]

Finally, the Tape Automated Bonding is another first level packaging technology with which a high bonding density can be obtained.

## DENSER PACKAGING USING T.A.B.

The pad arrangement on chips for TAB used in present current production has been typically made with a 180–120 micron pitch, as shown in figure 2.

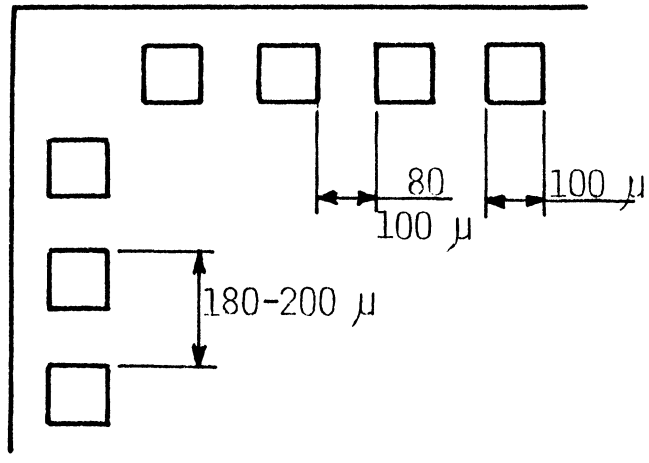



FIGURE 2 Typical bonding pad arrangement for present TAB bonding.

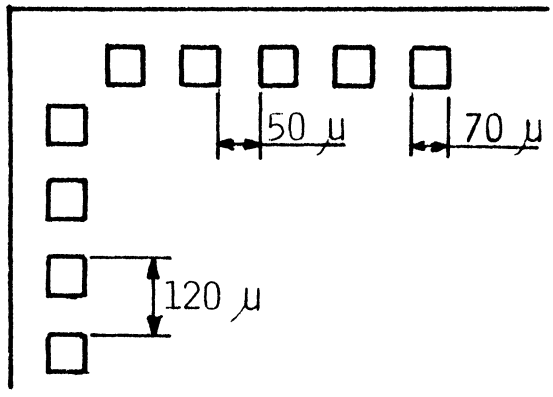
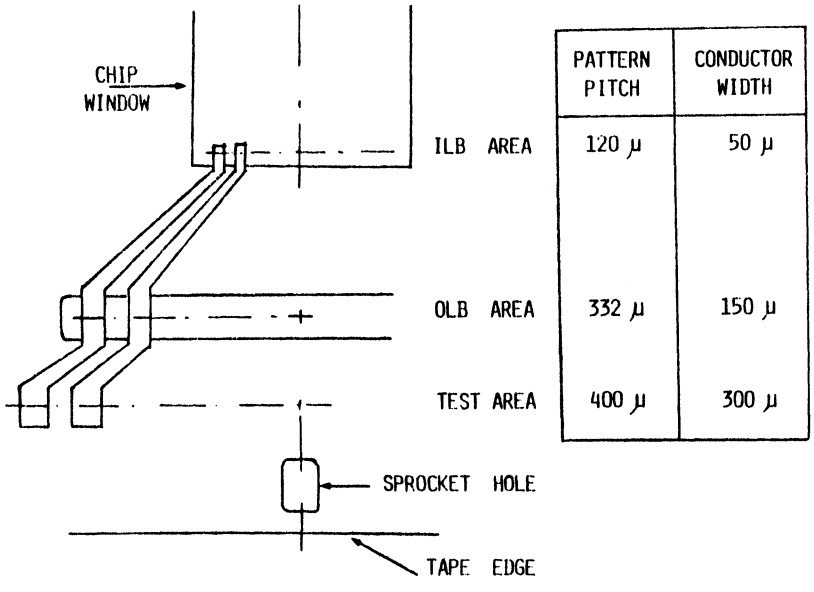



FIGURE 3 Typical bonding pad arrangement for VLSI TAB bonding.

As a first step of density increase in TAB a 120 micron pitch shown in figure 3 was used. It allowed of the placement of a total of 176 bonding pads distributed on the periphery of an approximately 5.5 x 5.5 mm chip.

The pitch of the pads on the chip corresponding to the density of inner lead bonding was the first of various design parameters to be taken into account, in order to generate the tape pattern design. CII-Honeywell Bull have decided to stay with the standard 35 mm tape width. Figure 4 shows one of the different possible, constructed configurations with an outer lead bonding of 332 micron pitch and pads for test purposes, which allowed of device test prior to the first level packaging.

After bonding on the tape the VLSI devices could be transferred into individual packages or mounted directly on a multichip substrate. In this second case a lead forming may be necessary and could be successfully performed in at least two ways which were developed and successfully demonstrated. Figure 5 shows a test chip with 176 bumps bonded after lead forming.




| PATTERN PITCH | CONDUCTOR WIDTH |
|---|---|
| 120 µ | 50 µ |
| 332 µ | 150 µ |
| 400 µ | 300 µ |

FIGURE 4 Main geometrical characteristics of lead configuration on 35 mm tape.

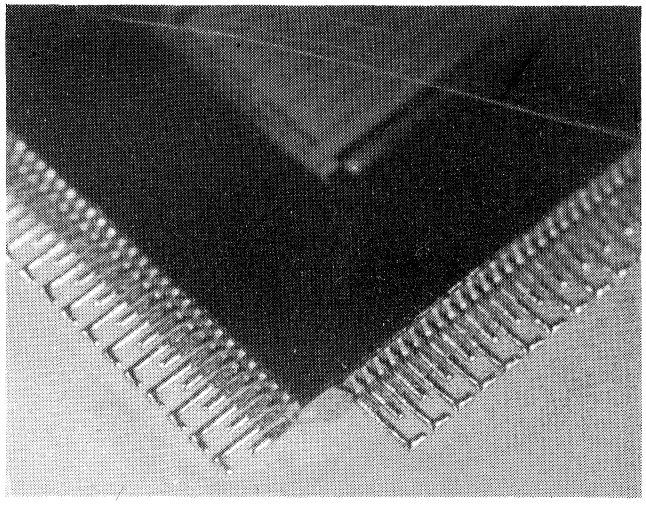


FIGURE 5 Partial view of a TAB chip bonded on substrate after lead forming.

The lead forming could be avoided when a "flip TAB" bonding approach was used. This approach (Figure 6) consisted in placing the active side of the chip towards the substrate into the electrically insulating adhesive material with a good thermal conductivity.

## MATERIALS, EQUIPMENT, PROCESSING

The dense TAB assembly was achieved by using materials and equipment equivalent to those applied for conventional TAB bonding, previously described.[4]

Some changes were necessary in the viewing optics as larger chip size and higher pad density required a larger field of observation and higher alignment accuracy.

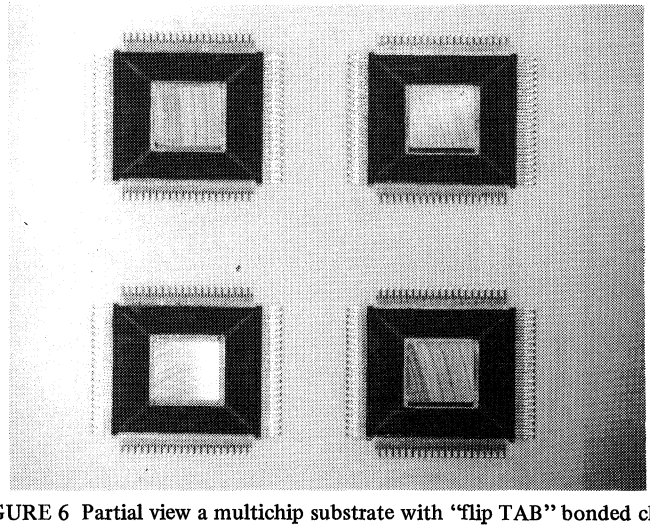


FIGURE 6 Partial view a multichip substrate with "flip TAB" bonded chips.

Some modifications were also introduced into the tape etching process in order to be able to achieve consistently the resolution necessary to meet the inner load bonding density.

## CONCLUSION

Tape automated Bonding (TAB) is one of the possible ways by which chips with increased bonding pad density can be assembled. The 120 micron pitch between centers of adjacent pads described in this paper is not the ultimate number which can be achieved with this method. The possibility of gang bonding and the lack of limitation on lead length between the chip and the package are considered as the main advantages of Tape Automated Bonding, together with the possibility of device testability at the tape level.

These advantages are to be taken into balance with the constraint of special bump metallurgy on bonding pads required by TAB.

## REFERENCES

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