

MID-FILM INTERCONNECTS FOR MULTILAYER MICROCIRCUIT PACKAGES

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The mid-film^R process has been developed to combine the photolithographic capability of thin film technology and the low cost, non-vacuum processing of thick film technology. In this paper, we present results on the characterization of mid-film gold for multilayer applications. The effects of various processing parameters on the properties of the conductor were investigated to establish optimum processing conditions on alumina and dielectric-coated alumina substrates. The use of a resin thickness in the range from 5 μm to 15 μm and firing temperatures from 750°C to 1000°C produced conductor lines with sheet resistances less than 4 $\text{m}\Omega/\square$, and with adhesion strengths capable of withstanding a pull force of 2.3 Kg exerted on a 2.03 mm \times 1.03 mm area. The conductor lines exhibited stable resistances upon several firings at 920°C. The ultrasonic bondability of 25 μm (1 mil) aluminum wire to the mid-film gold was observed to withstand pull forces of 7.3 ± 1.5 g before breaking the bond. In addition, it was confirmed that the resolution limit of the mid-film conductor is 50 μm for line widths and spaces. Furthermore, the prototype fabrication of a multilayer memory package has been successfully demonstrated using a combination of both mid-film and thick film processes. The finished packages were free of electrical shorts and conductor discontinuities and the resistance of the mid-film conductor lines was well within the required design specifications.

1. INTRODUCTION

In previous papers¹⁻³ we have introduced the mid-film (MF) process as a new technique to fabricate high density interconnects in hybrid microcircuits. The process was developed to combine the photolithographic capability of thin film technology and the non-vacuum, low cost and large area capability of thick film technology. In the MF process, the substrates are coated with a thin layer of an organic photosensitive resin which is then exposed to UV light through a positive photomask. The exposed portion of the MF resin crosslinks and becomes particle non-receptive. A solid powder of metallic conductor and glass frit is then applied to the surface and becomes physically embedded in the unexposed portion of the light-sensitive resin. The process is completed by firing the substrate at a high temperature to remove the organic resin by oxidation and bond the powder particles to the substrate through sintering and fusion mechanisms.

The present investigation was carried out to explore the feasibility of using MF conductors for hybrid-multilayer applications. In this case, high electrical conductivity, good solderability and bondability and good adhesion are the basic requirements imposed on the conductor. The characterization was accomplished by varying the MF parameters and observing the effects on the properties of MF-Au conductors printed on alumina and dielectric-coated alumina substrates. The fabrication of a multilayer memory package is presented as a practical demonstration of combining mid-film and thick film processes.

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^RTrademark of the Ferro Corporation, Cleveland, OH.

2. MATERIALS AND PROCESSING PARAMETERS

2.1 *Substrates*

Standard thick film 96% alumina substrates (AlSiMag #614, supplied by 3M) were ultrasonically cleaned in freon solvents followed by firing at high temperature, typically 900°C. The use of contaminated substrates may result in poor film adhesion.

Dielectric-coated substrates were prepared by screen printing and firing DuPont 9950 thick film dielectric on alumina substrates. As recommended by the vendor, the dielectric film was printed using a 200 mesh stainless steel screen, dried at 90°C for 10 min and then fired in a belt conveyor furnace using a 60 min cycle with 10 min at a peak temperature of 920°C.

2.2 *MF Resin and its application*

A positive acting photoresist resin was supplied by Ferro corporation. It was diluted with two parts by volume of 1-1-1 trichloroethane to one part resin and applied to the substrate by a variable speed motor-driven pneumatic sprayer head. The sprayer was set at a distance of 15 cm from the substrate and the scanning speed was set at 5.3 cm/s in the horizontal and 0.4 cm/s in the vertical direction. In a single pass, this set-up produced a uniform resin layer having a thickness of $6.0 \pm 0.6 \mu\text{m}$.

2.3 *Resin UV exposure*

A Tamarack model 143-B alignment and UV exposure system was used. The resin layers were exposed through positive photomasks for an average time of 10 s at a power density of 20 mW/cm². The photomask-to-substrate separation distance was fixed at 100 μm .

2.4 *MF Powder and its application*

Preliminary experiments showed that the MF conductor powder must be compatible with the thick film dielectric materials used in the multilayer circuit. To achieve optimum compatibility with DuPont 9950 thick film dielectric, we used MF-Au conductor powder extracted from DuPont 9791 thick film paste. To this end, the Au paste was dried in air at 110°C for approximately 30 min and then fired in a belt conveyor furnace in a 60 min cycle with a 10 min soaking period at 400°C. The fired ink formed a brittle aggregate which was ground and sieved through a 5 μm mesh screen. The powder was then applied to the resin-coated substrates using a soft cosmetic puff.

2.5 *Firing conditions*

The MF-Au conductors were fired in a standard thick film belt conveyor furnace. Unless otherwise specified, a 60 min cycle was used with 10 min at a peak temperature of 920°C.

3. FILM PROPERTIES

3.1 *Structural and geometrical characteristics*

In agreement with previous work³ the thickness and packing density of MF conductors were found to depend on the resin thickness. As shown in Figure 1, increasing the resin

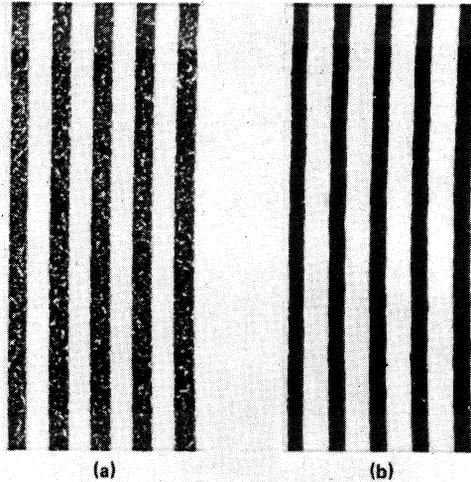


FIGURE 1 Packing densities of MF conductor lines obtained using different resin thicknesses of (a) $4.2 \mu\text{m}$ and (b) $9.2 \mu\text{m}$.

thickness increased the amount of embedded powder and thereby decreased the percentage of open areas (voids) in the fired conductor. The low packing density of the conductor lines in Figure 1(a) produced a sheet resistance which was 65% higher than the sheet resistance of the lines shown in Figure 1(b).

The relationship between the resin thickness and the conductor thickness is shown in Figure 2. The results indicate that, on the average, the conductor lines are $2 \mu\text{m}$ thicker than the resin thickness. Also, the thickness of the MF conductor is independent of its linewidth. For resin thicknesses greater than $15 \mu\text{m}$, the resultant conductor lines exhibited large cracks and poor adhesion.

A comparison between the printed quality of mid-film and thick film Au conductors on alumina and dielectric-coated alumina substrates is shown in Figure 3. It can be seen

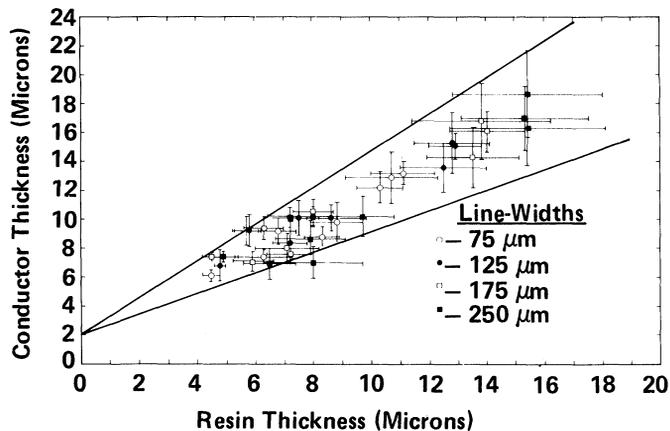


FIGURE 2 The effect of resin thickness on the fired thickness of MF-Au conductors printed on alumina substrates. Similar results were obtained for conductors printed on dielectric-coated alumina substrates. The thickness measurements were carried out using a Zeiss light-section microscope.



FIGURE 3 Comparison between MF and thick film Au printed on alumina and dielectric-coated alumina substrates.

that the edge definition obtained using the MF process is much superior to that of the thick film process. Also, while the thick film line definition decreases with increasing surface roughness, the line definition of MF conductors is virtually independent of the surface roughness of the substrate.

The line-width of the MF conductors is mainly influenced by the UV exposure time of the photosensitive resin and to a lesser extent by the firing temperature.² In the present experiments, an exposure time of 10 s caused a reduction of approximately 10% in the line-width of the MF-Au conductors and an additional 3% reduction occurred following firing at 920°C. This characteristic can be used to increase the density of interconnects in hybrid packages by compensating for the reduction in the line-width during the design and fabrication of the photomasks.

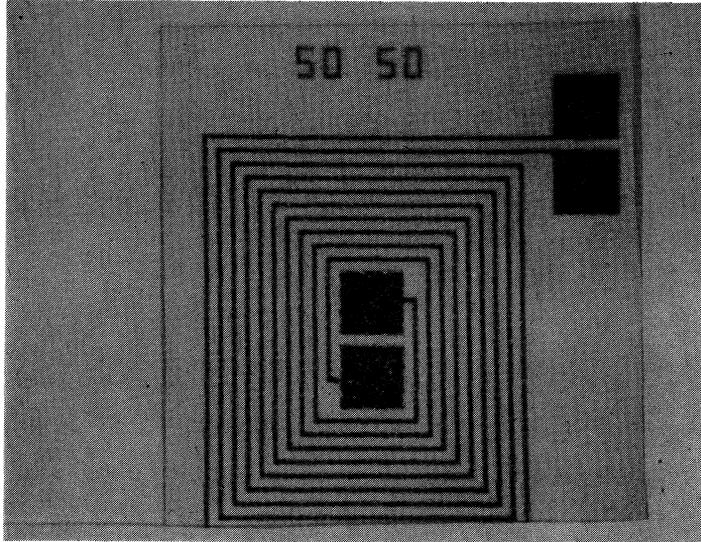


FIGURE 4 A 50 μm MF-Au spiral pattern printed on an alumina substrate.

3.2 Resolution limits

A printability test pattern was used to determine the lines resolution capability of the MF conductors. It contains spiral patterns with line-widths and spaces varying from 20 μm to 250 μm . A typical example of an MF 50 μm spiral pattern printed on an alumina substrate is shown in Figure 4. The as-fired patterns were electrically tested for continuity of the printed lines and for the absence of shorts between the lines. The yield (percentage of spirals without shorts or opens) for the various configurations was determined and the results are summarized in Figure 5 for small geometry spirals. No significant difference was observed in the MF line definition on alumina or dielectric-coated alumina substrates. The yields for 20 μm spacings were very low due to the predominance of shorts in the spirals, but for 50 μm spacings, the yields were much higher, particularly for 50 μm line-width spirals. A 100% yield was obtained for 75 μm line widths and spaces.

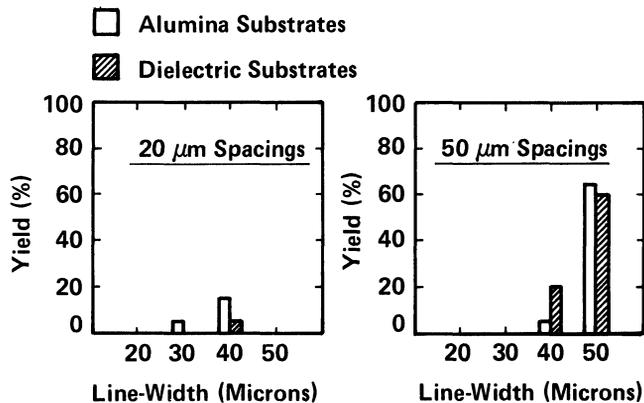


FIGURE 5 The yield of small geometry MF spirals fabricated on alumina and dielectric-coated alumina substrates.

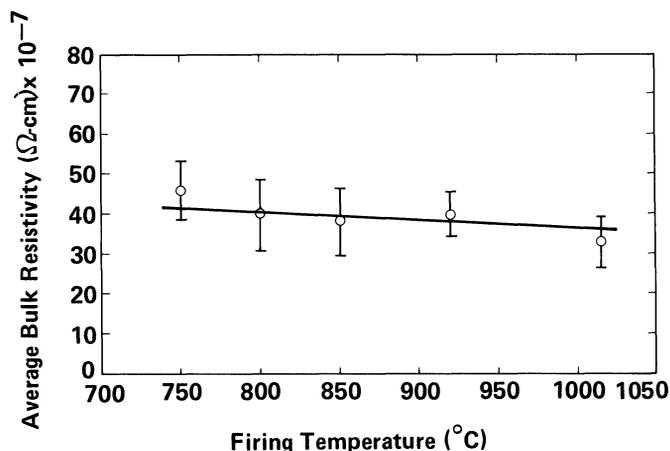


FIGURE 6 The effect of firing temperature on the bulk resistivity of MF-Au printed on alumina substrates.

3.3 Electrical resistivity

Resistivity measurements of fired conductors were carried out using point probes and a precision multimeter. Measurements of 50 μm to 250 μm spiral lines showed that the sheet resistance is independent of the line-width. The effect of varying the peak firing temperature on the bulk resistivity of the MF-Au conductors is shown in Figure 6. The apparent decline in the bulk resistivity of the conductor is due to the gradual increase in the grain size with increasing firing temperature, as shown in Figure 7. Although the conductor fired at 1015°C exhibited the largest grain size, it also developed blisters and a significant number of voids. A peak temperature of 920°C was chosen for convenience since the dielectric material for multilayer applications was fired at this temperature.

Figure 8 shows the change in resistance as a function of the number of refiring cycles; for each cycle the peak temperature of 920°C was maintained for 10 min. The largest change in resistance occurred between the first and second firing, while the resistance remained relatively stable for subsequent refiring cycles. This suggests that increasing the dwell time at the peak temperature to 20 min should stabilize the resistance of the conductor lines.

3.4 Adhesion

The DuPont 90° wire peel test⁴ was used to determine the adhesion of the MF-Au conductors to the substrate. A Dage-Precima MCT 15 pull tester was used in these experiments. The adhesion strength (maximum pull force required to induce failure) of the MF-Au on all substrates was greater than 2.3 Kg, and all failures occurred in the solder wire. These results are similar to those reported by the manufacturers of thick film Au conductors.

3.5 Bondability

Following the test procedure described by Harman and Cannon⁵ the ultrasonic bondability of Au-MF conductors was measured using the pattern shown in Figure 9(a). All the bonding pads in this pattern have dimensions of 125 μm × 125 μm and the bonds were made on pads separated by 200 μm (center-to-center) using 25 μm thick aluminum

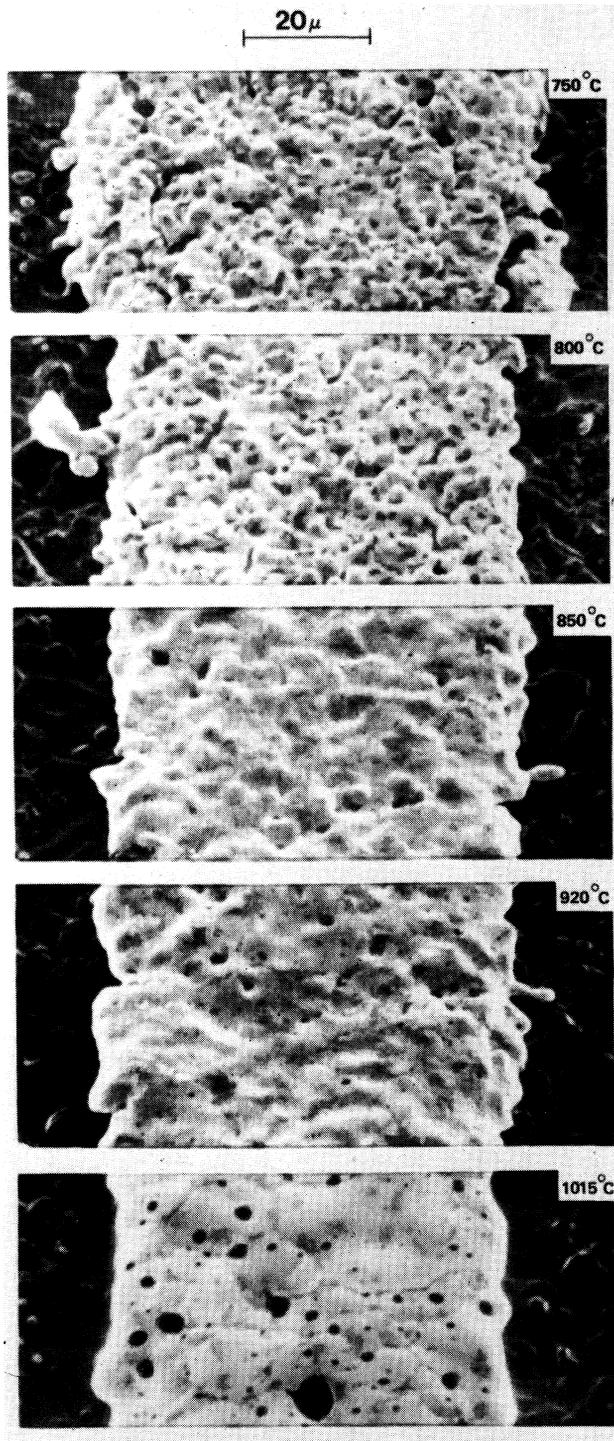


FIGURE 7 SEM micrographs of MF-Au conductors fired at different temperatures.

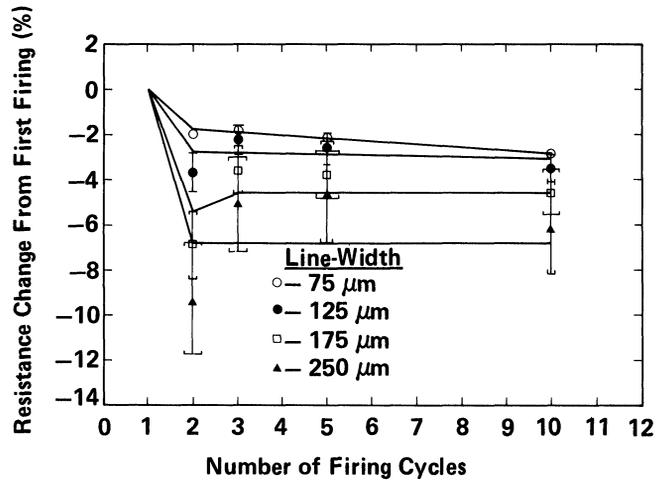
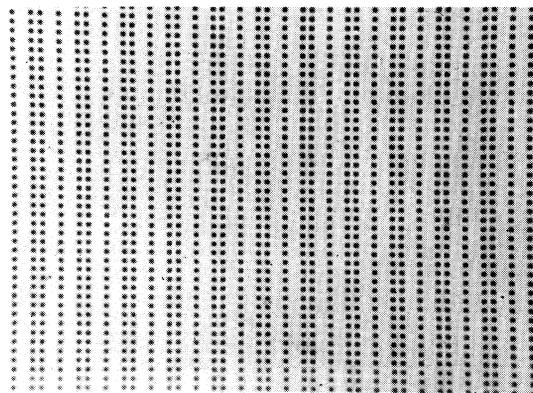
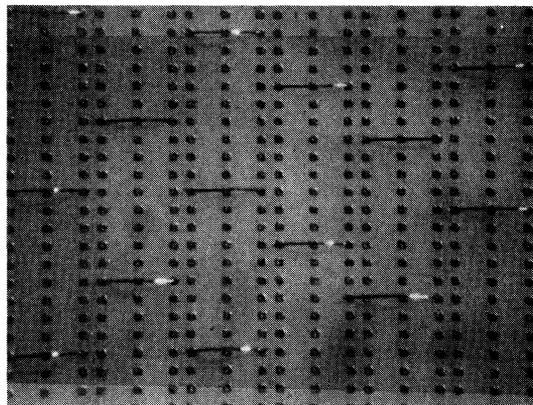


FIGURE 8 The change in resistance of MF-Au lines as a function of the number of firing cycles at 920°C.



(a) Test Pattern



(b) Wire Bonds on Mid-Film Gold

FIGURE 9 The bondability of MF-Au conductors, (a) test pattern and (b) Al wires bonded to MF-Au pads.

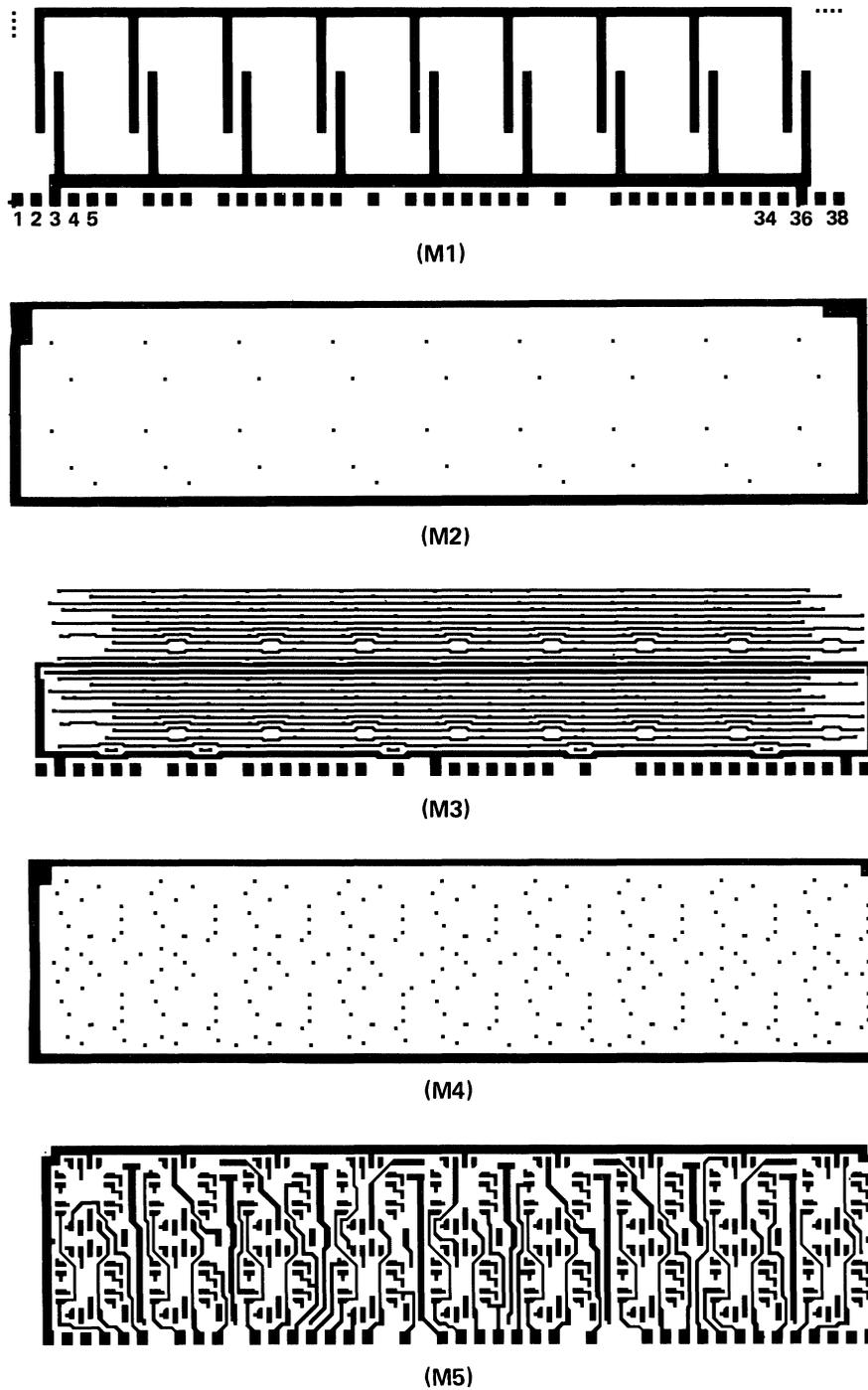


FIGURE 10 Photomasks of various layers used in the fabrication of the multilayer memory package: (M1) 1st. (bottom) metallization layer; (M2) 1st. dielectric layer; (M3) 2nd, (middle) metallization layer; (M4) 2nd. dielectric layer and (M5) 3rd (top) metallization layer.

wires as shown in Figure 9(b). The central unbonded pads were used to locate the position of the pulling hook at the center of the wire loops. Using the Dage-Precima pull tester, an average pull force of 7.4 ± 1.5 g was obtained for the MF-Au conductor compared to 7.7 ± 1.0 g for the thick film Au. Over 90% of the failures occurred in the wire. These results were obtained from samples which were not thermally aged.

4. A PROTOTYPE MULTILAYER MEMORY PACKAGE

To test the performance of MF conductors in a multilayer application, a prototype memory package has been fabricated. This package was originally designed as a thick film interconnection circuit for eighteen 16K memory chips, each packaged in a leadless hermetic chip carrier. It consists of three metallization layers and two insulating layers, as shown in Figure 10. The first conductor layer (M1) contains only two voltage lines for +5V and -5V. The second conductor layer (M3) consists of all the address interconnects, another voltage line for +12V and ground rails. The third conductor layer (M5) has all the component pads and control interconnects together with a power line which brings +12V to the top row of chips. The conductor lines have minimum line-widths and spaces of $375 \mu\text{m}$ (~ 15 mils). The conductor layers are interconnected through $500 \mu\text{m}$ wide vias formed in the dielectric insulating layers, (M2, M4).

The processing sequence for the fabrication of the memory package is summarized in the flow diagram of Figure 11. With the exception of the "back-filling steps", this

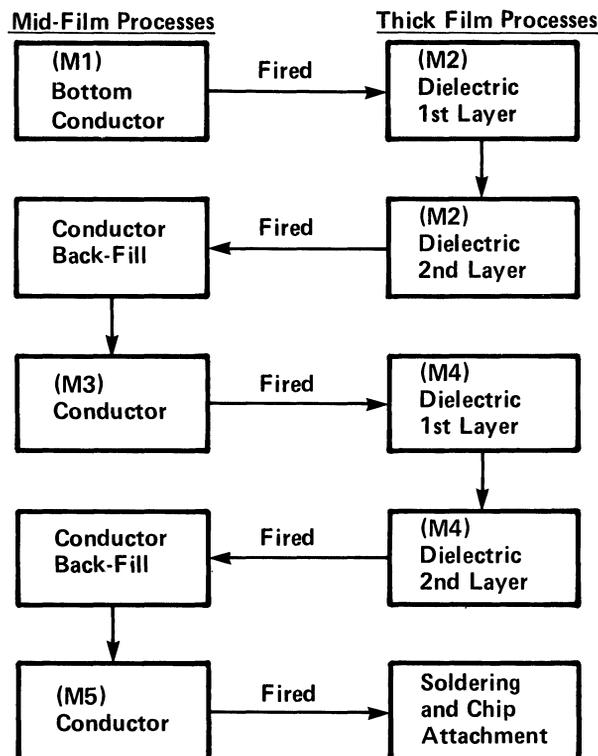


FIGURE 11 Flow diagram illustrating the combined mid-film/thick film processing steps followed during the fabrication of the multilayer memory package.

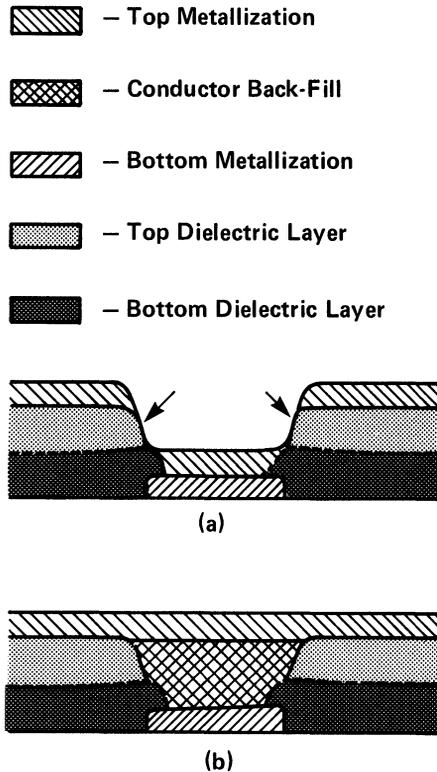


FIGURE 12 Schematic drawing of a $100\ \mu\text{m}$ deep via connecting top and bottom metallization layers (a) without back-filling where shearing of top conductor occurred at the sites indicated by the arrows and (b) with back-filling of the via which eliminates shearing and produces smooth step coverage.

sequence is similar to that for the fabrication of thick film multilayer circuits. These back-filling steps involve the deposition of MF-Au conductor into the vias using the photomask of the previously printed dielectric layer. These steps were necessary particularly for the deep vias connecting the top (M5) and bottom (M1) conductor layers which represented a vertical drop of $100\ \mu\text{m}$ (~ 4 mils). If no back-filling was performed, the conductor would shear at the edge of the via resulting in poor step coverage and a break in the connection between the metallization layers, as depicted in Figure 12(a). By back-filling the vias, proper step coverage developed, as shown schematically in Figure 12(b).

The average resistance of the MF address lines on layer M3 was $1.6 \pm 0.6\ \Omega$ and the average resistance from pad 1 to 38 (cf, Figure 10) was $261 \pm 56\ \text{m}\Omega$. These results were in good agreement with the design specifications of the memory package. A complete prototype package is shown in Figure 13.

It should be pointed out that poor interconnection between top (M5) and bottom (M1) metallization layers was the main cause of failure in packages fabricated with thick film conductor interconnects. However, the use of the MF process and the ability to back-fill the vias with MF conductor powder as described above ensured proper interconnection and improved the yield significantly.

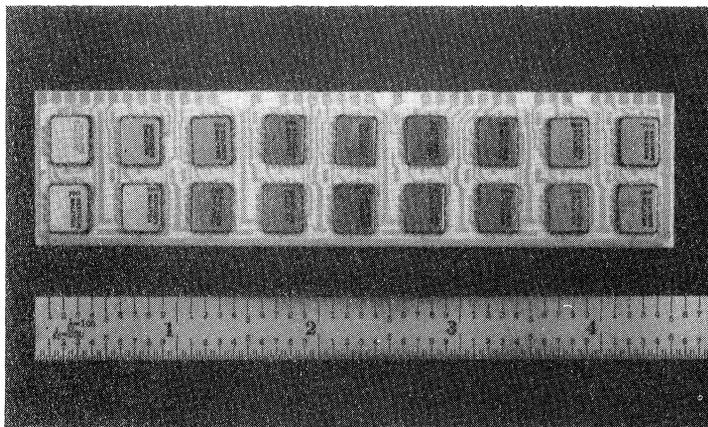


FIGURE 13 Fully assembled prototype multilayer memory package.

5. CONCLUSIONS

This investigation was carried out to evaluate the mid-film process for the fabrication of multilayer microcircuit packages. For this application, the conductor must be compatible with the thick film dielectric materials used in the multilayer application. In our laboratory study, we have used gold powder extracted from a thick film conductor paste. However, for industrial applications, the thick film conductor powder would be obtained from the manufacturer before the addition of the organic vehicle. In our case, it has been shown that the MF conductor would have characteristics identical to a thick film conductor printed on the same substrate material.

An optimized mid-film process is capable of producing fine metallic interconnects of 50 μm widths and spaces without the use of expensive lithographic thin film or high resolution thick film techniques. This is particularly attractive for the fabrication of low cost, high density interconnect packages. Using the MF technique, deep vias can be filled with conductor powders which upon firing eliminate shorts and improve the fabrication yield of multilayer packages. This technique has been successfully applied to the prototype fabrication of a multilayer memory package.

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