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MODELLING THERMAL RESISTANCE OF POWER MODULES HAVING SOLDER VOIDS WITH FINITE ELEMENTS

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A general thermal model to calculate the thermal resistance of a power module having rectangular die and layers has been constructed. The model incorporates a finite element computer program to solve for three-dimensional heat conduction. Effects of voids in the solder regions are included. A sample case is analyzed, and a comparison is made to a recent study.

1. INTRODUCTION

Thermal resistance is a primary factor in the design of electronic modules for use in motor control and power conversion. In order to ensure reliability of these power modules, temperatures at the heat-generating die must remain below a certain limit. This limit is given in terms of a thermal resistance (impedance) and prescribed by the heat duty and thermal properties of the die and their supporting layers. If the development of modules depends solely on constructing prototypes and testing, the procedure will be costly. Thus, theoretical heat transfer models are used to determine the temperature distribution or thermal resistance in a module.

The heat transfer mechanism in a power module is complex: the heat flow is three-dimensional, and the many layers can have contrasting thermal properties. Because of this, analytical solutions are available only for very idealized geometries.[1,2] For more complex and detailed cases, numerical approaches are generally taken. For instance, Wenthen[3] investigated heat conduction in a diode using finite differences. The finite element technique has been applied to high temperature electrical contracts[4]. Kadambi and Abuaf[5,6] relied on a commercially available finite element code to calculate temperature distributions in complex chip/sink structures. Both two and three-dimensional analyses were documented in which they determined the effects of solder layer thickness and the heat sink convective coefficient upon the thermal resistance. The constantly increasing computer capabilities make numerical computations attractive, and many more will follow.

The objective here is to report on the modelling of power modules utilizing an available general purpose finite element program. The model is flexible and will accept different geometrical configurations, material properties, and heat loads; the temperature distribution throughout the device is calculated. It is demonstrated how the commercial finite element program is utilized within the thermal model. This model is suitable for initial design work and also provides the capability of comparing, on the same basis, several competing designs. Calculations are based upon solution of the steady-state conduction equation in three dimensions. A description of the problem solution procedure is included along with a sample parametric study of a typical module.

2. FORMULATION OF THERMAL MODEL

The structure of a power module involves a number of die mounted upon a stack of supporting layers. Solder is usually included beneath the die as well as between all following

layers for thermal contact and mechanical bonding. During operation, thermal energy is generated within the die and is transferred by conduction through the supporting layers. Thermal resistance is governed by geometrical and thermal properties of the materials forming the power module. The heat flow is three-dimensional with both in-plane and transverse dissipation. These considerations are taken into account in the formulation of the model. Overall boundary conditions include a uniform heat flux at the top surface of the die as well as a uniform temperature at the bottom of the last layer or base. All four sides of each die and layer, as well as the top exposed surface of every layer, are considered to be adiabatic.

Mathematically, steady-state heat transfer within each die or layer is described by

$$\frac{\partial^2 t}{\partial x^2} + \frac{\partial^2 t}{\partial y^2} + \frac{\partial^2 t}{\partial z^2} = 0 \tag{1}$$

where t is the temperature and x, y, and z represent rectangular coordinates. Equation (1) holds as long as the thermal conductivity is constant, independent of direction or temperature. Figure 1 displays a top-view outline of a sample device having four die and three layers. A uniform heat flux is specified at the top of the die (z = H, where H = module thickness) or

$$-k\left[\frac{\partial t}{\partial z}\right]_{z=H} = Q \tag{2}$$

where k is the die thermal conductivity. The temperature at the base, t(z = 0), may be set to any convenient value such as zero,

$$t(z = 0) = 0 \tag{3}$$

It follows that the thermal resistance at any point within the module is the ratio of temperature drop to heat flow or power dissipation:

$$r = t/Q \tag{4}$$

It is evident that, by this definition, the maximum value for r occurs at the top of the die. However, typically an average resistance is called for in the design. Accordingly, the quantity R is defined as the average of all individual resistances calculated at the die top, or

$$R = \frac{1}{nQ}\sum_{i=1}^{n} t(z = H) \tag{5}$$

Effects of solder present between the layers must be included. One important characteristic of solder junctions is the presence of voids. These constitute a large resistance to heat transfer since the thermal conductivity of the void space, occupied by a gas, is much less than that of the solder. To account for voids, a simplified treatment is incorporated into the thermal model.

Heat transfer in a solder region is assumed to be one-dimensional (through the thickness) with the layer contact area proportional to the void fraction. Voids are considered to be evenly distributed throughout the solder junction. For example, if a void fraction of 0.20 (20%) is assumed, then the calculations are based upon an effective surface contact area of 80% along with the thermal conductivity of the solder. This approach differs from the void model proposed by Abuaf and Kadambi[7] which treats voids as cracks originating from the edges; as the void fraction increases, the cracks extend further towards the module's center.

3. SOLUTION OF MODEL

A numerical approach is employed to solve the system of equations to find the temperature profile within the device. A general application, finite element computer program is used. The program, ANSYS, was developed and is supported by Swanson Analysis Systems, Inc., Houston, PA. It is well established and has been shown to be reliable and accurate in solving similar heat transfer problems[8,9]. This program is incorporated within the computerized thermal model in such a way that the user does not have to be familiar with ANSYS or finite element methods. Instead, a pre-processor fortran program is included to convert the data file describing the module into ANSYS finite element code.

The pre-processor program serves primarily to subdivide any power module into nodes

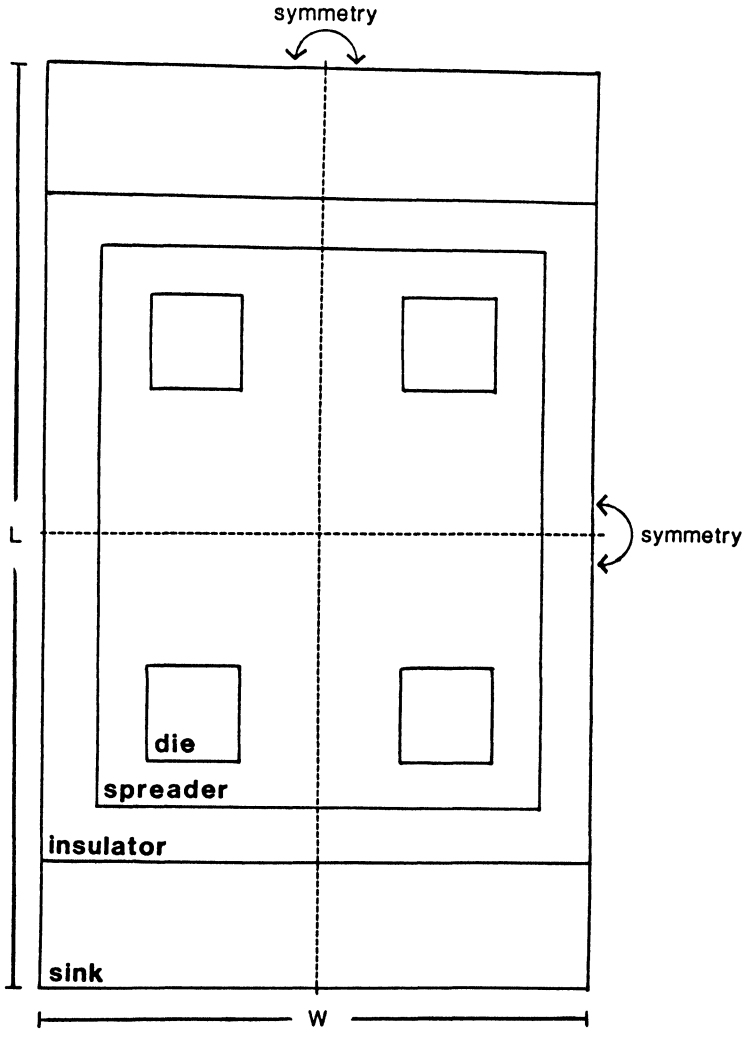

FIGURE 1. Top-view outline of idealized power module.

and individual finite elements. Two different ones are present: brick and conducting bar. The brick finite element represents three-dimensional conduction within the die and layers as described by Equation (1). If possible, it is important to take advantage of any geometrical symmetry present. For instance, the design of Figure 1 has symmetry about both the x and y axes so that only one-quarter of it needs to be analyzed; this greatly reduces computational time and storage space. Such a section is displayed in Figure 2.a while Fig. 2.b shows the same structure subdivided into brick elements. The solder regions are too thin to be seen in these views. Also, the die does have a finite thickness which is not apparent from the figure. The coordinate system indicated has its origin at the corner common to all layers with z = 0 defined at the bottom of the last layer. The heat flow is applied at the top surface of the die. Of course the device configuration in Figure 2 is arbitrary, and the model is capable of analyzing other variations, some of which are shown in Figure 3. Note that these represent one-quarter or one-half sections.

In the case of the solder regions, the one-dimensional conducting bar element is utilized. This is equivalent to setting $\partial^2 t/\partial x^2 = \partial^2 t/\partial y^2 = 0$ in Eq. (1) and adjusting the differential area, dxdy, to account for the void fraction. To illustrate the effect, consider the top-view of

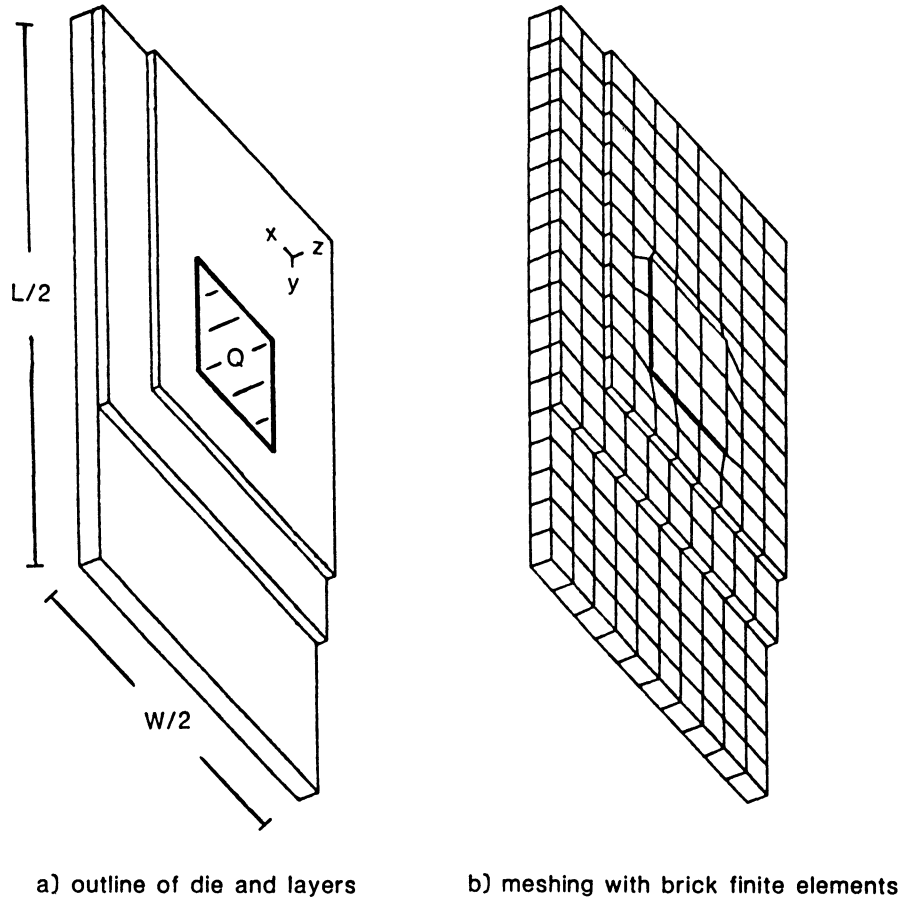

FIGURE 2. Top-view profile of modelled section.

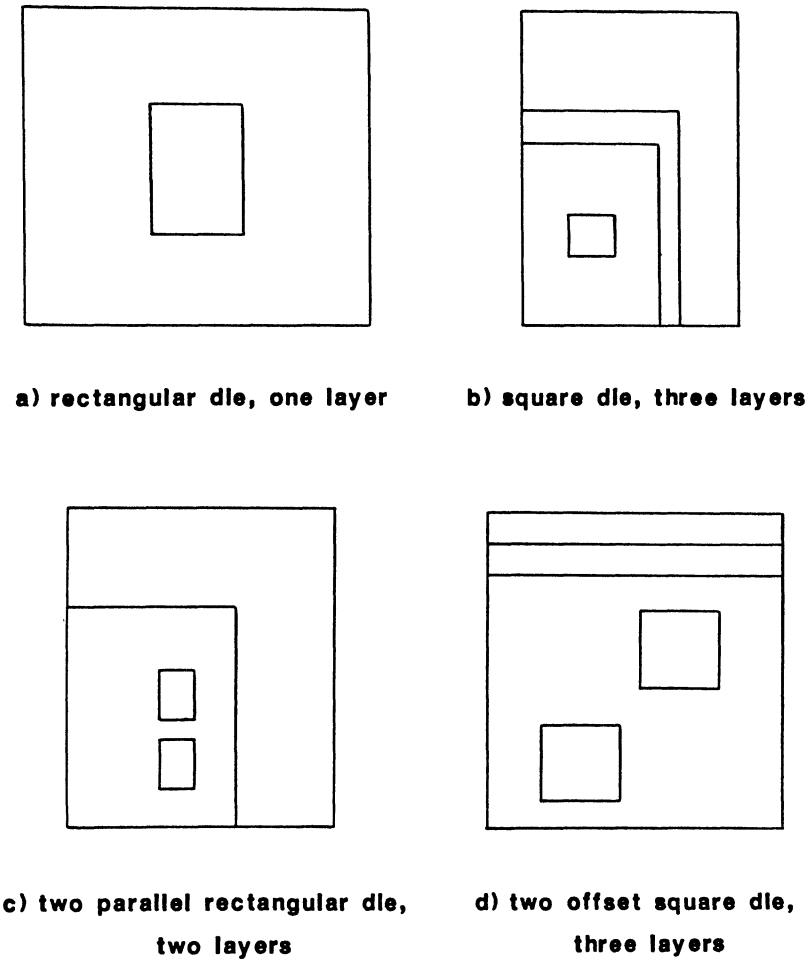

FIGURE 3. Top-view outline of some module die and layer variations.

the solder region seen in Figure 4. The heat flow is normal to the contact area which lies in the xy plane. In Figure 4.a, the case of zero voids is assumed so that all the differential area of each element is available for heat transfer. On the other hand, if the void fraction is set to 0.36, Figure 4.b indicates the proportional reduction in differential area.

As stated, the pre-processor program rewrites the data file into another one having the equivalent ANSYS format. The steps carried out automatically may be summarized as:—

- — read model geometry, solder void fraction, heat flow, and base temperature
- — mesh each die and layer with three-dimensional conduction brick elements
- — mesh solder regions using one-dimensional heat conduction bar elements adjusted in area by the void fraction
- — using the solder elements, link each die to the first layer and also link all following layers
- — apply uniform boundary conditions at individual elements at each die top and also at the bottom of the base layer
- — activate finite element code

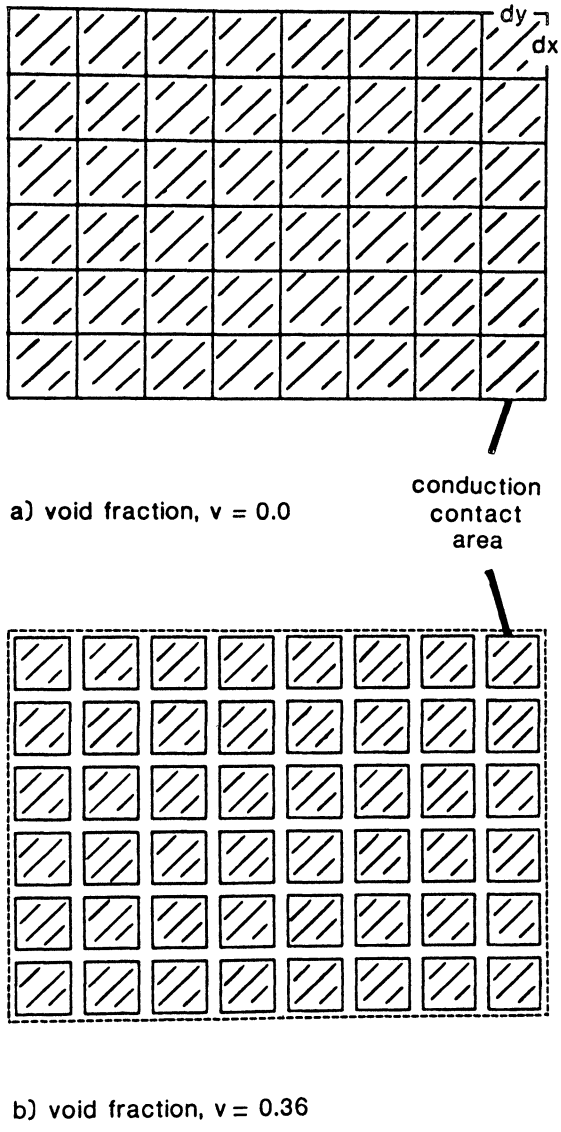

FIGURE 4. Representation of solder voids.

Numerical accuracy of the solution is dependent on mesh resolution. A finer mesh (more individual elements) will yield better results. However, a compromise exists between accuracy and computational time; in a three-dimensional simulation, the number of finite elements can quickly exceed the storage capacity of a large computer. In addition, it is impossible to predict all the different configurations that can exist through variation of the number and dimensions of layers and die. Thus, the mesh resolution is allowed to vary. The controlling parameter is a resolution factor which specifies the number of elements; it ranges from 1–7 in increments of one. A coarse mesh may be used in comparative cases when fast processing of models is desired. Finer resolution (increasing the resolution factor) can

determine solution sensitivity and provides more detailed and accurate results at the expense of computational time and storage. The resolution is dependent on the geometry, so that an identical mesh factor does not produce the same degree of accuracy if the geometry varies. On the other hand, if only the heat flow, base temperature, or thermal properties differ, the meshing of the module remains the same.

The resolution is linked to the dimensions of the individual brick finite elements. For best results, the width: length: thickness ratio of each individual element should be 1:1:1. In an actual device, the overall length or width is typically two orders of magnitude greater than the thickness. Hence, to maintain a 1:1:1 ratio would require a prohibitively large number of elements. The ratios available with the model range from 1:1:1 to 40:40:1 depending on the mesh factor. The recommended procedure is to begin with a relatively coarse mesh and calculate a solution. Then the mesh resolution may be stepped upwards by increments of one until the solution converges. The degree of convergence could be determined by comparing the overall thermal resistance of two successive runs. A deviation between the two values of less than a few percent may be an acceptable convergence criterion.

Since fractional elements are not allowed, certain limitations are inherent to this model. In general, difficulties arise when die are located too closely to each other or to the edge of a layer. Such problems are readily detected in examining the output geometry plot, generated by ANSYS, which would be distorted. When this is the case, modifications in die geometry or positions must be made. For instance, if two die are spaced too closely together, both of them are lumped into one heat source. If a die lies too near a layer edge, its boundary is extended to coincide with the layer edge. Such small changes will not significantly alter thermal conditions while allowing for proper dividing of the module into finite elements.

The solution to each case is contained in two output files. One contains (among other finite element details) a table of nodal temperatures referenced by the x, y, and z coordinates of the node. Another file, displayed by a graphics terminal, has three plots. The first two are a side profile and a top-view outline of the power module section modelled. These serve as visual checks of the geometrical input concerning die spacing and layer positions. The last plot is a top-view outline with the addition of labeled isotherms. Individual thermal resistances may be determined from the nodal temperature table while any hot spots can be quickly located from the temperature contour plot.

4. PARAMETRIC ANALYSIS OF SAMPLE POWER MODULE

The module illustrated in Figures 1 and 2 serves as the candidate for parametric studies by the computerized thermal model. Table I, which amounts to the input file, characterizes the one-quarter section to be analyzed. It consists of one die supported by three layers: a copper spreader, an insulator (either alumina or beryllia), and a copper base (sink).

TABLE I
Properties and dimensions of one-quarter module section, heat dissipation = 100 W (center of die located at x,y = 20.0,30.0 mm)

Module Layer	Material	Thermal Conductivity W/(m°C)	Void Fraction	Layer Dimensions (mm) width	length	thickness
die	silicon	126	–	15	15	0.250
solder	alloy	36	0.0–0.9	15	15	0.025, 0.050, 0.100
spreader	copper	398	–	35	45	1.000
solder	alloy	36	0.0–0.9	35	45	0.025, 0.050, 0.100
insulator	alumina (beryllia)	29 (197)	–	45	55	1.250
solder	alloy	36	0.0–0.9	45	55	0.025, 0.050, 0.100
sink	copper	398	–	45	75	2.500

Solder joins the die and each of the layers, and its thickness and void fraction are allowed to vary. An identical void fraction and thickness are assigned to each solder layer for convenience although this is not required. Effects studied include the influence of solder layer thickness and void fraction for both alumina and beryllia insulators.

Figure 5 summarizes the alumina results. The overall resistance is divided by the value for R at zero voids and plotted against void fraction. At all void fractions, R/R (v = 0) increases along with the solder thickness, h (solder), as expected. For example, when the void fraction, v, is 0.5, the relative resistance increases are 0.095 and 0.267 (9.5 and 26.7%) at h (solder) of 0.025 mm and 0.100 mm, respectively. Also, the ratio of increases is maintained at all void fractions; the 0.100 mm thickness case exhibits an average resistance increase approximately three times that of the 0.025 mm one. It should be noted that this does not mean that the average resistance is three times higher, but only the percent increase of R, based upon the no void case, is a factor of three. The actual value of R (v = 0) was computed to be 0.122, 0.134, and 0.156 °C/W for solder thicknesses of 0.025, 0.050, and 0.100 mm, respectively. Overall, this figure demonstrates that resistance increases are minor, less than 10%, as long as v < 0.25. However, at larger void fractions, the effects are significant; the resistance can double at 75% voidage (see h (solder) = 0.100 mm).

Similar trends are documented in Figure 6 in which beryllia replaces alumina as the insulator. Effects become large at v > 0.25. At h (solder) = 0.100 mm, a 50% resistance increase is observed at v = 0.50, and it is apparent that resistance is more sensitive in this case than for the alumina insulator. This is due to a reduction in the overall resistance with the beryllia since its thermal conductivity is much greater. At the same time, the impedance of each solder layer constitutes a larger portion of R. For beryllia, the overall resistance at no voids was 0.063, 0.078, and 0.106 °C/W at h (solder) = 0.025, 0.050, and 0.100 mm, respectively.

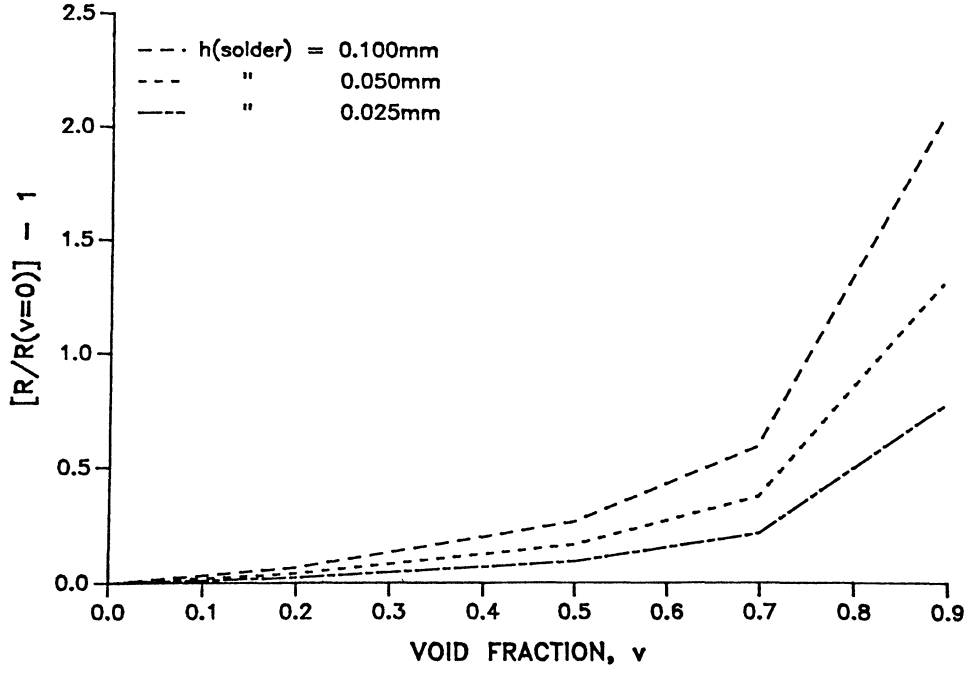

FIGURE 5. Effects of solder void fraction and thickness upon average resistance for alumina insulator.

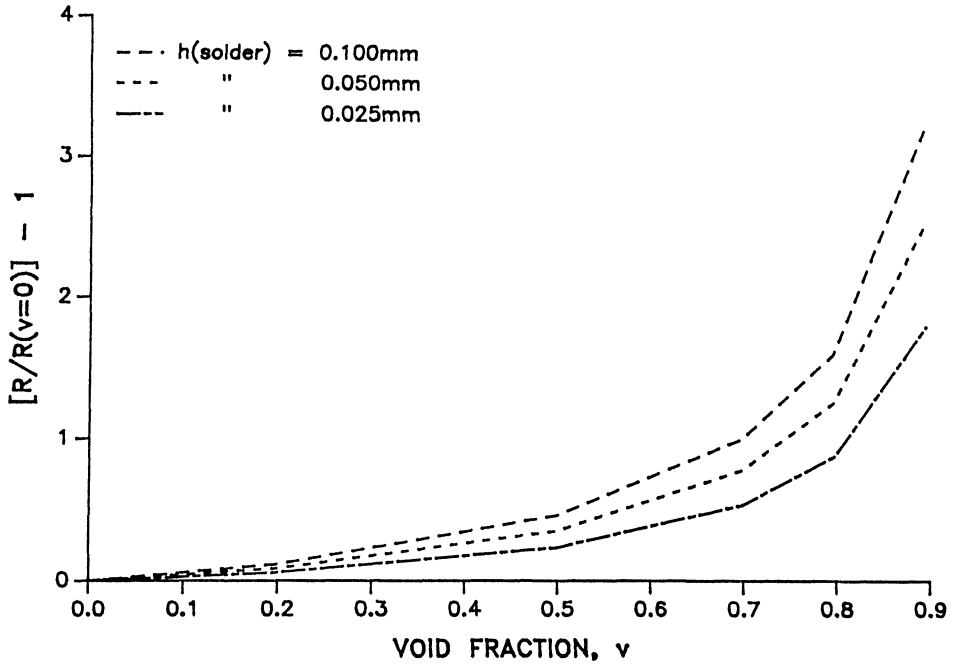

FIGURE 6. Effects of solder void fraction and thickness upon average resistance for beryllia insulator.

These trends are comparable to the numerical and experimental studies conducted by Abuaf and Kadambi[7] who concluded that void effects become significant at $v > 0.33$. At a void fraction of 0.60, a 50% resistance rise was measured. This compares favorably to the present data which indicate $v = 0.50$ for the corresponding resistance rise at 0.100 mm solder thickness. Although both studies utilized a beryllia insulator, the modules are significantly different in layer thicknesses and dimensions. Furthermore, the present results consider uniformly distributed voids in all layers whereas a single layer crack was simulated in the other study. In light of this, it is interesting that the data are comparable. This evidence suggests that power modules having the same basic structure may be affected to the same degree by any type of void as long as the correct void fraction is noted.

A benefit of the current computerized thermal model is the availability of temperatures throughout the entire module. From this information, local thermal resistance may be calculated. In Figure 7, this quantity is reduced by R and plotted versus the reduced width. This type of representation, showing temperature excursions relative to overall, is useful because in practice only the average overall impedance is known. It is desirable to identify locations where the temperatures are significantly higher. Resistance contours are indicated in the case of the alumina insulator, 0.050 mm solder thickness and $v = 0.0$. The y-coordinate is fixed at 30 mm which corresponds to the centerline of the power die. This yields the maximum resistance profile since any position off the centerline, at the same z-coordinate, exhibits a lower temperature or resistance. It is noted that local temperatures may be almost 50% greater than average at the die. Such temperature variations across layers have been computed by others[7], and point out the problem of basing design upon an average resistance while actual local temperatures may be much higher[10]. Similarly, Figure 8 shows the resistance profile throughout the module length, at $x = 20$ mm (corresponding to the die centerline). It is evident how much of the total resistance can be attributed to the alumina. Plots for the beryllia case (Figures 9 and 10) yield similar trends although the

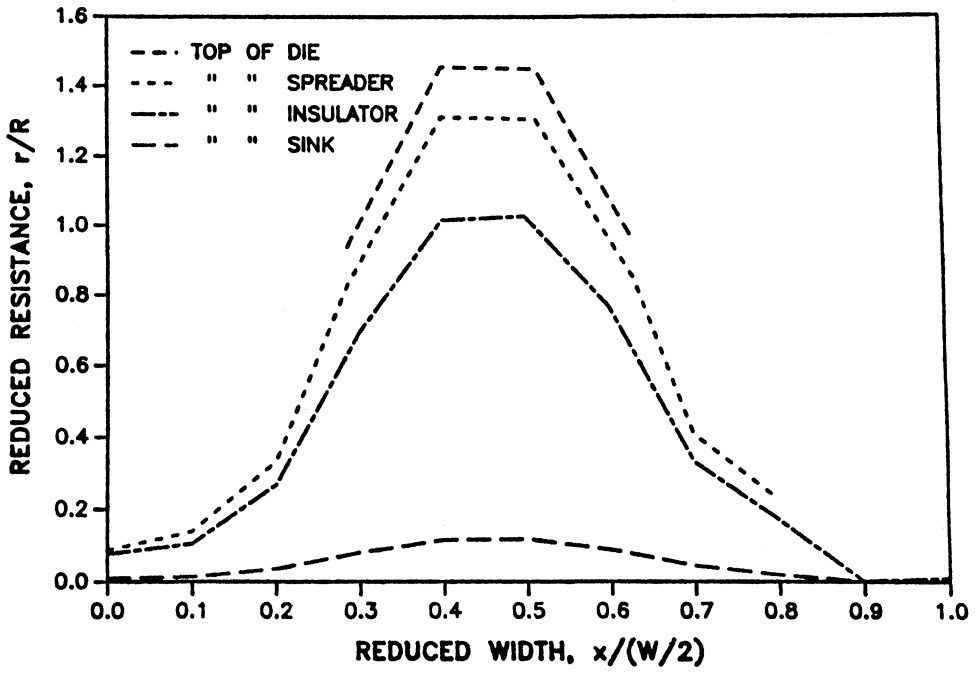

FIGURE 7. Variation of local resistance along width for alumina insulator case (no voids).

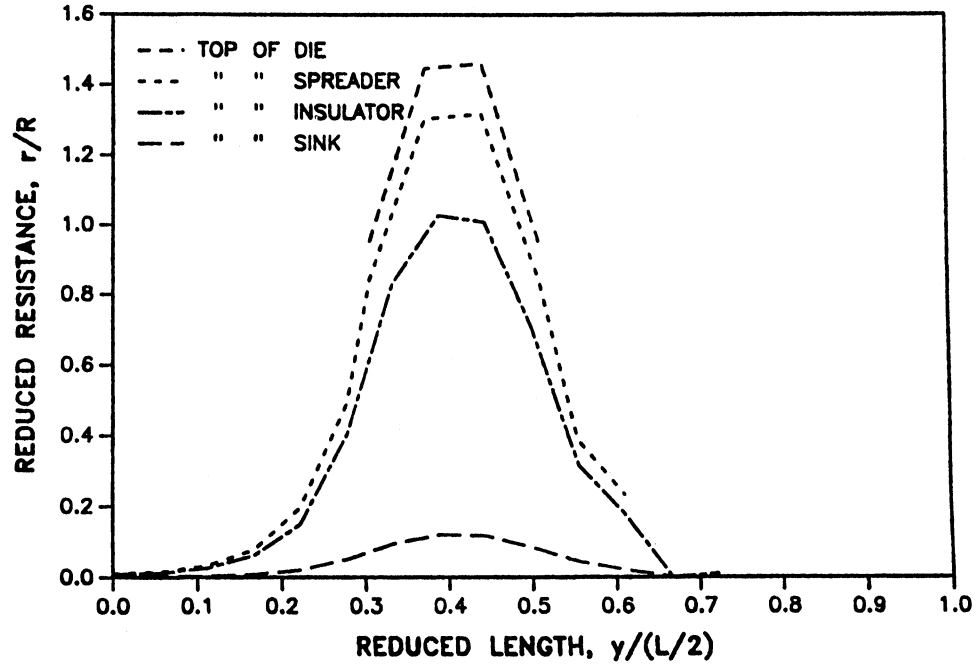

FIGURE 8. Variation of local resistance along length for alumina insulator case (no voids).

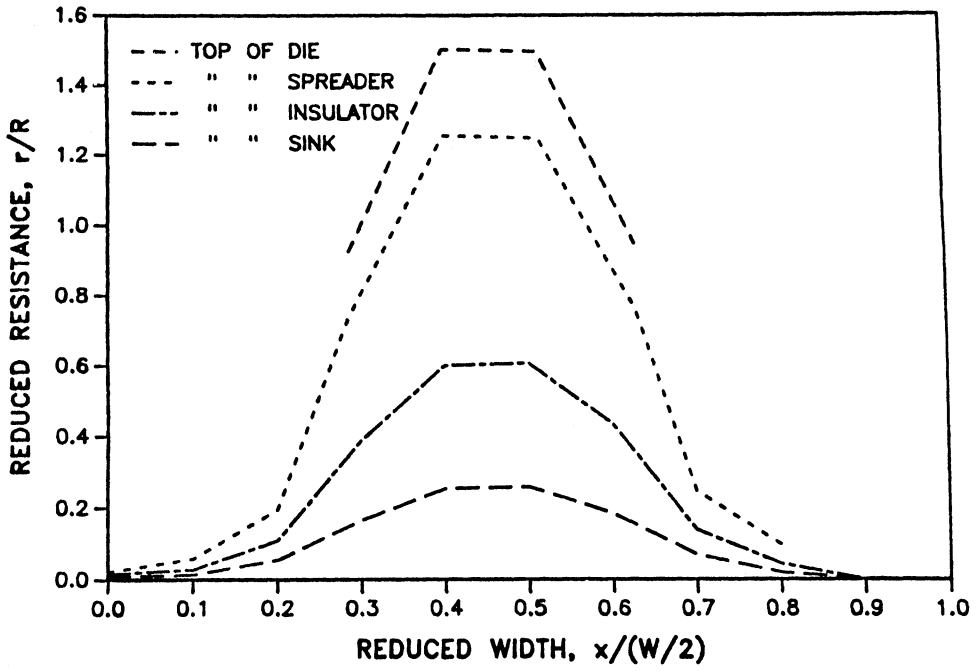

FIGURE 9. Variation of local resistance along width for beryllia insulator case (no voids).

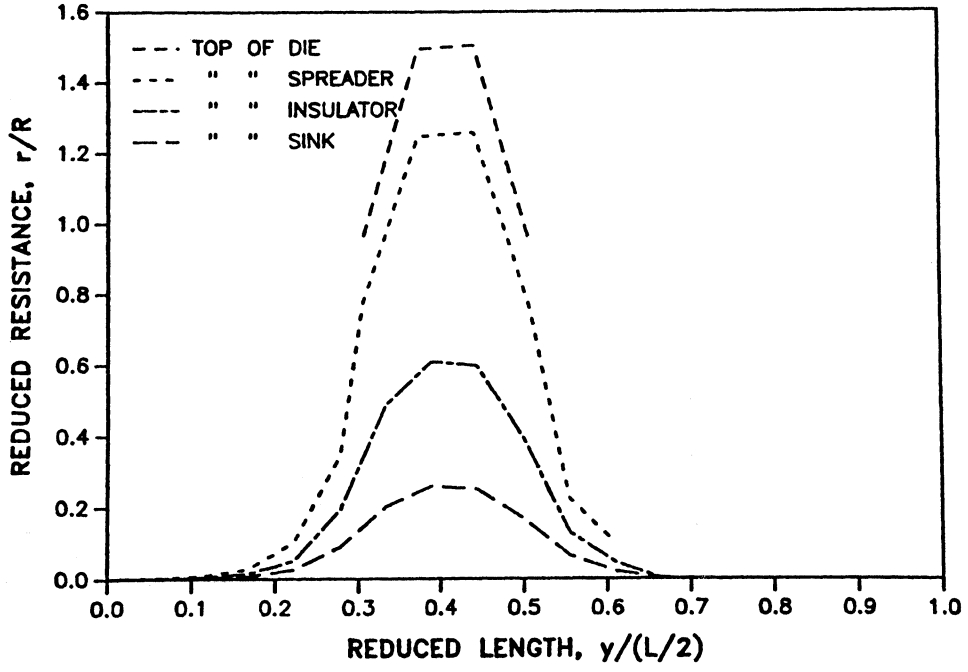

FIGURE 10. Variation of local resistance along length for beryllia insulator case (no voids).

relative contribution of the insulator is much less. Again, 50% excursions in local resistances are noted at the center of the top die surface.

5. CONCLUDING REMARKS

A computerized thermal model to aid in power module design has been described. Results have been generated for a sample case with different insulators and indicate the importance of solder voids. These effects are significant primarily when the voidage is greater than 25%. Comparison with another study has indicated that void fraction effects are similar in magnitude among different power module designs. Local resistance excursions as high as 50% of the overall were calculated at the die. This indicates that if average impedance is used as a design parameter, a large safety factor must be included to accomodate the temperature excursions.

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NOMENCLATURE

dx = differential width, mm
dy = differential length, mm
h = individual layer or solder thickness, mm
H = module thickness, mm
i = counting integer
k = thermal conductivity, W/m−°C
L = module length, mm
n = total number of local temperatures
Q = heat flow, W
r = local thermal resistance, °C/W
R = average, overall thermal resistance, °C/W
t = temperature, °C
v = void fraction
W = module width, mm
x, y, z = rectangular coordinates, mm

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