Active and Passive Elec. Comp., 1987, Vol. 12, pp. 201-211
Photocopying permitted by license only

A COMPARISON BETWEEN GaAs MESFET AND Si NMOS ESD BEHAVIOUR

A.J. FRANKLIN, E.A. AMERASEKERA and D.S. CAMPBELL

Component Technology Group, Department of Electronic and Electrical Engineering, University of Technology, Loughborough, Leicestershire, UK

Work is in hand at Loughborough University to investigate and compare the ESD sensitivity of GaAs D-MESFETs and unprotected enhancement mode NMOS structures.

The work to date has shown that GaAs MESFET structures can be severely degraded with ESD pulses above 600V as compared with 200V for Si NMOS. It has also been shown that both GaAs and NMOS structures are polarity sensitive.

The behaviour of the Schottky barrier is used to explain the polarity behaviour in GaAs MESFETs. The breakdown of the oxide in the NMOS devices can be explained by impact ionisation.

1. INTRODUCTION

It has been recognised for some time that one of the major failure mechanisms in semiconductors is electrical overstress (EOS) which includes device failure due to Electrostatic discharge pulses (ESD).

Equipment manufacturers, users and semiconductor manufacturers now estimate that 60% of semiconductor failures[1] can be attributed to EOS, a large percentage of this being due to ESD.

In order to idenfity the failure mechanisms associated with the application of ESD to unprotected GaAs MESFET and Si NMOS FETs, an investigation has been carried out and the results to date are summarised in this paper.

2. BASIC STRUCTURES

The two basic structures that have been investigated are n-channel, depletion mode metal-semiconductor GaAs FETs and n-channel, enhancement mode metal-oxide-semiconductor Si FETs. Figures 1a and b, show the structures and it can be seen that they are radically different.

The D-MESFET has a n-doped channel and the source and drain contacts are made using an ohmic metal. The gate contact is formed with a metal laid directly onto the surface of the GaAs forming a Schottky depletion region beneath the area of the gate contact.

The NMOS device has a lightly p-doped channel and has n^+ wells diffused to form the source and drain contacts. An oxide of 400Å is grown on the wafer, and the gate is formed with n^+ polysilicon laid on the oxide.

Electrical modulation of the drain current is fundamentally different in each case. Depletion mode MESFET operation uses the action of the Schottky depletion region, under negative voltage bias, to deplete the channel of carriers and hence decrease the current flow.

The enhancement NMOS device is modulated by a positive voltage on the gate which induces an inversion layer in the channel beneath the gate oxide thus allowing current to flow.

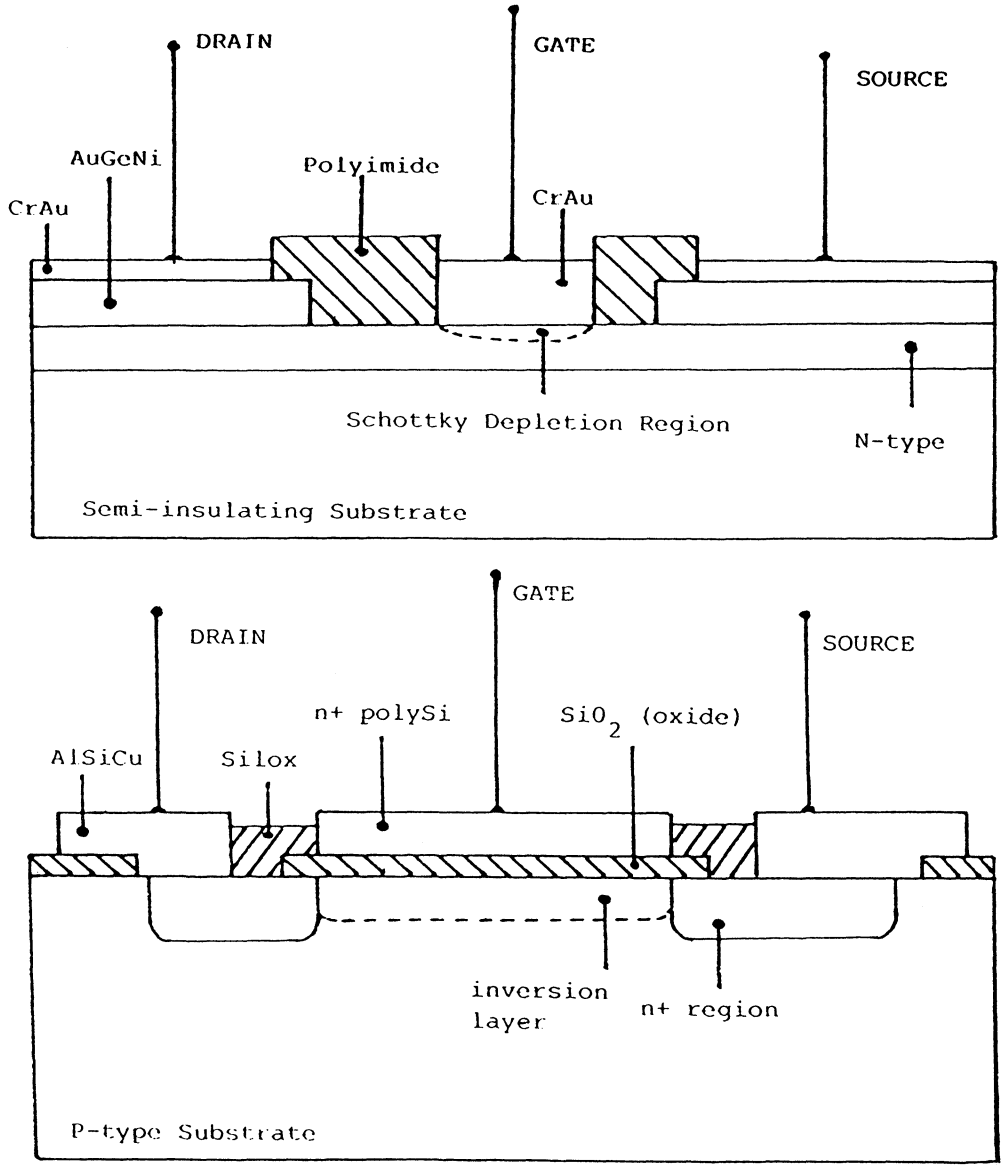

FIGURE 1 Basic diagrams of structures. (a) D-MESFET cross-sectional structure. (b) E-NMOSFET cross-sectional structure

3 EXPERIMENTAL WORK

3.1 Introduction

The present study has been concerned with ESD pulses applied to the gate of the device under investigation, resulting in a breakdown which may have different causes in the

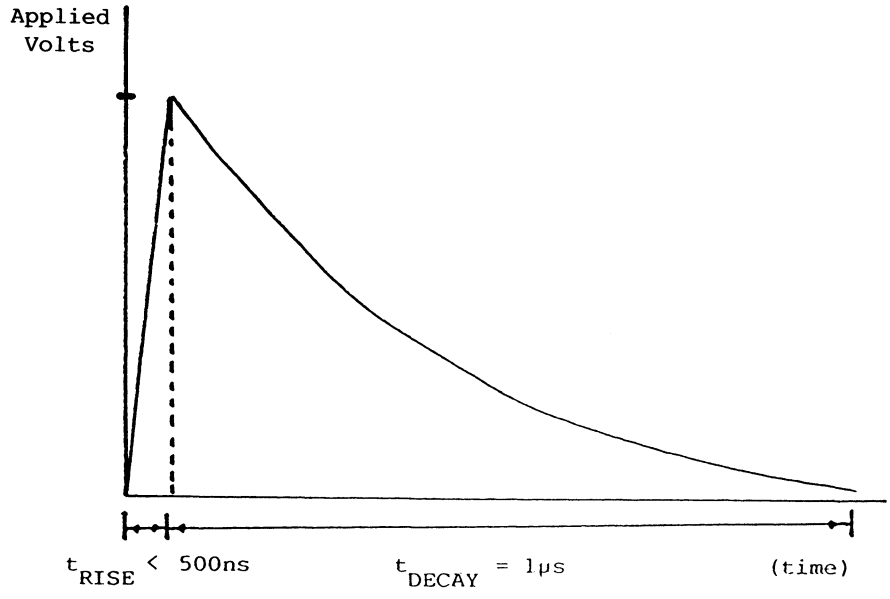

FIGURE 2 Typical ESD "Human Body Pulse"

two devices. The ESD pulses are derived using the MIL-STD-883C, "Human body model".[2] The human body model comprises of a circuit in which a high voltage supply charges a 100pF capacitor through a 1MΩ resistor. The discharge is through a 1.5KΩ (body) resistance in series with the device under test. The charge/discharge circuits are selected by means of a mercury wetted 2 pole relay.

The pulse generated using the human body model is of the shape shown in Figure 2 as observed on an oscilloscope and using a low capacitance probe. The rise time of the pulse, t_{RISE}, is less than 500ns, and the decay is approximately 1 μs. In practice this latter value will vary depending on the load offered by the device to the discharge circuit.

3.2 Related device geometries

The GaAs MESFET surface geometry is shown in Figure 3. It comprises two AuGeNi ohmic contacts and a CrAu gate of dimensions 2 × 150 μm. The gate/source/drain dimensions are 1 μm and 2 μm respectively. They are fabricated on a 2″ Si-ion implanted GaAs LEC wafer which contains 1500 D-FET structures. In the majority of cases the whole active area is overlayed with polyimide.

The NMOS structures are fabricated on a 3″ p-type Si wafer. The structures are arranged in rows each with a common source and gate, and they are directly accessible using a probe kit. The devices have various gate lengths and widths (maximum 100 μm, minimum 1.4 μm). There are also separate MOS capacitors present. The MOS FETs have polysilicon gates and alloyed AlSiCu drain and source contacts.

3.3 Procedure

The main part of the experimental programme consisted of pulsing the gate(s) with varying polarity voltages. The source and drain electrodes were either earthed (GaAs) or left floating (NMOS), with the substrate grounded.

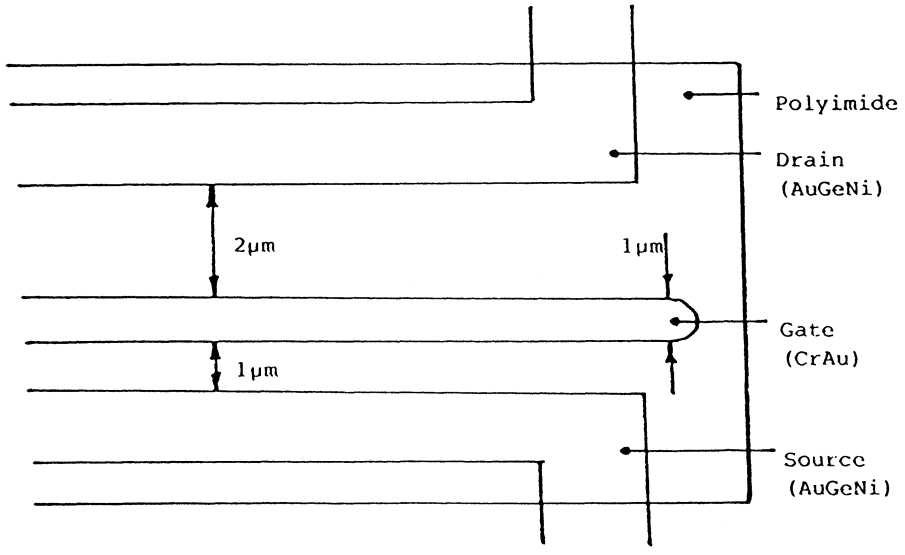

FIGURE 3 GaAs MESFET Surface Geometry

The gate was pulsed with voltages between ±50V up to ±1 kV, and in both cases this gave a range of resultant breakdown characteristics.

After the application of each pulse the devices were analysed electrically for any change in the I_D vs V_{DS} (I/V) characteristics. The MESFETs were examined with an optical microscope mounted on the wafer prober and were also examined for detailed breakdown effects using a scanning electron microscope.

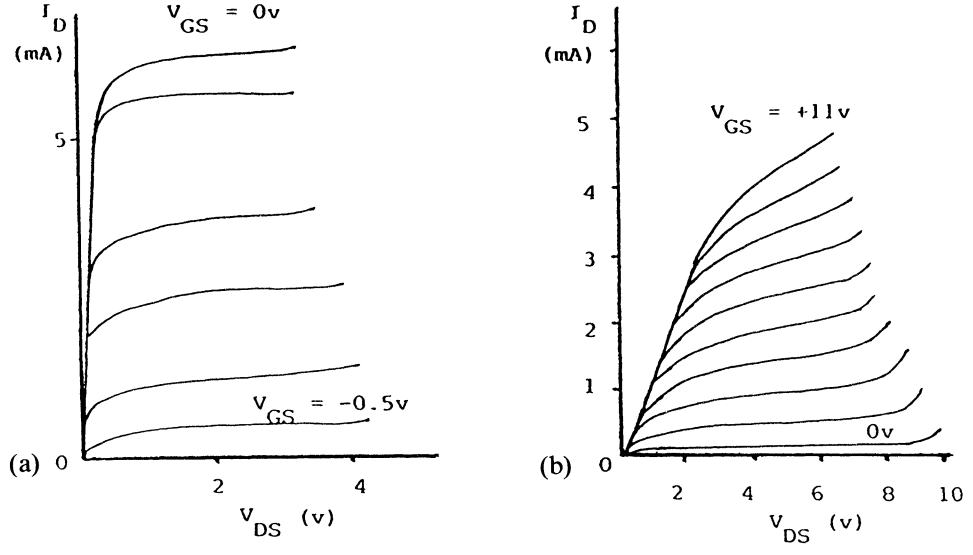

FIGURE 4 Typical I/V plots for devices (category 1). (a) MESFET, (b) MOSFET

4 RESULTS

4.1 Characteristics

In both cases the degradation after the application of one ESD pulse to the gate could be classified into one of 4 categories, although with the NMOS devices the behaviour is more complex.[3] These categories are based on the electrical I/V curves for the transistors before and after each pulse.

4.1.1 Category 1 - No change. All electrical parameters remain unaltered and the I/V curves, as seen in Figures 4a and b remain the same.

4.1.2 Category 2 - Degraded characteristic. Typical I/V curves are shown in Figure 5a and b. The degradation manifests itself as a decrease in g_m (transconductance) and an increase in I_{GL}, the gate leakage current to source or drain.

4.1.3 Category 3 - Partial Burnout. This category is still not indicative of complete breakdown. It is encountered when burnout is between the gate and source only, (Figure 6(a), (c)) or gate and drain only (Figure 6(b), (d)). It has been found that if partial burnout occurs, in 95% of occasions it is between gate and source. The NMOS breakdown point, and probability of breakdown, also depend on the gate dimensions[3], at any given voltage.

4.1.4 Category 4 - Total Burnout. This state is reached in the case of the MESFET when the I/V curves show constant resistive properties for all drain/source configurations

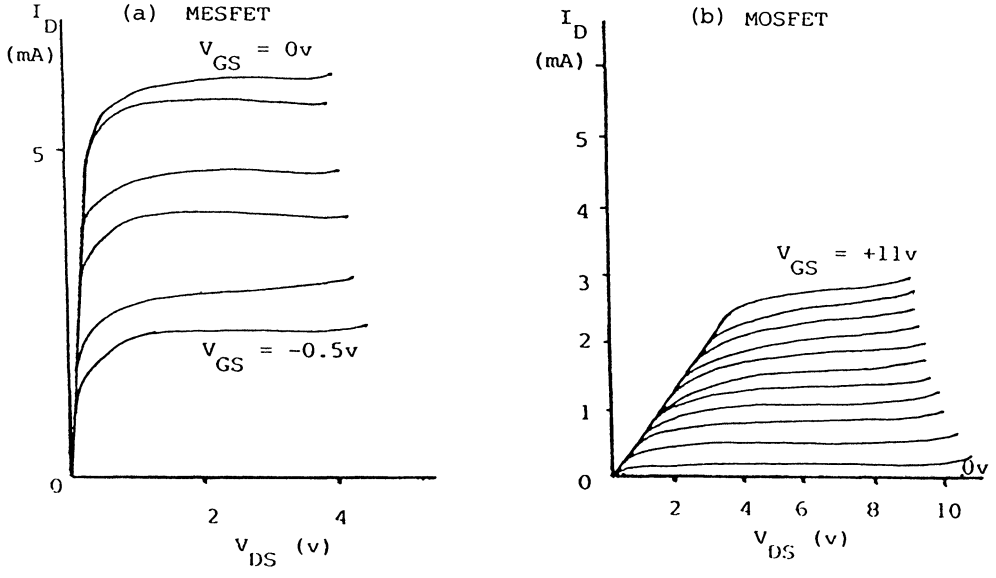

FIGURE 5 Typical I/V plots for devices showing degradation (category 2) (a) MESFET, (b) MOSFET

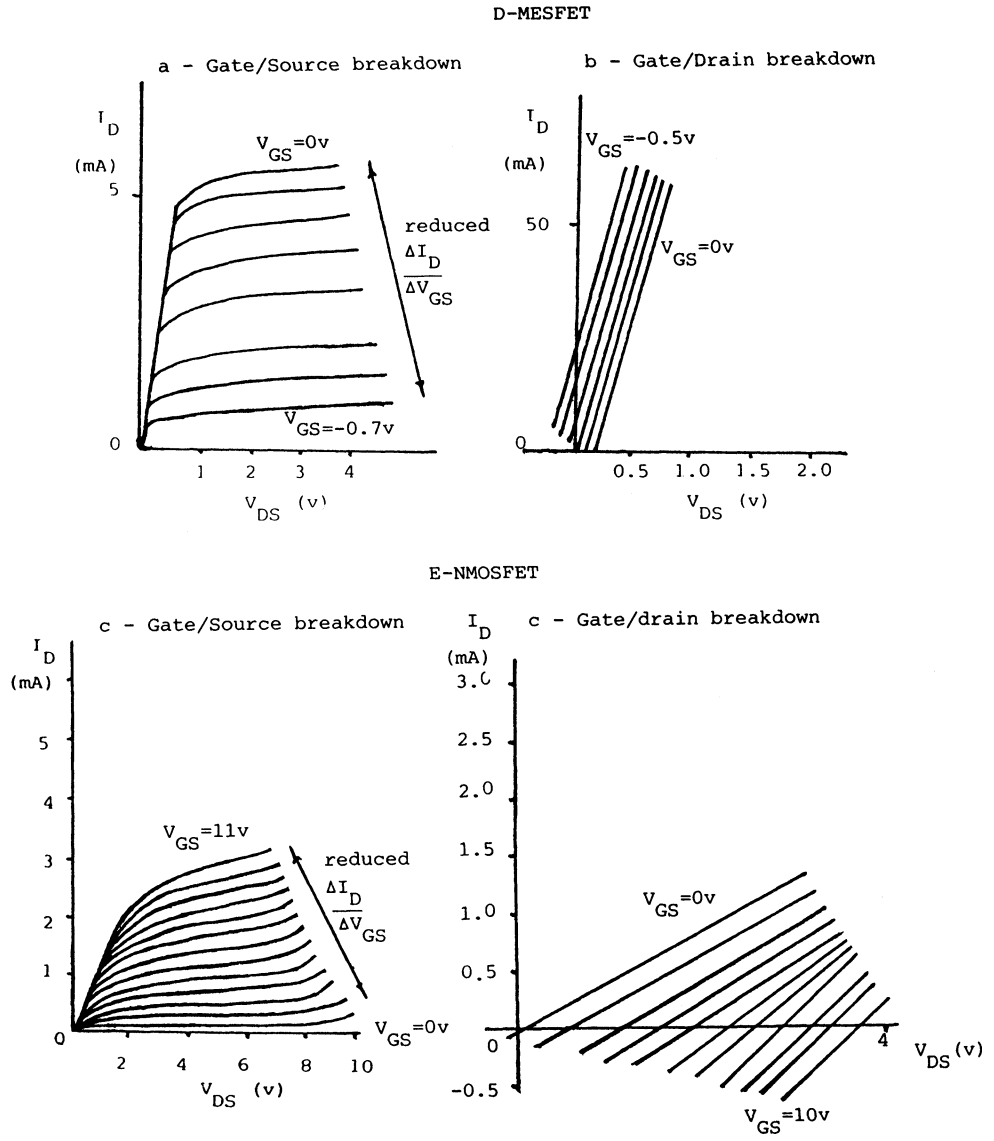

FIGURE 6 Partial Burnout Characteristics (Category 3). (a) Gate/Source breakdown, (b) Gate/Drain breakdown, (c) Gate/Source breakdown, (d) Gate/Drain breakdown.

(Figure 6(b)). In the case of the NMOS structures total burnout is defined when $I_D = 0$ for all values of V_{DS} and V_{GS}, or constant resistance properties (Figure 6(d)) for all drain/source configurations.

4.2 Voltage Effects

The voltages applied to the gate have a significant effect on the degradation of the

devices. It should be noted that it was not found possible to predict the exact behaviour of any one device and the figures given must be interpreted as statistical results found by measuring large numbers of devices.

At voltages between +200 and +800v the MESFETs fell into category 2, (a degraded characteristic) after the application of a single pulse. The NMOS FETs fell into category 2 between +50 and +200v. In both cases voltages lower than the stated minimum kept the devices in category 1. (No change observed).

Category 3, (partial burnout), was encountered for the MESFETs between +800 and +1kv and for the NMOS FETs between +200 and +300v.

For MESFETs, 5% of the partial burnout cases occurred between gate and drain. This was traced to the gate misalignment in the channel region.

Finally, category 4, (total burnout), was observed at voltages greater than +1kv (MESFETs) and +300v (NMOS FETs).

4.3 Polarity Effects

In both cases a polarity effect was evident. In section 4.2 the voltage magnitudes quoted for a given degradation category can be roughly halved for negative polarity pulses. This is shown in Table I. These polarity effects have been observed for MESFETs in other voltage stress situations.[7,9]

4.4 Temperature Effects

No detailed studies of the effect of temperature on changes in the I/V characteristic caused by a single ESD pulse have been made in the present work for the MESFETs. However, for the MOSFET devices it has been shown[3] that temperature change has a negligible effect on the voltage degradation behaviour as described in paragraph 4.2.

4.5 Cumulative Pulse Effects

The cumulative effects of pulsing the gates of the devices resulted in degradation (category 2), eventually leading to partial burnout (category 3) and in some cases total burnout (category 4). The extent of degradation could not be predicted but there was an overall dependence on the voltage magnitude and polarity of the pulse.

TABLE I
Normal operation and breakdown voltages of the devices

	GaAs D-MESFET	Si E-NMOS FET
Normal operation	d.c. operation -ve gate voltage to turn off device (−1.5v)	d.c. operation +ve gate voltage to turn-on device (+10v)
ESD +ve pulse breakdown (partial)	In the range +800v to 1 Kv	In the range +200 to 300v
ESD -ve pulse breakdown (partial)	In the range -400 to 500v	In the range −100 to 200v
Breakdown path	95% - Gate/Source 5% - Gate/Drain	Oxide

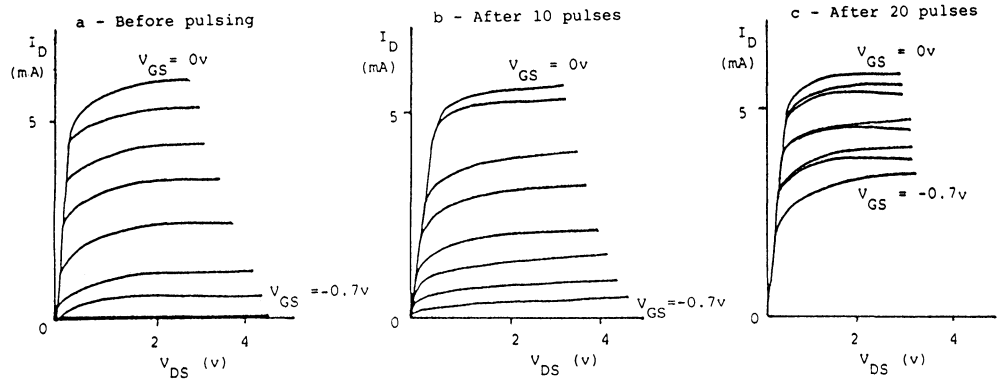

FIGURE 7 Degradation of the transconductance for a GaAs MESFET as a function of the number of ESD pulses applied to the gate

Figure 7a, b, and c shows the degradation of MESFETs subject to +600v pulses as a function of the number of pulses applied. It can be seen that the transconductance is decreasing and in many cases the transistors degrade to the single I/V curve normally associated with zero V_{GS}, for all values of V_{GS}.

The NMOS FETs degraded to zero I_{DS} for all V_{DS}, V_{GS}, or degraded until total burnout was obtained.

4.6 Physical changes after the application of an ESD pulse

After the application of an ESD pulse to the gate of a MESFET any changes in appearance along the gate or in the channel was noted. Due to the vertical nature of the NMOS FETs this was not possible for these structures. After the application of a pulse of sufficient magnitude to cause severe degradation, or partial burnout, a discolouration of the gate/source region occurred. If total burnout was encountered the discolouration extended across the channel region from drain to source. In general, partial burnout resulted in discolouration between source and gate, but sometimes it occurred between gate and drain. This however was traced to misalignment of the gate, moving the gate nearer the drain than the source.

S.E.M. analysis of the channel region, after removal of the passivation revealed greater damage to the source electrode than the gate electrode, for negative pulse. This is clearly shown in Figure 8. Similar damage to the gate electrode for positive pulses has yet to be found.

5 DISCUSSION

5.1 Degradation Characteristics

In both devices, degraded characteristics were manifested as a decrease in transconductance. This can be explained by a leakage path existing in:-

a) The channel between gate and source (MESFET).

b) The channel between gate and drain (MESFET).

c) The oxide either to the source, drain or channel (NMOS FET).

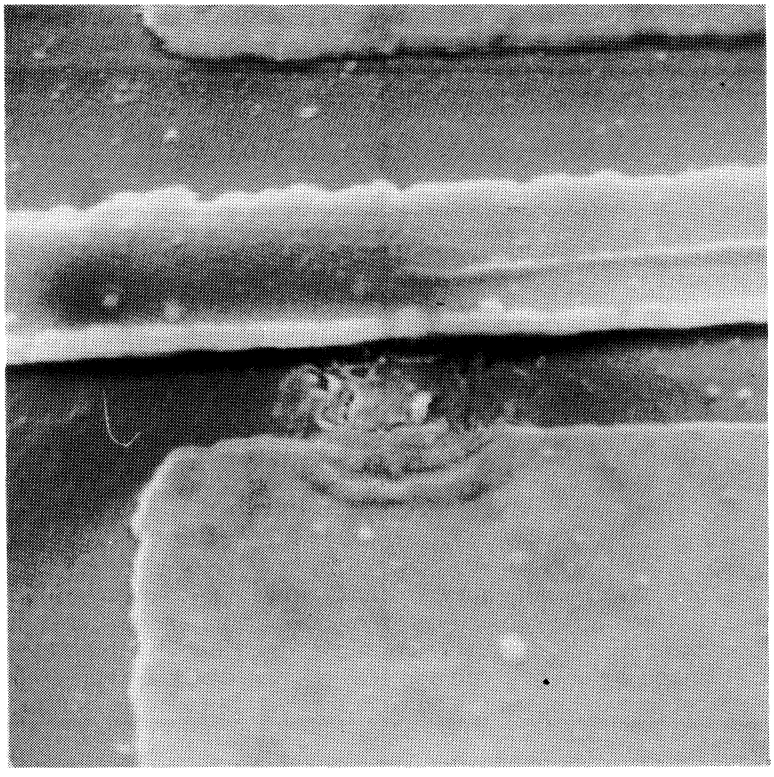

FIGURE 8 SEM of breakdown between source and gate in the channel region

In the MESFET the leakage resistance between gate and source acts like a current sink for the gate circuit. This gate current is normally negligible. Degraded transconductance (partial burnout) is a function of the voltage drop at the gate electrode caused by a decrease in the leakage resistance. In the other partial burnout case, i.e. between gate and drain, the gate current is added directly into the drain current measurement circuit, and will simply cause linear I/V characteristics which are dependent on the gate voltage.

In the NMOS devices, Category 2, 3 or 4 behaviour will depend on the position of the leakage path in the oxide. If the breakdown is between oxide and the drain (or source) then partial burnout will be obtained. If the breakdown is directly over the channel then total burnout will occur.

In both cases, after a single low voltage pulse, the devices that show 'degraded characteristics' would still be capable of digital operation. They would, however, be potential failures later in life. Such devices are thus often referred to as "walking wounded". In such cases, the leakage resistance of both types of devices will still be relatively large.

5.2 Cumulative Pulse Effects

In both devices cumulative degradation effects were present. It is postulated that the

MESFETs degraded because the leakage path resistance decreased with each pulse. This decreased resistance manifested itself as a decrease in the transconductance.

The NMOS FETs degraded as explained in section 5.1 but the degradation category depended on the nature of the leakage path within the oxide.

5.3 Polarity Effects on ESD Sensitivity

In both types of device it was found that a negative polarity would tend to degrade the device to a greater extent than a positive pulse.

In the MESFET case, the action of the Schottky barrier under voltage stress is different for each polarity. This would account for the observed effect. (See para. 5.5) In the case of the NMOS FETs the breakdown is through the oxide and would be expected to be polarity independent.[12] However studies on MOS capacitor structures[10] have led to the conclusion that surface charge effects[11] under the gate oxide will affect the extent of breakdown for a given voltage and this will involve polarity behaviour.

5.4 Physical Changes due to ESD Breakdown

The GaAs MESFETs generally burnt out between gate and source and this can be explained by considering the geometrical arrangement of the channel/gate region. (The gate/source spacing is 1 μm while the gate/drain is 2 μm.) Since both of these electrodes are earthed then the highest field will normally be created between gate and source. In 5% of the partial burnout cases, the burnout was between gate and drain. This was traced to the gate misalignment in the channel region. It is postulated that the ohmic contacts have uneven edges which may also extend into the channel region creating localised high field points. The breakdown should initiate at the opposite electrode to the current injection, as observed in the SEM micrographs. This effect has also been reported with D.C. drain/source breakdown.[7,9]

The NMOS FETs showed no observable changes after pulsing.

5.5 Schottky Barrier Effects (MESFETs)

A detailed analysis of the part played by the Schottky barrier in the degradation of MESFET devices subject to ESD pulses, is being undertaken in the present study. However, data is needed on both temperature and continuous voltage effects before a model can be presented. It is clear however that when a negative pulse is applied to the gate, the depletion region will extend deep into the substrate, while in the positive case a depletion region no longer exists.

5.6 Oxide Breakdown (MOSFETs)

Analysis of the results that have been obtained indicate that leakage paths created in the oxide can account for the changes in the I/V curves obtained. The position of the breakdown in the oxide will determine the changes in breakdown characteristics.

Previous work[4,5,6,8] indicated that oxide breakdown under transient high voltage stress was due to an electron cascade caused by avalanche breakdown (impact ionisation) within the oxide. Oxide defects,[3] present after growth, will influence the point of breakdown within the oxide. Also surface charge effects[10] will affect the breakdown point.

6 CONCLUSIONS

Degradation and burnout characteristics of GaAs MESFETs and Si NMOS FETs have been investigated.

It is concluded that degradation in the MESFETs is due to a leakage path forming at a high field point in the gate/source region. The probability of failure is governed by the polarity and magnitude of the applied ESD pulse.

In the NMOS FETs, degradation is due to oxide breakdown by impact ionisation within the oxide. The position and probability of failure mode is also influenced by polarity and magnitude of the applied ESD pulse.

7 ACKNOWLEDGEMENTS

We wish to thank Plessey Research (Caswell) Ltd. for supplying the NMOS test wafers and STC Components Ltd. for the GaAs MESFET wafers.

In detail we would like to thank Bill Holt, Roy Oakley and Nick Armstrong from Plessey and Richard Butlin, Ron Eggar and Steve Bland from STC for their support and advice.

One of us (AJF) is grateful for support from STC Components Group and the other (EAA) is grateful for support from the MOD Procurement Executive (DCVD).

The original version of this paper was presented at the ERA Seminar on Electrostatic Discharge Damage in Electronics, London, 8th May, 1986[13] and we are grateful to the organisation for permission to re-use some of the material.

REFERENCES

1. Amerasekera, E.A., Campbell, D.S. *"Failure mechanisms in semi-conductor devices".* In the press, John Wiley, (1986).
2. MIL Standard Handbook, Method 3015.2, "Electrostatic discharge sensitivity classification", MIL STD 883C, p 1, August (1983).
3. Amerasekera, E.A., Campbell, D.S. "Electrostatic pulse breakdown in NMOS devices." *Quality and Reliability Engineering International,* **2,** pp 107–116, (1986).
4. Di Stefano, T.H., Shatzke, M. "Dielectric instability and breakdown in wide bandgap insulators". *J. Vac. Sci. Technol.* **12,** pp 37–46, (1975).
5. Klein, N. "Electrical breakdown in thin dielectric films". *J. Electrochem Soc.* **116,** pp 963–972, (1969).
6. Ferry, D.K. "Electron transport and breakdown in SiO_2". *J. Appl. Phys.* **50,** pp 1422–1427, (1979).
7. Irie, T., Nagasako, I., Kohzu, H., Sekido, K. "Reliability study of GaAs MESFETs". *IEEE Trans. Micro. Theo. and Tech.* MTT**24,** pp 321–328, (1976).
8 Harari, E. "Dielectric breakdown in electrically stressed thin films of thermal SiO_2." *J. Appl. Phys.* **49,** pp 2478–2489, (1978).
9 Huang, C.L., Kwan, F., Wang, S.Y., Galle, P., Barrera, J. "Reliability aspects of small signal GaAs FETs". *Proc. Rel. Phys. Symp.* pp 143–147, San Francisco, (1979).
10 Amerasekera, E.A., Campbell, D.S. "ESD pulse and continuous voltage breakdown in MOS capacitor structures". To be published. *EOS/ESD Symp., Las Vegas, September,* (1986).
11 Amerasekera, E.A., Campbell, D.S. "Oxide breakdown in MOS structures under ESD and continuous voltage stress conditions." *Proc. RELCON '86* pp 325–330, (1986).
12 Osburn, C.M., Ormond, D.W. "Dielectric breakdown in SiO_2 films on silicon". *J. Electrochem. Soc.* **119,** pp 591–596, (1972).
13 Franklin, A.J., Amerasekera, E.A., Campbell, D.S. "A comparison between GaAs MESFET and Si NMOS ESD behaviour", *Proc. Electrostatic Discharge Damage in Electronics (ERA Seminar), Regent Crest Hotel, London, 8th May, 1986, pp 4.3.1.–4.3.3.*