

LAYOUT AND THERMAL ANALYSIS OF POWER DEVICES USING A PC/XT

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Thermal analysis during the design process is an essential step towards the achievement of high reliability in modern high density hybrid and integrated circuits. Thermal analysis is also essential for modern, high density PCBs. Traditionally, a solution of the thermal problem is obtained by either the method of finite differences or the method of finite elements. Both methods, however, require a fine 3-D partition of the substrate, leading to large systems of linear equations the solution of which demands substantial computing power provided by number crunching machines and/or powerful computer workstations.

The widespread use of personal computers, however, dictates the development of new approaches to the thermal problems so that a design engineer can solve them in reasonable time with a PC. A new treatment of steady-state thermal analysis combined with a layout editor is proposed in this paper, which makes use of the analytical solution for the temperature distribution in a single-layer substrate with heat sources on the surface, and having an isothermal bottom surface. In this way the mathematical complexity of the problem is dramatically reduced allowing the thermal analysis of Multi Chip Modules (M.C.M.s) and complex hybrid circuits with the use of a PC/XT or compatible.

I. INTRODUCTION

Thermal analysis tools have become of fundamental importance for the design of high power hybrid and integrated circuits and also for modern high density PCBs. The increasing demand for higher packing densities together with the use of modern high power integrated circuits require the complete thermal analysis of packages in order to ensure the selection of the proper substrate and the optimal location of the components. Several tens of watts can be dissipated, by directly attaching high power ICs onto ceramic substrates and/or heat spreaders, as for example in the case of the so-called Multi Chip Modules (MCMs). The heat transfer in hybrid circuits can take place by all three known mechanisms, i.e. conduction, convection, and radiation. However, if the substrate is mounted on a heat sink, convective heat transfer becomes negligible compared with that due to conduction. Furthermore, the effect of heat transfer by radiation is assumed to be included in the heat transfer coefficient. Therefore, the steady-state heat transfer problem in hybrid microcircuits may be solved by considering it to be one of pure heat conduction.

The standard way of solving this problem is the 3-D finite element method. This method, however, requires the solution of large systems of linear equations which is a very time consuming process especially on a small computer. As the circuit

density rises, a finer 3-D grid must be used in order to approximate the solution satisfactorily¹. Thus, the higher the density of a hybrid microcircuit the larger the system of linear equations to be solved, making more acute the computer time problem. The originality of the present approach is to apply systematically principles that have been used in numerous works²⁻⁹ for the last decade, in order to meet the designer's requirements for layout and subsequent thermal analysis of hybrid circuits and MCMs, with the aid of a PC/XT.

The software package developed consists of two main modules: the layout editor and the thermal analysis programme. The layout editor allows the layout of the heat dissipating sources and the metal interconnecting paths, on a predefined grid of, spacing λ , which appears on the monitor. After the completion of the layout and during the storage procedure the conducting paths pattern is stored separately from the pattern of the heat dissipating sources. The file where the latter has been stored, contains the power density of all the cells of area λ^2 , where λ is the grid spacing used during the layout. The layout editor has been developed in PASCAL since this language offers a great variety of graphics subroutines.

The thermal analysis program uses as its input the power density distribution extracted during the storage procedure of the layout geometry and calculates the temperature distribution with the aid of the method which is discussed later. This program has been developed in FORTRAN to take advantage of the higher processing speed offered in conjunction with the presence of a 8087 coprocessor.

The results are kept in a file that is used as an input file to a commercial 3D graphics package named ENER GRAPHICS for a quick qualitative inspection of temperature distribution on the screen of the PC/XT. In any case the file can be printed on the screen and/or a printer.

The flow chart of the complete software package developed in the framework of the paper is shown in Fig. 1.

II. THE METHOD USED FOR THERMAL ANALYSIS

The proposed method is a numerical one but it offers a substantial reduction of mathematical complexity in comparison to other numerical methods¹⁰⁻¹³, such as finite elements or finite differences. This is because the method takes into account the analytical form of the solution of the thermal problem. The method is described in this section with the aid of arbitrary circuit shown in Fig. 2.

Line shaded areas on the top surface of the substrate represent heat producing sources which may be either printed resistors and/or any active device. The black area shown at the bottom surface represents a suitable heat sink which ensures an isothermal bottom surface, at ambient temperature.

The following assumptions have been made:

- a.] The rear (lower) surface of the substrate is kept at ambient temperature with the aid of a heat sink. This is a realistic assumption for modern, high power hybrid circuits.
- b.] Thermal conductivity, k , of the substrate is independent of temperature, T and it is isotropic.

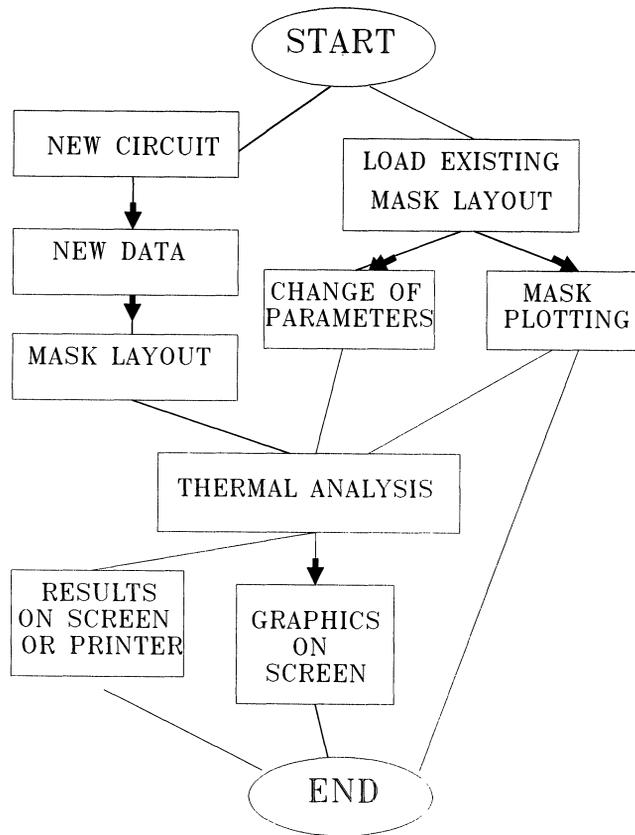


FIGURE 1 The flow chart of the developed software package.

c.] A small and negligible heat transfer is taking place at the substrate edges. This assumption is valid since the substrate thickness, t , is much smaller than its longitudinal dimensions L_1, L_2 , i.e. $t \ll L_1, L_2$.

d.] Heat transfer by radiation is accounted for by the heat transfer coefficient.

With these conditions, for any distribution of the power density $P(X, Y)$ dissipated at the upper surface, the steady-state temperature rise $T(X, Y, Z)$ is given by the solution of Laplace's equation:

$$\nabla^2 T = 0 \quad (1)$$

The boundary conditions associated with this equation are:

- i. At $Z = t$: $T = T_{amb}$ by assumption (a). T_{amb} is the ambient temperature.
- ii. At $X = 0, X = L_1$: $\partial T / \partial x = 0$ and at $Y = 0, Y = L_2$: $\partial T / \partial y = 0$ by assumption (c).
- iii. At $Z = 0$: $\partial T / \partial z = f(X, Y) = -P(X, Y)/k$, where $P(X, Y)$ is the heat flux

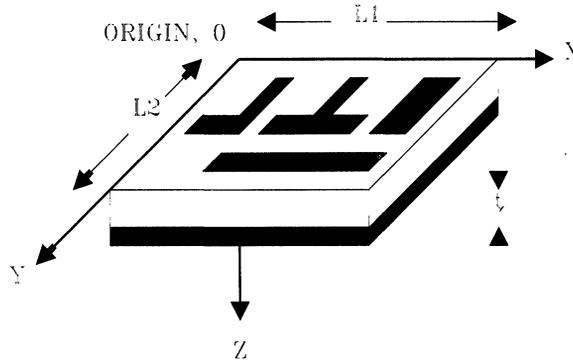


FIGURE 2 An arbitrary hybrid circuit (see text for details).

at the point (X, Y) . This boundary condition accounts for the Fourier conduction Law:

$$P(X, Y) = k \cdot \bar{z} \cdot \nabla T \quad (2)$$

where $-\bar{z}$ is the outward unit vector normal to the upper surface of the substrate. The Laplace equation will be solved with the well known technique of separation of variables. In order to apply this method, it is necessary to evenly extend the function $f(X, Y)$ in the range $|X| < L_1$ and $|Y| < L_2$, as shown in Fig. 3, so that

$$f(X, Y) = f(-X, Y) = f(X, -Y) = f(-X, -Y). \quad (3)$$

The eigenvalues of the Laplace equation in cartesian coordinates are the following complex exponentials¹⁴:

$$e^{jk_x X}, e^{jk_y Y}, e^{jk_z Z} \quad (4)$$

where k_x , k_y , and k_z are the unknown eigenvalues to be calculated. Since $f(X, Y)$ is even in the range $|X| < L_1$ and $|Y| < L_2$, the linear combination of the eigenfunctions

$$e^{jk_x X}, e^{jk_y Y}$$

generates the cosine functions $\cos(k_x X)$ and $\cos(k_y Y)$. In relation to assumption (c), i.e. no heat loss is taking place from the substrate edges, this provides the corresponding eigenvalues, since: if $\sin(k_x X) = 0$ at $X = 0, L_1$ then $k_x = n\pi/L_1$. In the same way $k_y = m\pi/L_2$. The general solution of the temperature distribution across the substrate can thus be represented on the basis of the eigenvectors of $\nabla^2 T = 0$ as:

$$T = T_{amb} + \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} C_{nm} e^{j(n\pi/L_1)X} e^{j(m\pi/L_2)Y} \sinh(k_{nm}(Z - t)) \quad (5)$$

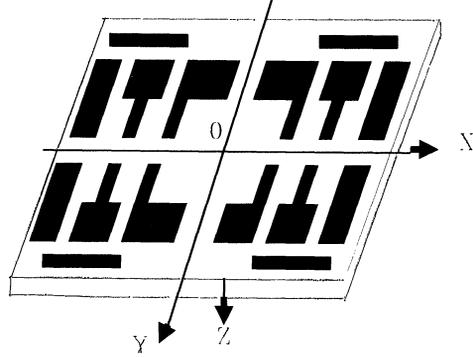


FIGURE 3 Modification of the circuit in order to apply the proposed method.

for

$$0 \leq X \leq L_1$$

$$0 \leq Y \leq L_2$$

and where:

$$k_{nm} = \sqrt{\left[\left(\frac{n\pi}{L_1}\right)^2 + \left(\frac{m\pi}{L_2}\right)^2\right]}$$

The only unknown in the latter equation is the coefficient C_{nm} . It is worth noting here that once C_{nm} has been evaluated for a given thermal density pattern, equation (5) can provide the temperature distribution for any thickness, t , of the substrate without it being necessary to re-evaluate coefficient C_{nm} . The orthogonality of the eigenfunctions, i.e.

$$\int_{-1}^{+1} e^{j(n\pi/L)\omega} e^{-j(m\pi/L)\omega} d\omega = \begin{cases} 2l & \text{if } n = m \\ 0 & \text{otherwise} \end{cases} \quad (6)$$

applied to boundary condition (c), which takes the following form if equation (5) is taken into consideration:

$$f(X, Y) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} C_{nm} e^{j(n\pi/L_1)X} e^{j(m\pi/L_2)Y} k_{nm} \cosh(k_{nm}t) \quad (7)$$

provides the following expression for C_{nm} :

$$C_{nm} = \frac{\int_{-L_1}^{L_1} \int_{-L_2}^{L_2} f(XY) e^{-j(n\pi/L_1)X} e^{-j(m\pi/L_2)Y} dX dY}{4k_{nm}L_1L_2 \cosh(k_{nm}t)} \quad (8)$$

The numerator of equation (8) can be easily found by a 2-D Fast Fourier Transform (FFT) which has complexity $\ln[N]$, where N is the number of points used to approximate the function $f(X, Y)$ ¹⁵.

Subsequent substitution of the calculated coefficient C_{nm} in equation (5) yields the analytical solution of the thermal problem. For computer calculation a more convenient form of equation (5) can be obtained by exploiting the symmetry of (X, Y) . This symmetry leads to the expression below for C_{nm} :

$$\frac{\int_{-L_1}^{L_1} \int_{-L_2}^{L_2} f(X, Y) \cos\left(\frac{n\pi}{2L_1} X\right) \cos\left(\frac{m\pi}{2L_2} Y\right) d^X d^Y}{k_{nm} L_1 L_2 \cosh(k_{nm} t)} \quad (9)$$

Factor k_{nm} in the denominator of equation (9) assures that the product $C_{nm} \sinh(k_{nm}[Z - t])$ in equation 5 tends rapidly to zero, thus minimizing the number of terms of C_{nm} which must be calculated in order to achieve the required accuracy for the calculated temperature distribution.

The accuracy of the solution depends on the value selected for the grid spacing, λ , during the layout of the heat dissipation sources. Indicatively, grid spacing, λ , should correspond to the smallest geometric feature (length or width) of the heat dissipation sources.

Also, the obtained accuracy depends on the number of terms of C_{nm} , that has been decided to be summed. It may be worth noting here that when the size of the heat source is much smaller than the substrate size, the number of terms of C_{nm} that have to be summed in order to obtain an accurate results is relatively high. For example in the case of $100\text{mm} \times 10\text{mm}$ substrate with a single $1\text{mm} \times 1\text{mm}$ heat source, about 300×300 terms have to be summed in order to obtain an accuracy of 86%, in relation to the solution obtained for the same problem when 900×900 terms (and 1200×1200 terms) had been summed. From the previous equation, it is apparent that the coefficient C_{nm} possesses the following property:

$$C_{nm} = C_{-nm} = C_{n-m} = C_{-n-m} \quad (10)$$

Applying the property shown in (10) in equation (5), a convenient form is obtained for the temperature distribution over the substrate:

$$\begin{aligned} T = & T_{\text{amb}} + C_{00} \sinh(k_{00}(Z - t)) + \\ & + 2 \sum_{n=1}^{\infty} C_{n0} \cos\left(\frac{n\pi}{4} X\right) \sinh(k_{n0}(Z - t)) + \\ & + 2 \sum_{m=1}^{\infty} C_{0m} \cos\left(\frac{m\pi}{L_2} Y\right) \sinh(k_{0m}(Z - t)) + \\ & + 4 \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} C_{nm} \cos\left(\frac{n\pi}{L_1} X\right) \cos\left(\frac{m\pi}{L_2} Y\right) \sinh(k_{nm}(Z - t)) \quad (1) \end{aligned}$$

Expression (11) involves no complex arithmetic and contains positive summation indices only.

To perfect the transposition of the real problem into an homogeneous infinite space, it is necessary to include the case in which thermal conductivity is temperature dependent. This is true for materials like silicon, alumina, and beryllium oxide. Kirchoff's transform¹⁶ allows the calculation of a fictitious temperature T^* :

$$T^* = (1/k_0) \int_{T_0}^T k(T) dT \quad (12)$$

where T is the real temperature and $k_0 = k(T_0)$ is the thermal conductivity corresponding to the reference temperature T_0 . This transform reduces the heat diffusion equation $\nabla\{k(T) \cdot \nabla T\} = 0$ to the Laplace's equation $\nabla^2 T^* = 0$, with boundary conditions applied to T^* and/or to the normal derivative $\partial T^* / \partial z$. So the calculations can be carried out as for a material with constant k as it has been assumed at the beginning of this paper. The real temperature in the case of temperature dependent thermal conductivity may then be deduced from T^* applying the inverse transform of equation (12).

III. THE LAYOUT EDITOR

The layout editor is a menu driven software package, developed in PASCAL, which allows the graphical design of the masks required for the MCM or the hybrid circuit under consideration. Moreover, the editor provides means of producing hard copies of the masks on an x-y plotter (HITACHI-Model 672-XD). The layout editor consists of a number of routines the most indicative of which are listed below:

MAKEFRAME: plots the frame of the mask on the screen, independently of the actual size of the substrate which has been introduced.

MAKEGRID: produces a grid on the screen, of a constant, λ , to facilitate the movements and the accurate positioning of the cursor.

DRAWPATTERN: contains all the subroutines that are needed for the design of the masks.

INDEX: fills up two tables one with the powerflow assigned to each cell of the grid and another with the coordinates of the masks.

CURSOR and **MOVECURSOR:** allows for the creation of a cross-hair cursor on the screen and the movement of it with the aid of the arrow keys.

PLOTMASK: transforms the data obtained from **INDEX** into graphs on a Hitachi x-y plotter and it allows for a predefined ratio between the dimension of the plot and the required real size. It allows for the plotting of single masks or the plotting of one mask on the top of the other, i.e. conductor mask and resistor mask or conductor mask and dies of IC's.

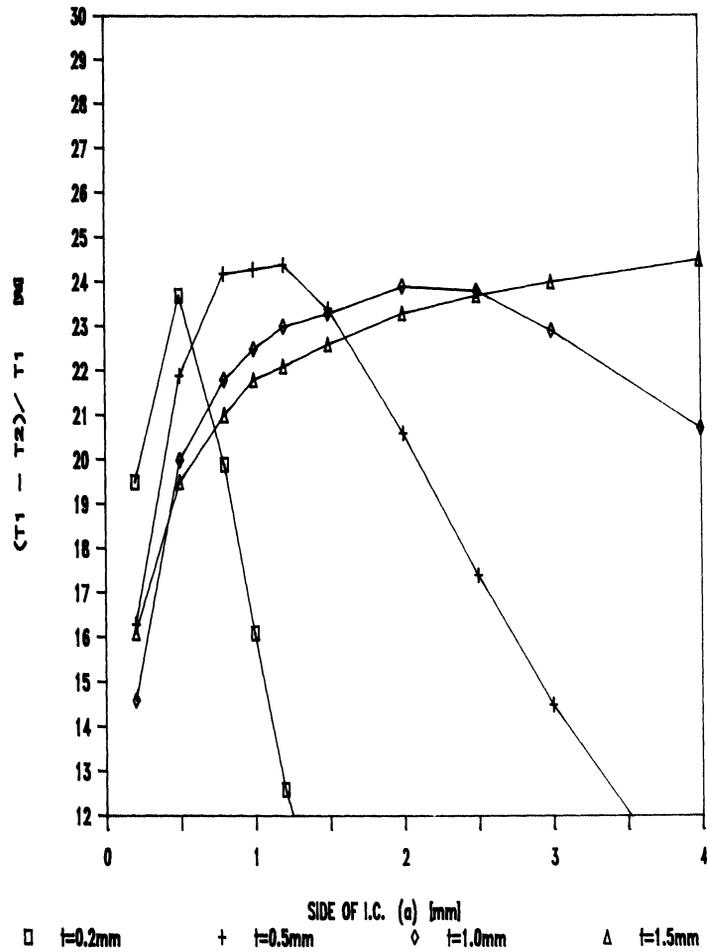


FIGURE 4 Percentile temperature differences against the edge of a square chip, for different substrate thicknesses, t .

IV. IMPLEMENTATION

For such tasks as temperature calculations, thermal coupling evaluation and component placement on the substrate the procedure is simple. It involves:

- a) Layout of the power source distribution related to the adiabatic faces, and typing through the keyboard the power dissipation values.
- b) Layout of the conducting paths.
- c) Plotting of the masks to the x-y plotter.
- d) Temperature calculation according to eq. 11.
- e) Temperature mapping in 3-D with the aid of ENER GRAPHICS.

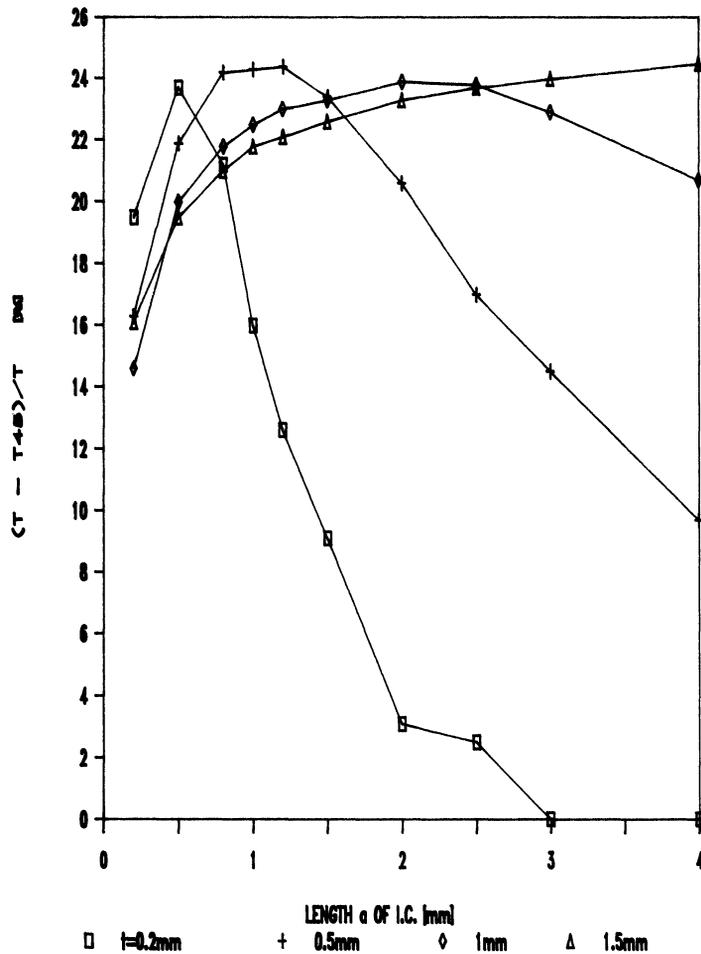


FIGURE 5 Percentile differences between the results obtained with the proposed method and the model of 45° , against the size of a square chip, and for different substrate thicknesses, t .

V. RESULTS

(a) The proposed method has been used for the thermal analysis in the case where a single square chip having an edge of length, a , and a constant power dissipation is attached to a substrate of thickness, t . More specifically the percentile difference between the temperature of the geometrical centre of the chip, T_1 , and that T_2 of the points of the chip lying on a circle of radius $r < a/2$ was examined as a function of thickness, t , of the substrate, and length, a , of the edge of the chip. This analysis would be very difficult to perform using conventional arithmetical methods which would require very fine grids to achieve satisfactory resolution.

Results produced are shown in Fig. 4, for $r = a/3$; for other values of r , the curves obtained maintained similar shapes. It is apparent that the percentile dif-

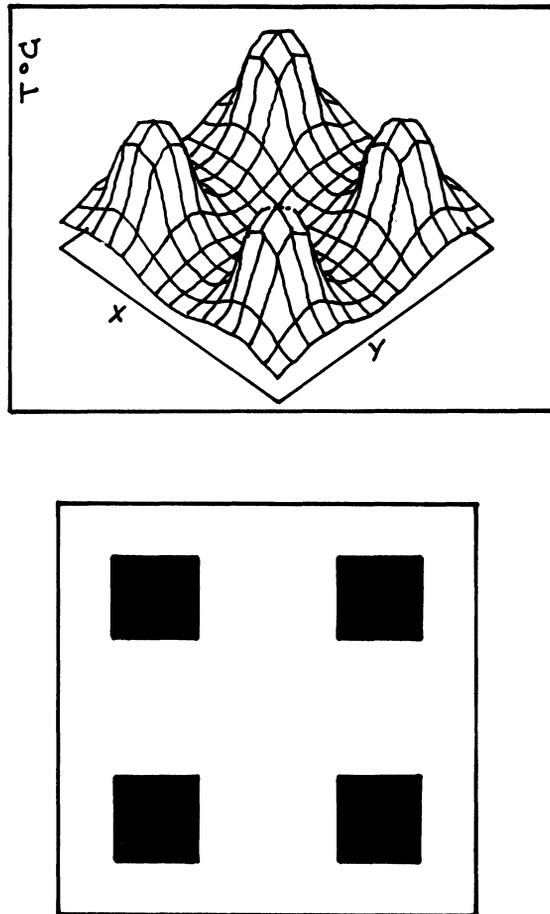


FIGURE 6 Layout of 4 dice and the corresponding temperature distribution on the upper surface of the ceramic substrate; the distance between them is $X = 5\text{mm}$ and $Y = 5\text{mm}$. Maximum temperature is seen to be 48°C .

ference reduces with decreasing ratio t/a . In other words, for a given chip, the temperature distribution becomes more uniform as the substrate thickness decreases. From a physical point of view this can be explained because as the thickness of the substrate decreases, longitudinal transfer of heat becomes negligible and the surface of the chip tends to become isothermal.

These results explain the discrepancies observed between temperature values, at the center of a square chip of edge a which is attached to a ceramic substrate, obtained with the use of the proposed method and the so-called model of 45° which is widely used in hybrid thermal design when isotropic substrates are considered^{17,18}.

The percentile difference of temperatures calculated by the two methods are plotted in Fig. 4 against the length of the edge of an integrated circuit, for various substrate thicknesses; it has been assumed that $P/k = 1$. Fig. 5 shows that for

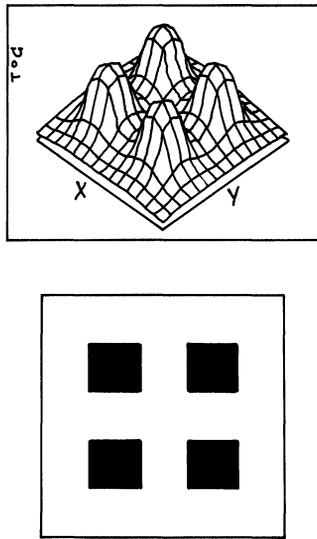


FIGURE 7 The 4 dice of Fig. 6 are 3mm; the temperature distribution on the upper surface of the ceramic substrate shows a maximum of 54°C.

relatively thick substrates temperature values, for the center of the chip, calculated with the 45° model are more than 30% lower, for a wide range of a , in comparison to the ones obtained by the proposed method; which are in full agreement with the results found by the analytical solution¹⁹.

(b) The software package developed in the framework of the present study has also been used in the case of four dice of ICs, positioned on a ceramic substrate, in order to show the temperature distribution on the surface of the substrate, as a function of the distance between the dice. To perform the calculation it has been assumed that:

- a] the dice are squares of edge $a = 3\text{mm}$,
- b] power density on the dice is $3\text{W}/\text{mm}^2$,
- c] the ceramic substrate has a thickness of $t = 1\text{mm}$, and a thermal conductivity of $25\text{W}/(\text{m}^2\text{K})$.

It is worth noting that the calculated temperatures are the differences between actual temperature values at a certain point at/or in the substrate, and the temperature of the heat sink which is assumed to be attached onto the ceramic substrate.

The results of this latter exercise are shown in Figs. 6–9. Please note that the maximum temperatures calculated are indicated in the corresponding figure legends. From these figures it is apparent that the temperature in the middle of each die increases from 48°C, above the heat sink temperature, to 81°C, when the dice are brought in contact from an initial distance of 5mm. Fig. 10 shows similar results for different numbers of chip dissipating power as in the previous case, and which are attached symmetrically on to a ceramic substrate.

(c) Finally, results are presented for a relatively complex hybrid circuit consisting

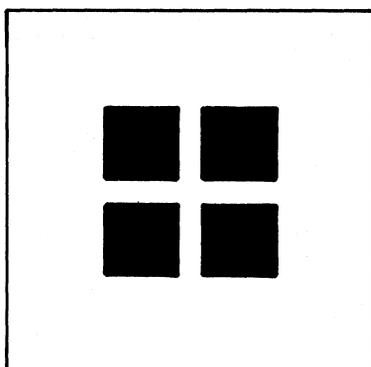
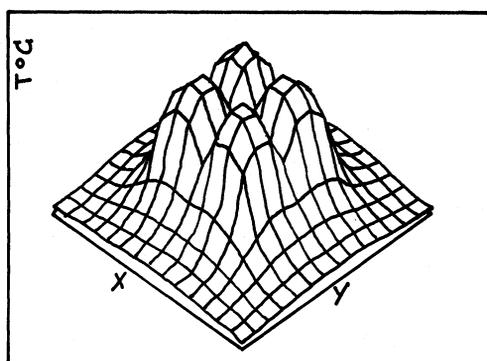


FIGURE 8 The dice of Fig. 6 are 1mm apart; the maximum temperature is now 61°C .

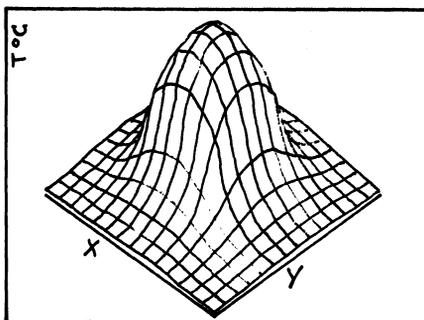


FIGURE 9 The dice of Fig. 8 are zero mm apart; the maximum temperature, on the upper surface of the substrate, is 81°C .

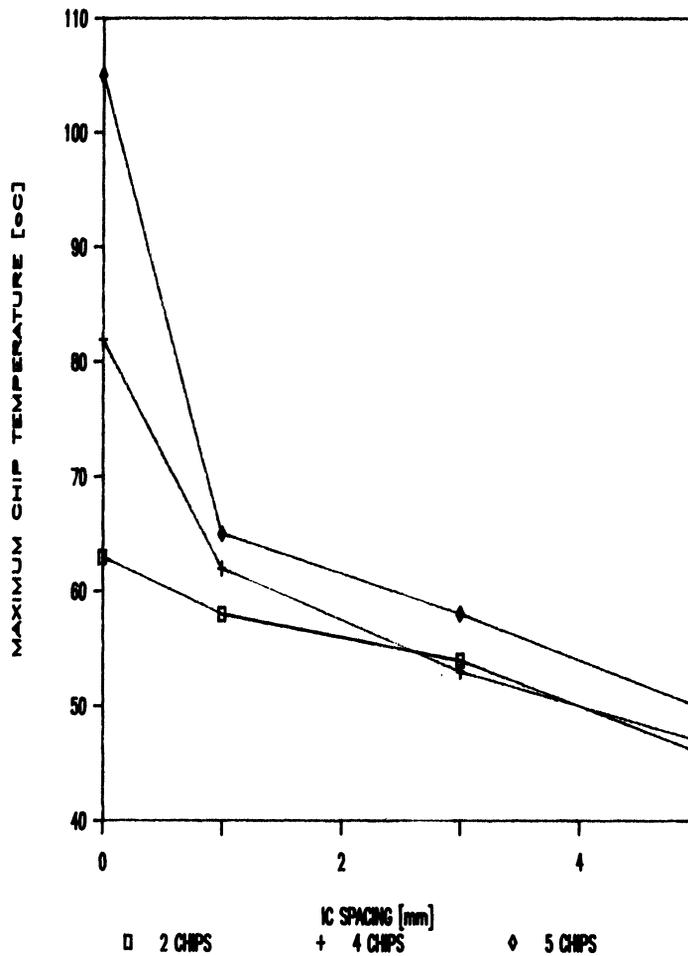


FIGURE 10 Calculated maximum temperature values at the center of dice against the distance between them, and as a function of the number of dice positioned on the substrate in a symmetrical manner.

of one metal layer and one resistor layer. The layout, which was accomplished with the aid of our layout editor, is shown in Fig. 11(b). The temperature distribution profile, at the surface of the ceramic substrate which contains the resistors, has been calculated with the aid of the method of thermal analysis already discussed, and is shown in Figure 11(a).

The assumptions made for these calculations are listed below:

substrate dimensions:	17mm × 15mm × 0.5mm
minimum resistor width:	1mm
thermal conductivity of the substrate:	25W/(m ² K)

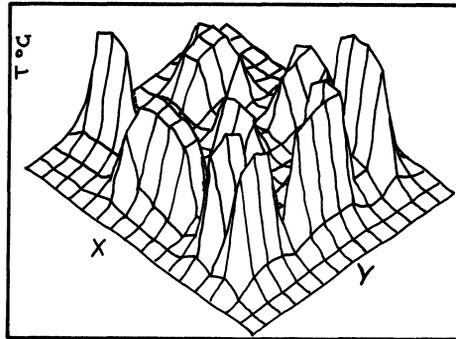


FIGURE 11(a) Temperature distribution profile of the thick film circuit shown in Fig. 11(b).

h parameter:	$1 \times 10^7 \text{W}/(\text{m}^2\text{K})$
power dissipation density:	$1 \text{W}/\text{mm}^2$
ambient temperature:	25°C

The maximum temperature calculated was 28°C above ambient. Incidentally the time required for the calculations and the presentation on the screen of the temperature profile was 4 min, using the 8087 co-processor in the computer. It may be worth noting that in the absence of the co-processor the time required for the solution of the previous problem was approximately 10 mins.

The high value for the parameter h, is indicative of the presence of a heat sink which keeps the temperature at the bottom surface of the ceramic substrate at the ambient temperature. However, if $h = 50$ for example, the computed results show a temperature distribution profile with maximum temperature calculated to be 454°C above ambient.

VI. CONCLUSIONS

A method for layout and thermal analysis of hybrid and Multi Chip Modules attached to a heat sink has been presented which can handle complex circuits with

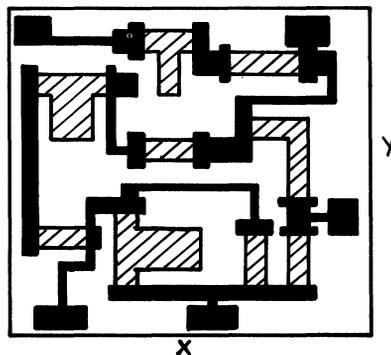


FIGURE 11(b) Thick film circuit layout. (Black areas are conductors, shaded areas are resistors.)

relatively reduced mathematical complexity. It is intended for the thermal analysis of plane structures most often encountered in semiconductor assemblies in the field of power electronics.

Results have been presented which show that the proposed method is capable of producing an estimation of temperature distributions in arbitrary circuits with the use of a personal computer. It seems to be suitable for the CAD of power electronic devices with respect to thermal aspects like computation of temperature values at sensitive points on the substrate, evaluation of the minimum distance between power dissipating components at the substrate surface and characterization of substrates.

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