

## SMALL-SIGNAL AND NOISE MODEL DETERMINATION FOR DOUBLE POLYSILICON SELF-ALIGNED BIPOLAR TRANSISTORS

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In this paper, noise characterization and modeling of a double polysilicon self-aligned bipolar transistor are presented. The device has been characterized in terms of noise and scattering parameters by means of an original automatic noise figure measuring system only. Measurements have been performed over the 1-4 GHz frequency range and at different bias conditions. The extracted model refers to the performance of the *chip* device since the package and bond parasitics have been accurately de-embedded by proper calibration techniques.

### INTRODUCTION

Consumer applications in the field of wireless communication systems (cellular phones, cellular data transceivers, local- and wide-area networks, etc.) at low microwave frequencies (up to 4 GHz) widely use silicon bipolar circuits due to the attractive features they offer in terms of performances, low cost technologies, chip count, and power consumption, which make them competitive alternatives to GaAs technologies. Today's advanced bipolar processes often use double polysilicon (i.e., polycrystalline silicon) self-aligned (PSA) schemes. The key issue is the self-alignment of the extrinsic base and the emitter, both of which are *outdiffused* and contacted with highly doped polysilicon layers separated by an oxide spacer.

The use of PSA technology allows for a remarkable increase of the common emitter current gain  $\beta$  and a smaller dependence of  $\beta$  itself on temperature as compared to conventional transistors.

In addition, PSA processes drastically reduce the base resistance and the collector-base capacitance, thus improving the device performance in terms of gain-bandwidth product, maximum oscillation frequency, and low power dissipation. Parasitics reduction also allows for scaling down both the lateral and the vertical dimensions of the transistor, thereby obtaining ultra-submicrometer junction depths [1, 2].

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In the aim of achieving an in-depth knowledge of the performance of this bipolar structure, we have characterized and modeled a packaged PSA device over the 1–4 GHz frequency range and at different bias conditions. The measurements of the eight scattering parameters and the four noise parameters have been carried out using only an automatic noise figure measuring set-up whose configuration has been implemented according to an original methodology and proper data processing techniques developed in our Lab [3, 4]. Since the characterization involves both scattering and noise parameters, we have extracted an accurate equivalent circuit model that includes noise sources.

To our knowledge, this is the first complete analysis reporting details on the microwave performance of a double PSA transistor. The results presented in this work are relevant to the preliminary part of an extensive experimental investigation (100 devices supporting 16 different topologies) on the influence of the geometrical size and shape of the PSA emitter upon the transistor performance. It is well known that small-geometry effects take place affecting device operation. Thus, only a careful and reliable characterization can provide the manufacturer clear information on the adjustment to be carried out on the relevant process parameters. (\*)

## IN-PACKAGE DEVICE CHARACTERIZATION AND EXTRACTION OF CHIP PARAMETERS BY DE-EMBEDDING

The *chip* device structure, whose schematic cross section is illustrated in Fig. 1, exhibits an effective emitter made out of 250 nm of N-poly and 50 nm of As-doped single crystal Si with an opening width of 200 nm. The intrinsic B-doped base thickness is 80 nm and the extrinsic base is contacted by P-poly, which is separated from the N-poly emitter contact by a sidewall oxide having a typical thickness of 300 nm. A Si-filled deep trench with self-aligned oxide cap isolation contributes to the reduction of the collector-base capacitance.

The device has been enclosed in a standard microwave-type package (100 mil square) to facilitate its handling and insertion into electronic equipment. The transistor terminal pads have been electrically connected to the metalized segments and to the grounding pattern of the package. From the enclosing body, the external leads provide a way of connecting the device to the circuit.

As a consequence, the package introduces a variety of parasitic elements that modify the device performance at microwave frequencies. Such parasitics have, therefore, to be identified in order to determine the performance intrinsic to the chip by applying a computational procedure known as *de-embedding*. That is, the chip characteristics are extracted by “peeling off” the scattering and noise correlation matrices of each parasitic element from the scattering and noise parameters referred to the external terminals, thus proceeding towards the inner circuit section until the chip configuration is reached. By doing so, the obtained measured values and the relevant model properties can be employed to provide feedback information for optimizing the chip manufacturing process.

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(\*)The devices are supplied by CoRiMMe (an SGS-Thomson Research Center, Catania, Italy).

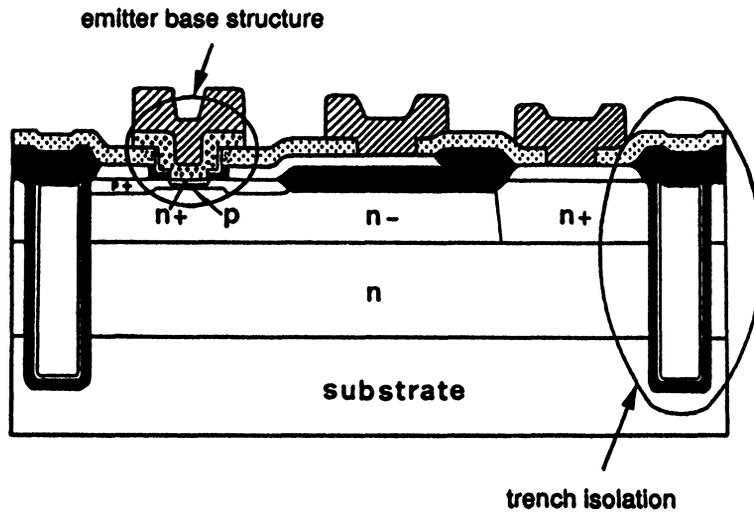


FIGURE 1 Schematic cross section of the PSA transistor

Knowledge of the parasitics features have been acquired through S-parameter measurements performed on special dummy loads, i.e., packages providing the *open*, *short*, and *thru* calibration layouts. By means of such measurements, it has been possible to extract an equivalent circuit that accurately models the effects introduced by the package (wire-bonding included) and its electrical contacts with the test fixture where the device is placed for testing. In Fig. 2, the modeled parasitic elements and the relevant element values are shown as a passive electrical network in which the device under test (DUT) is embedded.

The device characterization has been carried out over the 1–4 GHz frequency range and in the bias condition ranges  $V_{ce} = 2.5$  to 5 V,  $I_c = 1$  to 2 mA. The measuring system is presently operating in the 1–18 GHz range and over the  $-100$  to  $+100^\circ\text{C}$  temperature range by means of a thermocontrolled chamber. The im-

$A_1=0.2$ dB/m	$A_2=0.2$ dB/m
$LT_1=29.1$ mm	$LT_2=29.85$ mm
$C_{T1}=0.14$ fF	$C_{T2}=0.14$ fF
$C_{P1}=0.39$ fF	$C_{P2}=10.7$ fF
$C_{T12}=0.73$ fF	$C_{P12}=34$ fF
$R_{PB}=0.5$ $\Omega$	$L_{PB}=0.5$ nH
$R_{PC}=0.5$ $\Omega$	$L_{PC}=0.5$ nH
$R_{PE}=0.5$ $\Omega$	$L_{PE}=0.2$ nH

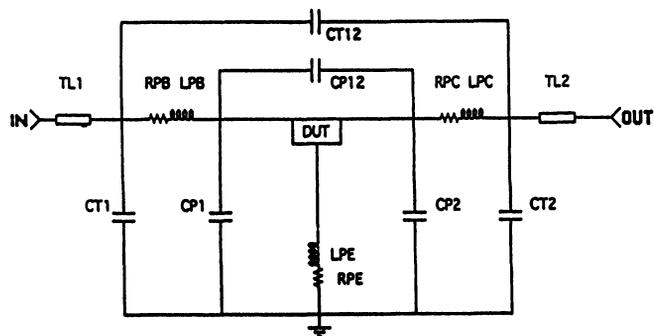


FIGURE 2 Equivalent circuit model of the parasitics introduced by the package with the relevant element values

plementation of a more compact version extended up to 40 GHz and to cryogenic temperatures directly on chip is in progress.

## EXTRACTION OF THE SMALL-SIGNAL AND NOISE MODEL OF THE PSA TRANSISTOR

The transistor chip model is a standard hybrid- $\pi$  structure where the effects due to distributed base resistance and distributed capacitance between intrinsic base and collector region have been introduced for an accurate representation of the transistor performance at microwave frequencies.

By de-embedding the effects of the previously described parasitics network from the measured parameter values, we obtained a different set of measured scattering and noise parameters, which refer directly to the chip device performance. The latter parameter sets have therefore been employed in the extraction of the chip model at the bias condition  $V_{ce} = 5$  V,  $I_c = 2$  mA.

The modeling procedure is based upon the minimization of the global error function, which accounts for the differences between the values of each measured and simulated parameter. It has been found that, for better final results, the optimum weights  $W_{ij}$  to be attributed to the different scattering parameter error functions during optimization should take on the following values:

$$W_{11} = 3, W_{12} = 0.5, W_{21} = 1.5, W_{22} = 0.6$$

The optimization cycles have been performed using commercial software CAD packages. The value of the  $g_m$  parameter stems from the application of the well-known relationship

$$g_m = I_c q/KT$$

which is a good approximation for small-signal operating devices. The model so determined is reported in Fig. 3 with the relevant element values. Sample results showing the model performance as compared to the measured parameters are reported in the graphs of Fig. 4.

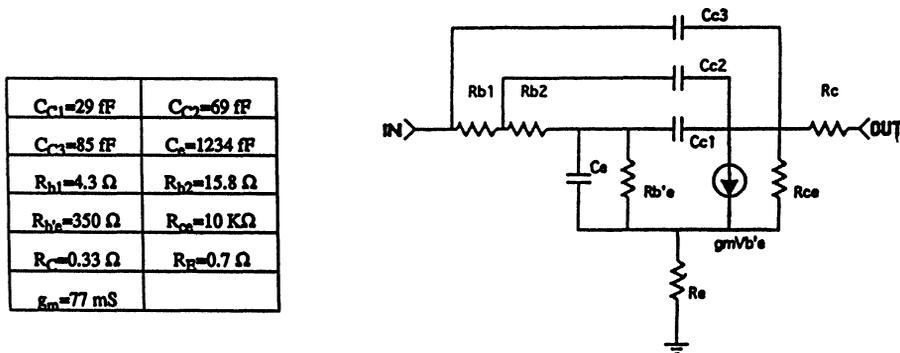


FIGURE 3 Equivalent circuit model of the chip device with the relevant element values

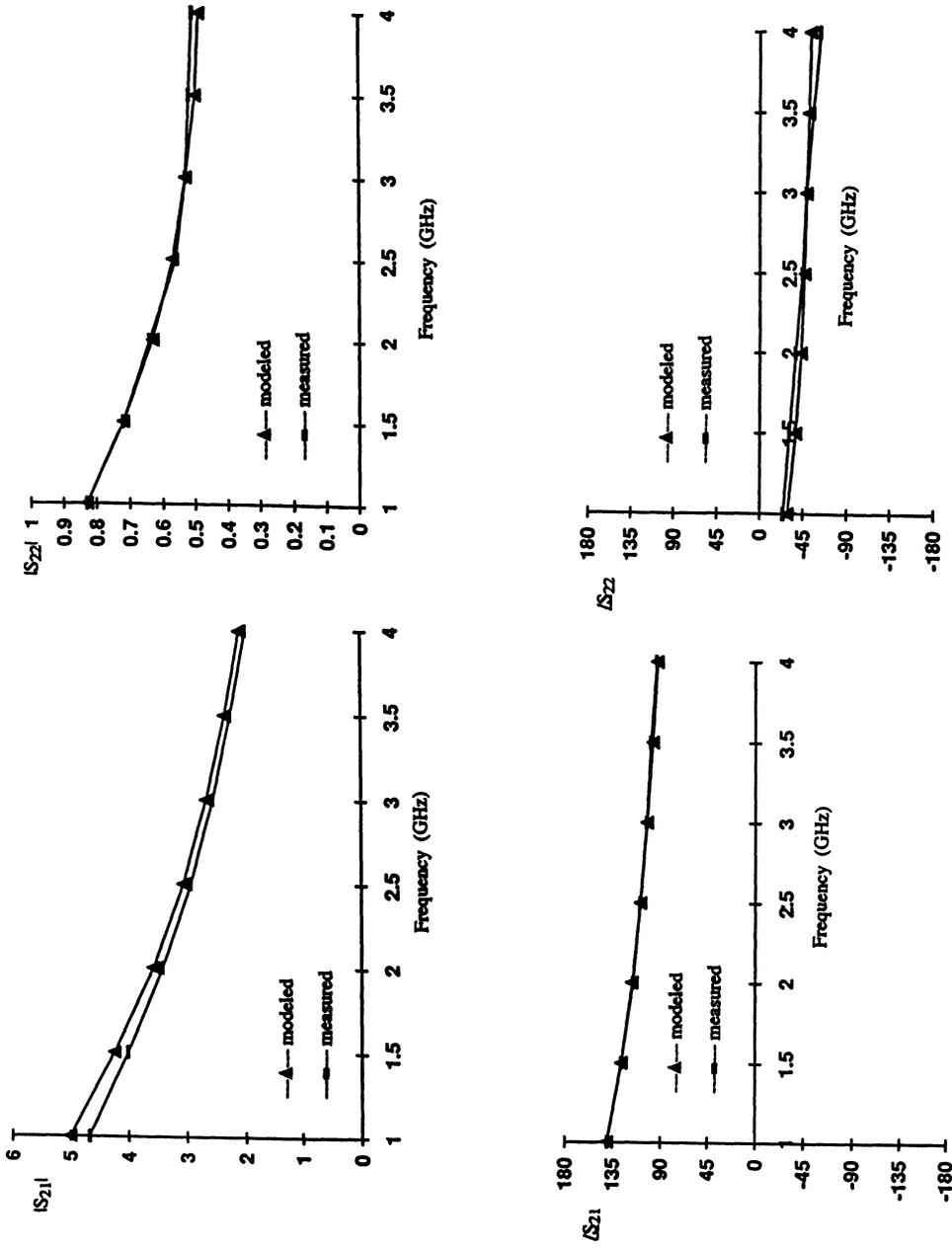


FIGURE 4 Comparison between measured and modeled values for the  $S_{21}$  and  $S_{22}$  parameters

A sensitivity analysis has been carried out on the above model to bring out the influence of each circuit element on all the scattering parameters. The incidence matrix so determined is not sparse, thus demonstrating that for bipolar transistors, it is impractical to use a decomposition approach, as it has been successfully employed in modeling low-noise GaAs and pseudomorphic HEMTs [5].

The model effectiveness has then been tested by determining the element value variations in the different bias conditions. All the model elements exhibit value trends in very good accordance with the physics-related predictions.

As far as the microwave noise performance is concerned, we refer to the representation in terms of the four noise parameters that appear in the well-known relationship

$$F(\Gamma_s) = F_0 + 4 r_n \frac{|\Gamma_s - \Gamma_0|^2}{|1 + \Gamma_0|^2(1 - |\Gamma_s|^2)}$$

where  $F_0$  (minimum noise figure),  $|\Gamma_0|$  and  $1/\Gamma_0$  (optimum value of  $\Gamma_s$ ), and  $r_n$  are the four parameters,  $F$  and  $\Gamma_s$  are the noise figure and the relevant input termination reflection coefficient of the DUT, respectively.

In order to extract a noisy model, two fundamental noise sources have to be accounted for in modeling bipolar transistors, i.e., thermal noise sources and shot noise sources. The thermal noise is generated by the resistive elements representing losses in the base, emitter, and collector regions respectively, and it is calculated by associating the ambient temperature value to them. In the common emitter (CE) configuration, the shot noise is generated by the statistical fluctuations of the base and collector current values that are, to some extent, correlated to each other. The adopted noise model for the chip device is, therefore, that reported in Fig. 5.

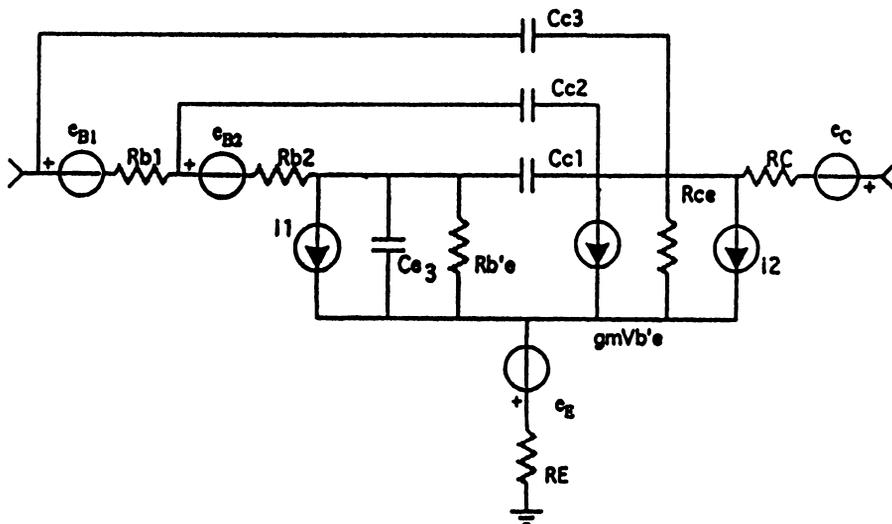


FIGURE 5 Noise model adopted for the chip device. The noise current sources  $i_1$  and  $i_2$  are mutually correlated

On the basis of this noisy equivalent circuit, the noise parameters are then calculated.

The physics-based relationships that allows for evaluating the amount of noise power generated by the above generators, including correlation, are as follows

$$\langle |i_1|^2 \rangle = 4KT_B \operatorname{Re}(Y_{11e}) - 2qI_B B$$

$$\langle |i_2|^2 \rangle = 2qI_C B$$

$$\langle |i_2 i_2^*| \rangle = 2qI_C B + 2KT_B Y_{21e}$$

where  $I_B$ ,  $I_C$  are the dc values of the base and collector current,  $Y_{ije}$  are the network admittance parameters in the CE configuration, and  $B$  is the frequency bandwidth that is assumed to be 1 Hz for *spot* noise measurements.

From the above equations, derived for conventional BJT's, we calculated the initial values of the noise sources and their correlation coefficient (at the above cited bias condition) that have subsequently undergone the optimization procedure in order to minimize the global error function. Such initial values are reported in Tab. 1, a). It has to be noted that the element values of the small-signal model have not been involved in the noise optimization procedure, which is quite different from the modeling technique adopted for HEMTs [5]. The optimum weights associated to the noise parameter error functions have found to be:

$$W_{F0} = 42, W_{|\Gamma_{0j}|} = 60, W_{|\Gamma_0} = 0.7, W_{Rn} = 1$$

The optimization results exhibit an excellent matching between the theoretically predicted and the simulated noise current source values, whereas the correlation coefficient changes remarkably from its initial value turning to be mostly imaginary. A subsequent noise sensitivity analysis has allowed a further refinement of the previously optimized values, thus obtaining the final results reported in Tab. 1, b).

TABLE I

(a) Initial values of the noise current sources and the real and imaginary part of the correlation coefficient @  $V_{CE} = 5$  V,  $I_C = 2$  mA; optimized values of the correlated noise generators @  $V_{CE} = 5$  V,  $I_C = 2$  mA (b) and @  $V_{CE} = 5$  V,  $I_C = 1$  mA (c)

$i_1 = 32 \sqrt{\text{pA}^2/\text{Hz}}$	$CR = 0.43$	
$i_2 = 640 \sqrt{\text{pA}^2/\text{Hz}}$	$CI = 0.08$	(a)
$i_1 = 27 \sqrt{\text{pA}^2/\text{Hz}}$	$CR = 0$	
$i_2 = 607 \sqrt{\text{pA}^2/\text{Hz}}$	$CI = 0.64$	(b)
$i_1 = 18 \sqrt{\text{pA}^2/\text{Hz}}$	$CR = 0$	
$i_2 = 290 \sqrt{\text{pA}^2/\text{Hz}}$	$CI = 0.53$	(c)

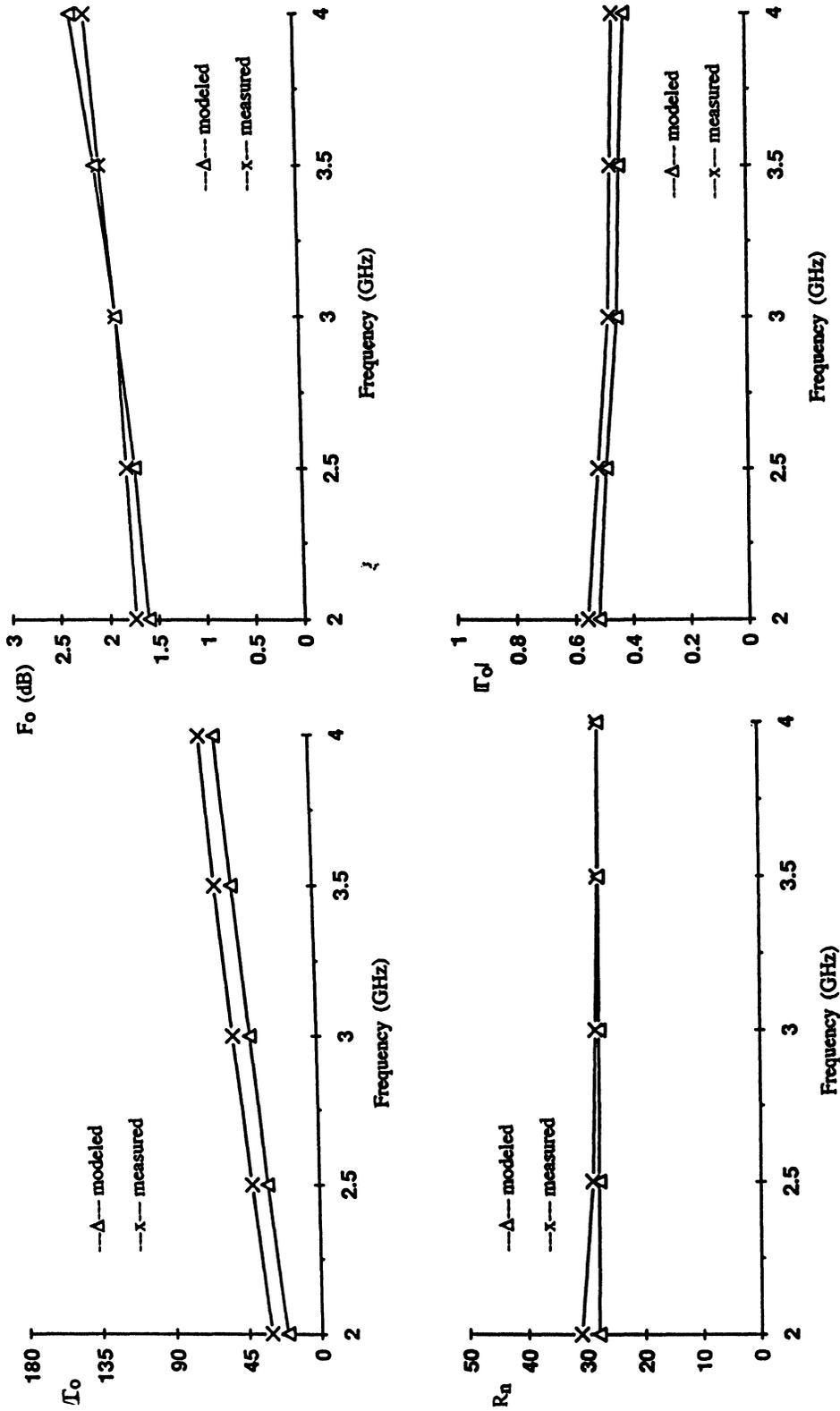


FIGURE 6 Comparison between measured and modeled values for the noise parameters

An interesting result of this sensitivity analysis is that the real part of the correlation coefficient has a negligible influence on all four noise parameters, which confirms the final value assessed by the optimization procedure for the above coefficient. The comparison between measured and modeled noise parameters is shown in Fig. 6. Such results show outstanding values of the minimum noise figure over the entire frequency range, thus suggesting the adoption of PSA transistors in low-noise amplifiers of receiver front-ends.

By testing the effectiveness of the noise model at the bias conditions  $V_{ce} = 5\text{ V}$ ,  $I_c = 1\text{ mA}$ , we have obtained the values of the noise current sources and their correlation coefficient as reported in Tab. 1, c). As can be seen, the noise generators still match the physics-based predictions with a value reduction close to 50%, whereas the correlation coefficient reduces its absolute value still maintaining a phase of  $90^\circ$ .

We might, therefore, hypothesize that the behavior of this latter noise coefficient be the only one markedly influenced by the structural difference between a PSA and a conventional Si transistor. As discussed above, a more extensive analysis on a wide variety of this device type is in progress, whose results will be employed to assess these preliminary results and to support modifications of the analytical noise relationships.

## CONCLUSIONS

A complete characterization and modeling study has been presented on a double polysilicon self-aligned bipolar transistor over the 1–4 GHz frequency range and at different bias conditions. The characterization involved determination of both the scattering and the noise parameter sets by means of a noise figure measuring set-up only.

To the aim of referring the measured performance directly at the chip reference planes, we applied an accurate de-embedding procedure to the experimental data of the packaged device.

An equivalent circuit model has then been extracted that includes noise sources. Such model exhibits distinguished performances that are going to be further assessed through in-progress extensive investigation on several PSA devices.

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