MEASUREMENTS AND ANALYTICAL COMPUTER-BASED STUDY OF CMOS INVERTERS AND SCHMITT TRIGGERS

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Modified CMOS inverters with three and four transistors have been made. Two varieties of CMOS Schmitt Triggers have been considered. CMOS Schmitt Trigger with wide hysteresis has been obtained. Complete detailed theoretical, experimental and computer based results are derived and exhibited.

INTRODUCTION

CMOS circuits have revolutionized the digital applications. In this paper, the behavior of CMOS transistors used in inverters and Schmitt Triggers have been analysed. Inverters with voltage-controlled threshold at a constant supply voltage have been obtained. Modified inverters with three and four transistors have been discussed.

A very simple circuit for a CMOS Schmitt Trigger, consisting of four MOS transistors has been proposed [1]. Three transistors are of enhancement type and one is of depletion type. Another type of Schmitt Trigger [2] has been said to have used a total of eight MOS transistors.

In this paper, the Schmitt Trigger circuit using four transistors is analyzed in view of voltage controlled and resistance controlled thresholds and the characteristics for various voltage relationships are obtained. The hysteresis effect on the static transfer characteristics are indicated graphically. Theoretical test results for each circuit are obtained through digital computer simulation and the results are verified with the experimental ones.

ANALYSIS OF MODIFIED CMOS INVERTERS

Inverters with Three Transistors

Such inverters are obtained when one PMOS (Fig. 1a) or NMOS (Fig. 1b) transistor is connected to the source of a PMOS or NMOS transistor of the base inverter. In the transition region, their characteristics are approximately linear and can be replaced by R_p & R_n resistors, respectively, with resistance being a function of V_x . Due to negative feedback at these resistors, the transfer characteristic shape is

FIGURE 1

changed as well as the inverter threshold voltage. When β -constants of all transistors are equal the inverter threshold voltage is given by:

$$V_T = V_{TN} + 2(V_{DD} + V_{TP} - V_x) \left[\left(\frac{1 + 0.5 V_{DD} - V_{TN}}{V_{DD} + V_{TP} - V_x} \right)^{1/2} - 1 \right] \quad (1)$$

or

$$= V_{DD} + V_{TP} - 2(V_x - V_{TN}) \left[\left(1 + 0.5 \frac{V_{DD} + V_{TP} - V_{TN}}{V_x - V_{TN}} \right)^{1/2} - 1 \right] \quad (2)$$

(Equation (1) is valid for Fig. 1a, Equation (2) is valid for Fig. 1b). Figure 2 shows the experimental (solid line) and theoretical (dashed line) dependence of threshold voltage as a function of controlling voltage V_x . Certain differences between theoretical and experimental results are due to approximate values of V_{TN} , V_{TP} , β_N , and β_P . Besides threshold change, the controlling voltage V_x has also influence on the transfer characteristics shape. The transfer characteristics are shown in (Fig. 3).

With reference to the standard inverter the slope of the transfer characteristics in the transient range is increased as in the linearity range, being of special importance in analog applications of inverters.

Inverters with Four Transistors

In this case, one more pair of CMOS transistors has been added to the basis inverter (Fig. 4).

FIGURE 2

For the same control voltage change, the inverter threshold change in this case is approximately twice as high as compared to the previous case. The threshold voltage is approximately a linear function of ' V_x '. When the β -constants of all transistors are equal, it can be considered that $V_T = (V_{DD} - V_x)$. Maximum deviation from a linear change is less than 15%.

CMOS Schmitt Triggers

The Schmitt Trigger circuit consisting of one PMOS and three NMOS transistors is shown in (Fig. 5). The transfer characteristic has the shape of the hysteresis curve because of the effect of transistors ' T_{n1} ' and ' T_{n2} '. Regenerative feedback is obtained using transistor ' T_{n2} ' which, during the change of state, works like a follower.

Assuming that the input voltage is varied from a zero value to the supply voltage level (V_{DD}), the transfer characteristics, with reference to the states of individual transistors, can be divided into seven different regions shown in (Fig. 6a,b).

The details of the transistor states and the voltage conditions conditions for these seven regions are described in Table-1: Through equalization of the drain currents T_{n1} and T_{n2} in saturation, we obtain

$$V_{DSn1} = V_{DD} - V_{Tn2} - \sqrt{K_n} (V_{in} - V_{Tn1}) \quad (3)$$

Where $K_n = (W_{n1}/L_{n1})/(W_{n2}/L_{n2})$, the geometry ratio.

$$V_{in} = (V_{DD} + \sqrt{K_n} V_{Tn1})/1 + \sqrt{K_n} \quad (4)$$

Transistor characteristics of standard inverter

The inverter Fig 1(a) supply voltage \$V_{DD}\$ 10V

FIGURE 3

In view of equation (4), the threshold voltage is obtained from the fact that $V_T^+ = V_{in}$ in the region V of the operating conditions. Thus,

$$V_T^+ = \left[\frac{V_{DD} + V_{TP} + \sqrt{\frac{\beta_n}{2\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{2\beta_p}}} \right] + \left[\frac{\sqrt{\frac{\beta_n}{2\beta_p}} (V_{DD} - V_{Tn})}{(1 + \sqrt{K_n}) \left(1 + \frac{\beta_n}{2\beta_p}\right)} \right] \quad (5)$$

FIGURE 4 Modified inverter with four transistors.

FIGURE 5 Circuit with one PMOS and three NMOS transistors.

FIGURE 6 (a)

FIGURE 6 (b)

TABLE 1

Region	Voltage condition	States of individual Transistors			
		ON	OFF	Saturated	Unsaturated
I	$0 \leq V_{in} \leq V_{Tn1}$	T_p, T_{n2}	T_n, T_{n1}	T_{n2}	T_p
II	$V_{Tn1} \leq V_{in} \leq V_{DSN1} + V_{Tn1}$	$T_p, T_{1'}, T_{n2'}$	T_2	$T_{n1'}, T_{n2}$	T_p
III	$V_{DSN1} + V_{Tn1} \leq V_{in} \leq V_{DSn1} + V_{Tn}'$	All	—	$T_n', T_{n2'}, T_p$	T_{n1}
IV	$V_{Tn}' = V_{Tn2}'$	All	—	T_n', T_{n2}	T_p, T_{n1}
V	$V_{Tn}' = V_{Tn2}'$	All	—	T_n', T_p	T_{n1}, T_{n2}
VI	$V_T^+ < V_{in} < V_{DD} + V_{Tp}$	$T_e, T_{n'}$	T_{n1}	T_p	T_n, T_{n1}
VII	$V_{DD} + V_{Tp} \leq V_{in} \leq V_{DD}$	T_n, T_{n1}'	T_p, T_{n2}	—	T_n, T_{n1}

Where, V_{DSn1} = output voltage across Schmitt Trigger.

V_{Tn1} = Threshold voltage of T_{n1} .

V_{Tn}', V_{Tp} = Threshold voltage of T_n, T_p respectively.

V_{Tn2}' = Threshold voltage of T_{n2} .

V_T^+ = high threshold voltage of Schmitt Trigger.

In Region-VII, T_{n2} is off until both T_n and T_p are saturated. When the transistor T_{n2} starts conducting, regenerative feedback takes place and a much steeper characteristic is obtained. This is characterized by the two terms available in equation (5), within the parenthesis. The first term represents the low threshold voltage (V^-) and the second term represents a hysteresis voltage component of V^+ . The regenerative process is clearly indicated between points A–B and C–D of Fig. 6(b).

Analysis of the Schmitt Trigger circuit with three PMOS and one NMOS transistors can be carried out in a similar way as the previous one with reference to the circuit of Fig. 7.

Schmitt Trigger Circuit With Three Pairs of CMOS Transistors

A wider hysteresis window for the same supply voltage and the same geometry of transistors can be obtained if the circuits of Fig. 5 and Fig. 7 are combined in one circuit as shown in Fig. 8.

Regenerative feedback, either at a positive or negative output, is realized through T_{n3} and T_{p3} . Hence the transfer characteristic is almost ideal. In this case, the threshold voltage is obtained as

$$V_T^+ = \left[\frac{V_{DD} + V_{Tp} + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\beta_n/\beta_p}} \right] + \left[\frac{\sqrt{\beta_n/\beta_p} (V_{DD} - V_{Tn})}{(1 + \sqrt{K_n}) (1 + \sqrt{\beta_n/\beta_p})} \right] \quad (6)$$

The low threshold and hysteresis components of this voltage are (V^-), (V_h), respectively, and are given as,

$$V^- = \left[\frac{V_{DD} + V_{Tp} + \sqrt{\beta_n/\beta_p} V_{Tn}}{1 + \sqrt{\beta_n/\beta_p}} \right] - \left[\frac{V_{DD} + V_{Tp}}{(1 + \sqrt{K_p}) (1 + \sqrt{\beta_n/\beta_p})} \right] \quad (7)$$

FIGURE 7 Schmitt Trigger with one NMOS and three PMOS transistors.

$$V_n = \left[\frac{1}{1 + \sqrt{\beta_n/\beta_p}} \left(\frac{\sqrt{\beta_n/\beta_p} (V_{DD} - V_{Tn})}{1 + \sqrt{K_n}} \right) \right] + \left[\frac{V_{DD} + V_{Tp}}{1 + \sqrt{K_p}} \right] \quad (8)$$

The dependance of the high and low thresholds as a function of supply voltage and ratios of T_{n1} and T_{n2} (K_n) and T_{p1} , T_{p2} (K_p), for the condition that $\beta_{n1} = \beta_n = \beta_{p1} = \beta_p$ is shown in Fig. 9. The hysteresis voltage increases when K_n and K_p decrease.

Schmitt Trigger with Resistance Controlled Thresholds

A CMOS inverter will have a static transfer characteristic with hysteresis if the source voltage of one or both the transistors is made dependent on the state at the output, as shown in Fig. 10. Let us assume that the input voltage increases from zero to V_{DD} . While T_n is off, $V_{out} = V_{DD}$ and when $V_{in} = V_{IN} + R_1 I_{DN1}$, T_N turns on. Considering that threshold voltages for both (T_n & T_{N1}) are equal, the following relation holds good.

$$V_{in} = V_{DD} - \frac{1}{2\beta_{n1}} R_1 \{ \sqrt{1 + 4\beta_{N1} (V_{DD} - V_{TN1}) R_1} - 1 \} \quad (9)$$

FIGURE 8

FIGURE 9 Schmitt Trigger with three phase of CMOS transistors.

FIGURE 10 (a)

(a) $R_1 = 560\Omega$; $R_2 = 150\Omega$

(b) $R_1 = 2.7K$; $R_2 = 8.6K$

FIGURE 10 (b) Schmitt Trigger 2/3 and two resistors.

The input voltage corresponding to when the output is changed from the high level to a low one is called the high threshold (V_T^+) of the Schmitt Trigger. For $V_{in} > V_T^+$ the output is low ($V_{out} \cong 0$). In this condition, T_{n1} is off and T_{p1} is ON. If

$$\text{the input voltage is reduced, then equation (9) will reduce to } V_{in} = \frac{1}{2 \beta_{p1} R_2} \{\sqrt{1 + 4 \beta_{p1} (V_{DD} + V_{Tp}) R_2} - 1\} \quad (10)$$

If the input voltage is further reduced, T_N passes from the non-saturated to the saturated zone. Then, the input voltage becomes equal to the low threshold (V_T^-) of the Schmitt Trigger. The voltage hysteresis, $V_n = V_T^+ - V_T^-$, depends on the supply voltage and R_1 & R_2 . When $R_1 = R_2 = 0$ the Schmitt Trigger of Figs. 11(a) and 11(b) are obtained.

In this case, the source voltage of one transistor is fixed (V_{DD} or zero). When $V_{out} = 0$, T_{n1} is OFF and has no influence on the low threshold (V_T^-) as shown in Fig. 11(a) and similarly the transistor T_p of Fig. 11(b) has no influence on the high threshold (V_T^+).

Schmitt Trigger with Voltage Controlled Thresholds

As indicated in Fig. 12, the two CMOS inverters (I_1, I_2) determine the voltage thresholds and the RS Latch provides a regenerative element of the Schmitt Trigger. Fig. 13 indicates the various stages of input voltage variation on V_{out} . The high and low threshold voltages are given by,

$$V_T^+ = V_{DD} + V_{Tp} - 2(V_{x1} - V_{TN}) \left\{ \sqrt{1 + 0.5 \left(\frac{V_{DD} + V_{Tp} - V_{TN}}{V_{x1} - V_{TN}} \right)} - 1 \right\} \quad (11)$$

$$V_T^- = V_{TN} + 2(V_{DD} + V_{Tp} - V_{x2}) \left\{ \sqrt{1 + 0.5 \frac{V_{DD} + V_{Tp} - V_{TN}}{V_{DD} + V_{Tp} - V_{x2}}} - 1 \right\} \quad (12)$$

The hysteresis will be maximum when the transistors T_p and T_N are in a weakly conducting state, approximately

$$V_H(\text{Max}) = V_{DD} - V_{TN} - |V_{Tp}|.$$

When

$$V_{x1} = V_{DD} \text{ and } V_{x2} = 0,$$

the hysteresis is minimum. The maximum hysteresis is given by

$$V_H(\text{Max}) = V_{DD} - 2V_{TN} - 4(V_{DD} - V_{TN}) \left\{ \sqrt{1 + 0.5 \frac{V_{DD} - 2V_{TN}}{V_{DD} - V_{TN}}} - 1 \right\} \quad (13)$$

FIGURE 11 Schmitt Triggers and one resistor.

COMPUTER IMPLEMENTATION AND VERIFICATION

The theoretical results for all the circuits have been obtained with the help of a computer program. The results so obtained are then compared with the experimental ones. The necessary assumptions made in the process of computer implementation are as follows:

- The geometry ratio of transistors is assumed to be 0.2.
- The β constants are assumed the same ($\beta_n = \beta_p$).
- V_{TN} and V_{Tp} are assumed to be 1.5V.

ALGORITHM

- 1) Initialize input voltage and check the states of all transistors.
- 2) If T_n is OFF then $V_{out} = 0$.

FIGURE 12 Logic diagram of the Schmitt Trigger with voltage controlled threshold.

FIGURE 13

- 3) If T_n is saturated and T_p is ON, then calculate output voltage by equalizing drain current equations of the corresponding states.
- 4) If T_p is saturated, ' V_{out} ' suddenly falls to ' V_T ' value.
- 5) Calculate V_T^+ , V_T^- .
- 6) Increase ' V_{in} ' in steps of small increments (0.2V) and check the states of all transistors.
- 7) Repeat with this process by going to Step 2 until $V_{in} = 10V$.
- 8) Decrease ' V_{in} ' in steps of small decrement (0.2V) and repeat the whole process until $V_{in} = 0$.
- 9) STOP.

CONCLUSION

The functional possibilities of CMOS circuits for digital and digital-analog applications have been expanded by modified inverters. A large range of threshold voltage change and very low loading of the control signal source makes it possible for such a mode of threshold voltage regulation to have an advantage over the conventional voltage control through power supply variations.

A Schmitt Trigger consisting of only four MOS transistors has been obtained. One of the advantages of this circuit is the possibility of all transistors being made by conventional CMOS technology. The required hysteresis is realized through adequate geometries of transistors in the feedback loop.

The Schmitt circuits and inverters described in this paper [3–4] can be used as basic circuits for making more complex logic circuits with hysteresis characteristics. The threshold voltages of the circuit are a function of the controlling voltages and can be changed independently of each other [5]. The voltage hysteresis of the circuit can be regulated from a few tens of milli volts to approximately $V_H = V_{DD} - 3V$.

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