MODELING OF INTERFACE DEFECT DISTRIBUTION FOR AN n -MOSFETs UNDER HOT-CARRIER STRESSING

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We propose to model the evolution of the interface defect density, induced by the hot-carrier-injection, during stress time for n -MOSFET transistor. This interface defect density is modeled by a spatial and temporal gaussian distribution centered close to the extremity of the channel near the drain. The gaussian Parameters (standard deviation and maximum) vary according to the stress. The stress generated defects leads to the degradation of the threshold voltage. The analysis of the threshold voltage evolution with stress time allows us to handle informations on the device performances degradation. The mathematic expression is simple so that the present model is suitable for circuit simulator.

Keywords: n -MOSFET; Defects; Stress; Hot-carrier; Aging

1. INTRODUCTION

Hot carrier injection into the oxide and at the Si–SiO₂ interface has been recognized as a major limitation to the long term reliability of short channel n -MOSFET devices. Indeed, the transistor miniaturization entails the presence of higher electric fields. These high electric fields increase the injection of the hot carriers in the oxide and at the interface. Therefore, localized defects near the drain are created [1–3]. These defects generate a parasitic currents [4–8] and contribute to

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the device aging and degradation. Understanding the physical phenomenon of the degradation process is required in order to find technological solutions to minimize the aging effect and device performances degradation. It is reported that for the maximum substrate current condition ($V_G = V_D/2$) the interface defects density is greater than the oxide one [9–13]. Many efforts have been devoted to determine the variation of the interface and oxide defects densities during stress time [3, 14]. On the other hand, one of the most important parameters which describe the MOSFETs degradation amount is the threshold voltage. The analysis of its evolution during stress offers some interesting information on performances degradation and device reliability. The threshold voltage is obtained by solving the two-dimensional Poisson's equation and taking into account the spatial and temporal charge and the channel electric field variations during stress. The model of the interface defect density presented in this paper is well suited for device reliability investigation and circuit simulators.

2. INTERFACE DEFECT DENSITY MODELING

The MOSFET degradation is induced by the hot carrier injection in the oxide and at the Si–SiO₂ interface. In general the large electric field is strongly localized near the drain, therefore, defects are similarly concentrated. Moreover, for $V_G = V_D/2$ (maximum substrate current condition) the interface defects density is greater than the oxide one [9–10]. Consequently, we are only interested to the interface defects induced during stress. According to experimental results [1, 15], we choose a spatial and temporal gaussian distribution, centered near drain (Fig. 1), to represent the defect density, with parameters depending (standard deviation and maximum) on time and stress conditions. Therefore, the defect density is modeled by:

$$N_{it}(x, t) = N_{it_{\max}}(t) \exp\left(\frac{-(x - x_c)^2}{2\sigma(t)^2}\right) \quad (1)$$

where t is the stress time and x_c is the gaussian center. The maximum defect density $N_{it_{\max}}(t)$ and the standard deviation $\sigma(t)$, depend on transistor technology and stress conditions.

FIGURE 1 Illustration of gaussian spatial distribution of defects localized at the interface.

On the basis of the interface charge variation during the stress [12, 16], $N_{it_{max}}(t)$ is given by:

$$N_{it_{max}}(t) = \frac{a}{S_e V_{th}} t^n \left(\frac{I_D}{W} \right)^n \quad (2)$$

where W is the channel width, I_D is the drain current and a is a correction factor. $S_e = 10^{-15} \text{ cm}^2$ is the average capture cross section, $V_{th} = 10^7 \text{ cm/s}$ is the thermal velocity, the exponent n has been found

to range between 0.5 and 0.75 [12, 16]. In our simulation it is taken equal to 0.5. Otherwise, $\sigma(t)$ is related to the degraded zone variation with time. To take account for the saturation of the degraded zone extension [4, 17], the standard deviation of the gaussian distribution is expressed as:

$$\sigma(t) = \sigma_0 + b \log(t) \quad (3)$$

b is a factor which depends on stress conditions [17].

σ_0 is regarded as an effective ionization length [18].

$$\sigma_0 = 0.22 t_{\text{ox}}^{1/3} x_j^{1/2}$$

where t_{ox} is the oxide thickness and x_j is the depth junction. a and b are the fitting parameters which can be extracted, according to the flowchart (Fig. 2), by comparing experimental and simulation results.

FIGURE 2 A flowchart showing the extraction of interface defects density evolution.

3. THRESHOLD VOLTAGE IMPACT

The spatial and temporal space charge variation must be taken into account in the threshold voltage derivation. The injected charges at the Si–SiO₂ interface during stress are simulated by the gaussian distribution (1). The surface potential variation along the channel is described by the following differential equation [19]:

$$\frac{\partial^2 \psi_s(x, t)}{\partial x^2} - k^2 \psi_s(x, t) = -\frac{12C_{ox}}{6\epsilon_s W_d + C_{ox} W_d^2} \left[V_{GS} - V_{FB} - \frac{Q_{dep}}{C_{ox}} - \frac{q}{C_{ox}} N_{it}(x, t) \right] \quad (4)$$

V_{GS} , V_{FB} , C_{ox} , ϵ_s , W_d and Q_{dep} are the gate bias, the flat-band voltage, the oxide capacitance per unit area, the dielectric permittivity, the depletion depth and the depletion charge, respectively.

The resolution of Eq. (4) which gives the surface potential profil $\psi(x, t)$ is determined in a previous work [19]. The threshold voltage is defined as the gate bias when the minimum surface potential is equal to $2\phi_f$ (fermi potential). The threshold voltage is then derived from resolution of equation system: $\psi_s(x) = 2\phi_f$ and $d\psi_s(x)/dx = 0$.

4. SIMULATION AND EXPERIMENTAL RESULTS

In order to check the modeling accuracy, the simulation results of the threshold voltage, which takes into account the spatial-temporal defect distribution variation with stress time, and the experimental data are compared. The transistor parameters are: $L = 0.6 \mu m$, $t_{ox} = 14 \text{ nm}$, $x_j = 0.15 \mu m$, the channel doping is $N_b = 6.510^{16} \text{ cm}^{-3}$, the source/drain doping is $N_{s,d} = 10^{19} \text{ cm}^{-3}$, the temperature is $T = 300 \text{ K}$ and the electrical conditions are $V_{GS} = 2.3 \text{ V}$ and $V_{DS} = 6.5 \text{ V}$.

The flowchart represented in Figure 2 illustrates the procedure used to extract the fitting parameter a and b . The evolution of the interface defect density according to the stress time is sketched in Figure 3. This figure shows the extension of the degraded zone along the channel and the amount of the interface defects density. Figure 4 shows the

FIGURE 3 Variation of the interface defects density along the channel *versus* stress time.

FIGURE 4 Evolution of threshold voltage shift *versus* stress time, the marks are the experimental data while the line is the modeling result.

variation of the threshold voltage variation during stress where the solid line and marks represent respectively the simulation results and the experimental data.

5. CONCLUSION

This model allows us to determine the evolution of the interface defects density during stress, induced by the hot carrier injection under the maximum substrate condition. The present model of the interface defect density is suitable for circuit simulator because of its mathematical simplicity and computing efficiency. The threshold voltage variation during stress time provide an interesting informations on performances degradation and device reliability.

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