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CHARACTERIZATION OF DEFECT TRAPS IN SiO_2 THIN FILMS

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In order to understand the degradation of the electrical operations of metal-oxide-semiconductor (MOS) devices, this work is concerned by the defects generation processes in the non-stoichiometric SiO_x area and at the SiO_2 interface. For this purpose, a new measurement technique to study slow-state traps and their relationship with fast-state traps is developed. This method considers capacitance-voltage measurements and temperature effects during the hysteresis cycle.

Keywords: Gate oxide; MOS capacitor; C-V characteristics; Hysteresis; Slow-state traps; Defects

1. INTRODUCTION

Under normal operating condition, interface states and oxide defects are generated in the oxide SiO_2 film and at the oxide-silicon interface of a metal-oxide-silicon (MOS) structure of microelectronic devices. High electric fields, which appear in very thin isolative oxide layers, are

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known [1–3] to be the cause of this generation which induces degradations of the devices properties.

In this work we are interested in the study of slow traps, which are responsible for long time electrical instabilities of MOS devices [4]. This paper introduces a new measurement technique to characterize these defects. The method is based on capacitance-voltage C(V) [5–8] measurements at low temperature and it uses thermal energy to generate an inversion regime during the hysteresis cycle. It is applied on p-type poly-Si gate-MOS capacitors with thin (17.8 nm thickness) oxide layer to separate the effects of the different types of charges and traps.

2. THEORETICAL APPROACH

The C(V) characteristic is measured along a cycle which is described by varying the applied bias across the MOS capacitor from –5V to +5 V and back to –5 V. An hysteresis effect is observed. The method is based on the observation of the modification of the hysteresis cycle induced by a degradation process, which consist in a Fowler-Nordheim electron injection from the gate, made under a constant voltage.

The C(V) characteristics measurements were carried out at temperatures below 100 K. In the case of p-type MOS devices firstly, the C(V) characteristics were measured from a negative bias to a positive bias. In this measurement, a deep depletion situation is observed at positive biases due to the low-temperature measurement. At the maximum positive bias, the sample temperature was raised to 300 K and kept for one hour, (heating and cooling cycle). Due to this high-temperature process, electrons are thermally excited and are accumulated in the inversion layer. Moreover, the excited electrons are captured in the traps in the oxide and at the interface. All slow-state traps are also occupied in electrons and the charging process obeys Jonsher's law [9]. Once the traps have been occupied by electrons, the sample was cooled down below 100 K again, and then the C-V measurement was performed from the positive bias to the negative bias. During this process, the electrons trapped by slow states in the oxide were not observed to be emitted from the states. Therefore, a complete hysteresis can be obtained. We can separate slow-state traps from fast-state traps because the electrons are quickly released from the fast states.

A complete description of one hysteresis cycle needs a global approach with the parameters: temperature, voltage and time. From the differences between the C(V) hysteresis obtained after degradation and the initial hysteresis after the heating process described above was applied to the sample, three voltage shifts ΔV_{ii} may be determined from curves displacements ('*ii*' will be '*ss*' for slow states, '*fs*' for fast states, '*of*' for oxide fixed charges or '*mg*' for migration species), together with the evolution in time of the voltage shift ΔV_{ss}. Differences are observed between charging and discharging processes in the relaxation of traps.

From these voltage shifts, we can obtain the values N_{ii} of each trap density:

$$N_{ii} = \frac{\Delta V_{ii} \varepsilon_{ox}}{q e_{ox}} \quad (1)$$

Here e_{ox} is the oxide thickness and ε_{ox} is the dielectric permittivity of the oxide. In the case of slow-state traps, Jonsher's law [9,10] is written as:

$$\Delta V_{ss}(t) = \frac{q N_D}{C_{ox}} \left[1 + \left(\frac{t}{t_c} \right)^{-\alpha} \right] \quad (2)$$

N_d is the equilibrium density of defect sites. In this equation, a slow-state trap is taken as an oxide trap. The model considers the slow-state trap as a vacancy. This model can be applied successfully to the E' center case [11–14]. ΔV_{ss} is then the gate voltage shift in the C-V characteristics due to the slow-state traps, C_{ox} the maximum capacitance, q charge of the electron, t the time, t_c the time needed to discharge half of the slow-state traps and α is a coefficient depending on t_c. Experimental results for t_c and α will be given. Our assertion, here, is to give the saturation term $\Delta V_{ss}(\infty) = q N_d / C_{ox}$. The general evolution Eq. (2) is also developed in [9]. ΔV_{ss} represents a part of ΔV_{mg} relative to the variation of the effective slow state traps, where ΔV_{mg} is the voltage shift due to defects in the mid-gap and is indeed a true measure of the effective net oxide.

3. EXPERIMENTS AND DISCUSSION

Experiments were performed with sample #1: a MOS capacitors fabricated on a p-type Si (100) substrate with a boron concentration of

2×10^{17} cm^{-3} using LOCOS isolation (Local Oxidation of Silicon). The oxide film was grown in a wet environment at 850°C and its thickness was 17.8 nm. The sample was subjected to boron implantation through the gate oxide under 40 keV to adjust the transistor threshold voltage. The polycristalline silicon gate area was 3.82×10^{-4} cm^2.

For this new High/Low Temperature C(V) (HLTCV displacement method), thermal energy is used to generate inversion regime and also to study slow-state traps more thoroughly. As far as formation of the inversion layer is concerned, both light illumination /13/ and thermal heating have physically comparable effects. The heating treatment results in generation of extra oxide charges which effects can be separated. These effects are investigated in this present paper.

Figure 1 shows C(V) characteristics measured at a temperature of 100 K for sample #1 after a voltage stress under an applied field of 10 MV/cm, where the density of injected electrons was $N_{inj} = 5 \times 10^{17}$ cm^{-2}. A good hysteresis is obtained for the separation of traps. The C-V curve from negative bias to positive bias has a feature of

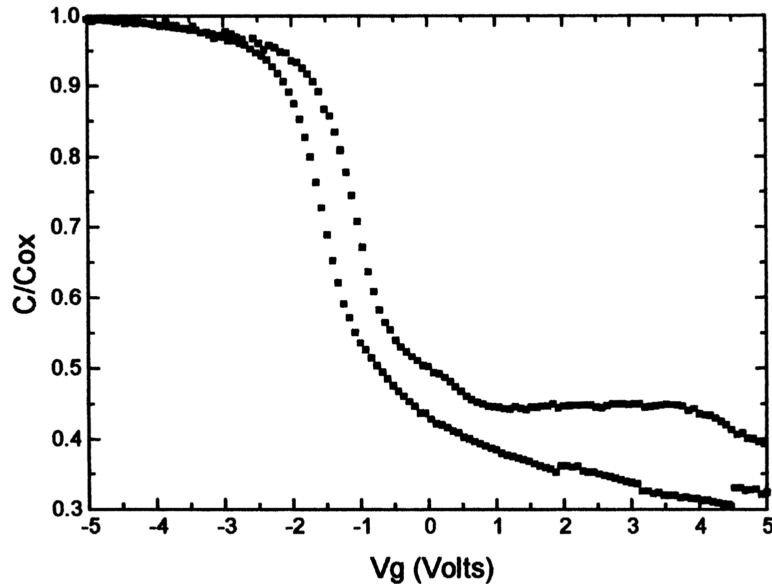

FIGURE 1 Hysteresis after a constant voltage stress that injected $N_{inj} = 5 \times 10^{17}$ cm^{-2} at inversion conditions: 308 K, one hour.

deep depletion condition due to the low measurement temperature. At 15 V, the sample was warmed up to 308 K for 15 min and thus the capacitance increases by the formation of the inversion layer.

Figure 2 displays the capacitance change at +5 V during warming up to 308 K, as a function of warming-up time. This result which would seem to show that the capacitance saturates above 500 s, which means that a 10 min warming-up is sufficient to form the inversion layer.

In Figure 1, at around 0 V, the reverse C(V) curve has a plateau originating from the fast-state traps. Under the depletion region, the reverse curve runs parallel with the forward curve, which clearly indicates the existence of the slow-state traps. In this manner various traps effects are observed as induced voltage shifts. The shift between the forward and the reverse curve at the plateau region is $\Delta V_{ss} + \Delta V_{fs}$, and at the depletion region ΔV_{ss} is determined. Accordingly, we can distinguish the slow-state traps from the fast-state traps and obtain here, $N_{ss} = 5.4 \times 10^{11}\,\text{cm}^{-2}$, $N_{fs} = 6 \times 10^{11}\,\text{cm}^{-2}$.

The voltage shift between the non-stressed and the reverse characteristics, ΔV_{of}, corresponds to the density of oxide fixed charge N_{of}. We found $N_{of} = 1.2 \times 10^{11}\,\text{cm}^{-2}$. Figure 3 shows these contribu-

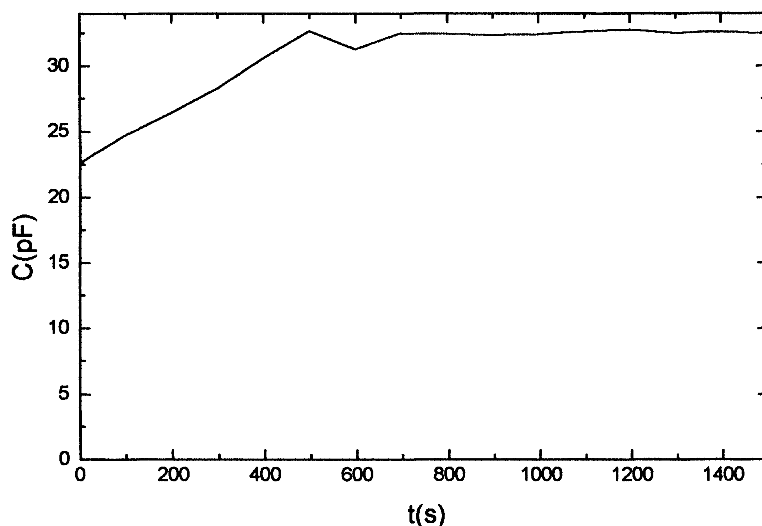

FIGURE 2 Capacitance increase at the inversion region by warming up at room temperature.

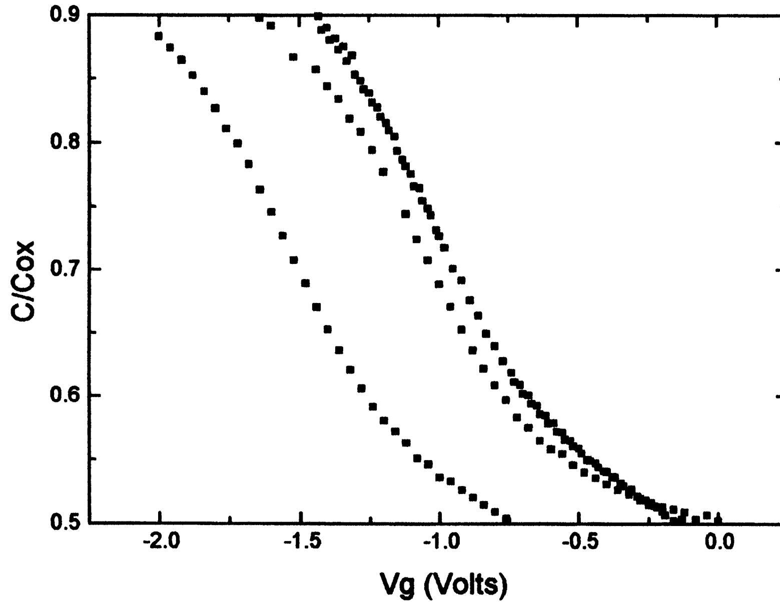

FIGURE 3 Zoom of C-V characteristics. Superposition and expansion of curves obtained for the stressed sample (Fig. 1) and for a non-stressed sample.

tions due to slow-state traps and fixed oxide charges by superposition of both hysteresis cycles. It is a zoom of the two C(V) curves to show the separation of charge and to calculate densities. The total density of oxide trapped charges, N_{ot}, is N_{ot}–N_{ss}+N_{of}, $N_{ot} = 6.8 \times 10^{11}\,\mathrm{cm}^{-2}$.

The total measurement process takes about two hours. It was found that, for an injected electrons density of $N_{inj} = 5 \times 10^{17}\,\mathrm{cm}^{-2}$ and for an applied electric field of $E = 10\,\mathrm{MV/cm}$, the relaxation time t_c is roughly one hour. The parameter α was evaluated, for an applied bias of $V_g = 5\,\mathrm{V}$, to be 0.14 [9].

4. CONCLUSION

We have established a new C(V) method in order to separate slow-state traps from fast-state traps. Various oxide defects can also be separated (as migration ions at high temperature in inversion).

Compared with other methods, the HLTCV displacement method gives new information about slow state traps and mobile species by varying temperature in the inversion region. The relaxation time of slow state traps have been determined together with the densities of slow states, fast states and of oxide fixed charges obtained from voltage shifts measurements.

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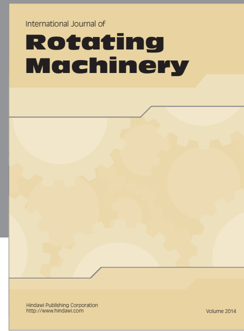
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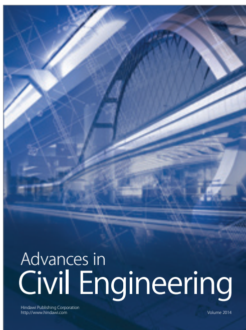
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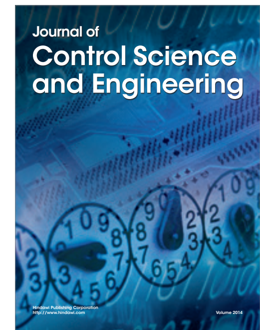
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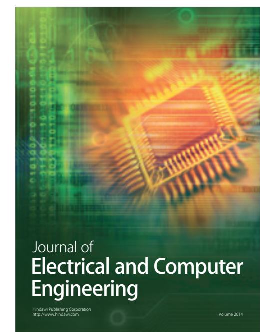
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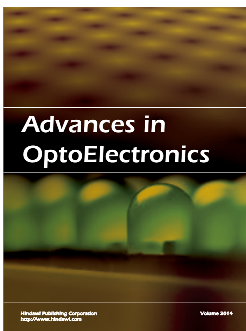
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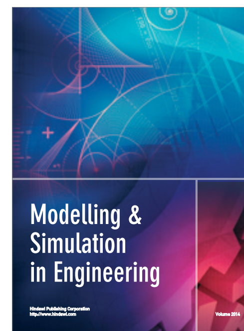
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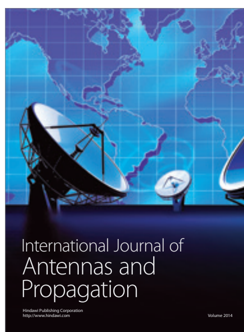
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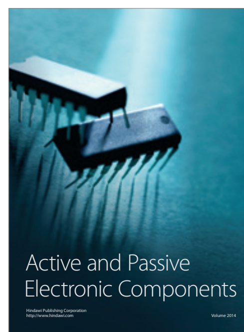
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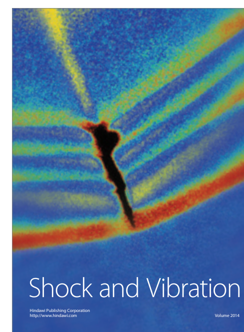
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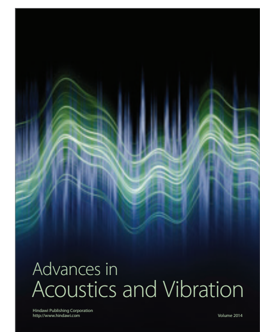
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