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X-BAND MMIC ACTIVE MIXERS

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In this paper two active MMIC mixers for RF front-end applications are described. A down-converter that converts an RF signal ($f_{RF} = 10.45$ GHz) into an IF signal ($f_{IF} = 0.95$ GHz) using an LO signal $f_{LO} = 9.5$ GHz and an up-converter that performs the opposite process have been fabricated. The down-converter is designed using the topology of a dual-gate pHEMT, while the up-converter is implemented in the form of a double balanced mixer using the topology of the Gilbert cell and the occupied areas are approximately 0.78 mm^2 and 3.86 mm^2, respectively. Both mixers present conversion gain, very low input and output return losses, very good isolation between all of their ports and the required LO power is quite low, while the up-converter contains on chip, except for the dc-bias and matching sub-circuits, the required LO and RF baluns. Both circuits have been fabricated using the H-40 process of GEC-Marconi. Section 1 presents fundamentals on mixer circuits theory and mixer design while in Section 2 the characteristics of H-40 process are described. In Section 3 and in Section 4 the designing, the simulated and the measured results of the down-converter and the up-converter are presented, respectively.

1 INTRODUCTION

1.1 Fundamentals on Mixer Theory

Mixers are the most basic elements of the superheterodyne transceivers. They are used to shift signals to frequencies where they can be amplified and demodulated more effectively. Figure 1 shows, for example, the block diagram of a VHF or UHF communication receiver. The receiver has a single-stage input amplifier that increases the strength of the received signal so that it exceeds the noise level of the following stages. The first IF frequency is relatively high. It moves the image frequency well away from the RF, thus allowing the image to be rejected effectively by the input filter. The second conversion occurs after considerable amplification and is used to select some particular signal within the input band and to shift it to the second IF frequency. Many of the same receiver-design considerations apply at microwave frequencies.

A mixer is fundamentally a multiplier. This point is illustrated in Figure 2 which shows an ideal analog multiplier with two sinusoids applied to it. The signal applied to the RF port has a carrier frequency ω_s and a modulation waveform $A(t)$. The LO signal is a pure sinusoid at
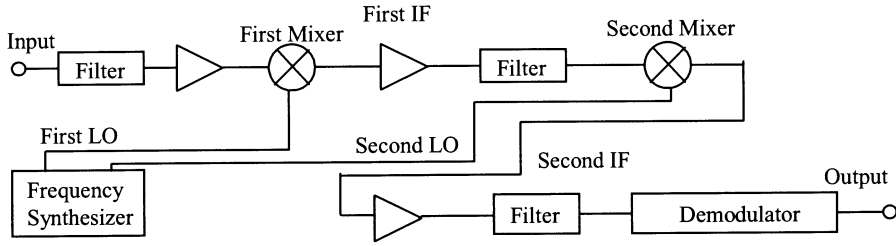
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FIGURE 1   Dual conversion VHF/UHF communication receiver.

frequency ω_p. The output is found to consist of modulated components at the sum and difference frequencies. The sum frequency is rejected by the IF filter, leaving only the difference.

An ideal multiplier is not the only topology that can realize a mixer. Any nonlinear device can perform the multiplying function. The use of such devices results in the generation of LO harmonics and in mixing products other than the desired one. The desired output frequency must be filtered from the resulting frequency spectrum. The use of a nonlinear multiplier can be illustrated by describing the I/V characteristic of the nonlinear device via a power series,

$$I = \alpha_0 + \alpha_1 V + \alpha_2 V^2 + \alpha_3 V^3 + \cdots \tag{1}$$

and letting V equal the sum of the inputs in Figure 2. The output is found to be a signal having the original modulation, but shifted to the difference frequency. If it is assumed that the voltage of the modulated input signal is much smaller than that of the LO, the current contains small-signal components at the frequencies

$$\omega_n = \omega_0 + n\omega_p \tag{2}$$

where ω_0 is the difference frequency $\omega_s - \omega_p$ and $n = \cdots -3, -2, -1, 0, 1, 2, 3, \ldots$ These frequencies are shown in Figure 3 and are separated from each LO harmonic by ω_0.

Another way to view the operation of a mixer is as a switch. Figure 4(a) shows a mixer modeled as a switch, which interrupts the RF voltage waveform periodically at the LO frequency and IF voltage is the product. In some cases the switching waveform might not have a 50% duty cycle, so, in general, it includes all harmonics of its fundamental frequency, plus a dc component. Thus the IF includes a large number of mixing products. The desired output can be separated from the others by filtering. Another switching mixer is shown in Figure 4(b), where instead of simply interrupting the current between the RF and IF ports, the switch changes the polarity of the RF voltage periodically. The advantage of this mixer over the previous is that the LO waveform has no dc component, so the product of the RF voltage and switching waveform does not include any voltage at the RF frequency.
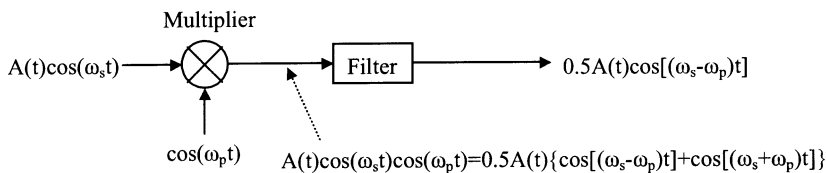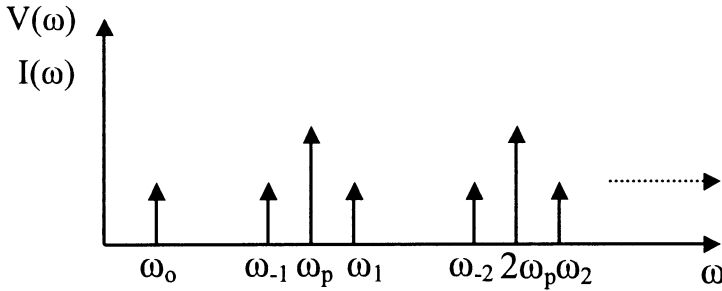

FIGURE 2   A mixer as a multiplier.

FIGURE 3   Small-signal mixing frequencies ω_n.

Thus, even though no filters are used, the RF and LO ports of this mixer are inherently isolated. Doubly balanced mixers are realizations of the polarity-switching mixer.

1.2   Different Structures of Mixers

Single FETs or diodes can be used as mixers. However, designs sometimes combine two, four or even eight components in a balanced structure. Balanced mixers have significant performance advantages compared to single-device mixers. One of these advantages, the inherent RF-to-IF isolation of the polarity-switch mixer has already been described. Another advantage is that the RF and LO are inherently isolated. A balanced mixer also rejects the AM noise from the LO source and certain spurious responses. This rejection occurs because of the phase relationships of the voltages in the circuit and does not require any filtering. Because the input power is divided between multiple devices, the power-handling capability of a balanced mixer is better than that of a single-device mixer. For this reason, as well as its spurious-response rejection, a balanced mixer is usually chosen for applications that strong signals are anticipated. Unfortunately the LO power is divided between the components as well, so the LO power requirements are greater.

Balanced mixers are divided into two classes, called singly balanced mixers and doubly balanced mixers. Singly balanced mixers usually use two devices and are usually realized as two single-device mixers connected by a 180- or 90-deg hybrid. Doubly balanced mixers
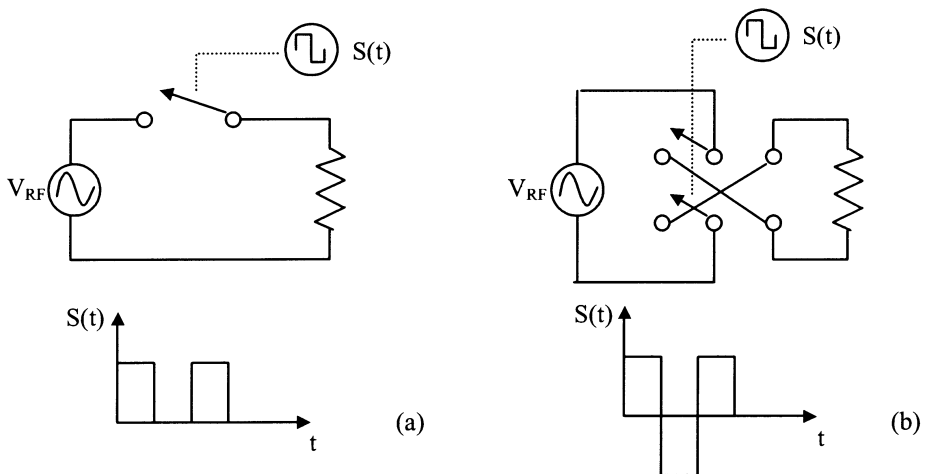

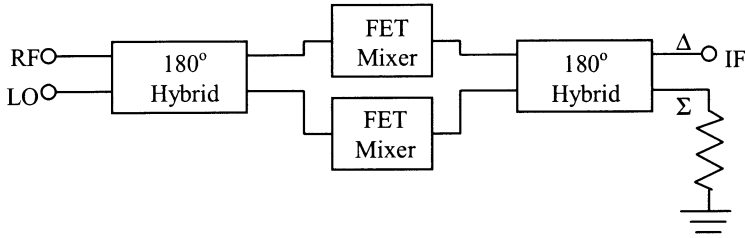FIGURE 4   (a) A simple switching mixer, (b) a polarity-switching mixer.

FIGURE 5   Single balanced FET mixer.

usually consist of four devices interconnected by multiple hybrids, transformers or baluns. They are usually too complicated to allow for individual tuning of the devices, so they may have higher conversion loss or lower gain than single-device or singly balanced mixers.

Balanced FET mixers can be realized with either single-gate or dual-gate devices. Unlike diodes, FETs cannot be reversed and as a result balanced FET mixers require IF hybrids, while diode mixers do not. Figure 5 shows the fundamental type of balanced single-gate FET mixers. The conversion gain and noise figure of an ideal balanced FET mixer are identical to that of a single-device mixer and the output power and intermodulation intercept points are increased 3 dB by the power combining effect of the two devices. In real mixers the loss and imbalance of the hybrids degrade the conversion loss or gain and noise figure and fundamentally limits the rejection of even-order spurious responses.

Doubly balanced FET mixers exhibit the same performance advantages, compared to singly balanced or single-device mixers, as doubly balanced diode mixers: inherent port-to-port isolation, broad bandwidth, and rejection of all even-order spurious responses. However they require hybrids at all ports.

Figure 6 shows a doubly balanced mixer using dual-gate FETs. It consists of four devices connected in a manner reminiscent of the classical Gilbert multiplier used in bipolar transistor analog multipliers. The RF and LO signals are applied to the gates and the IF is extracted from the drains via baluns or microwave hybrids. Of course the mixer requires dc bias and gate and drain matching circuits, which are not shown in the figure. The drains of the FETs are virtual ground points for the RF and LO and as result, in contrast to the single-device mixer, no special circuit is required to provide an RF/LO short to the drains. The baluns, as well as
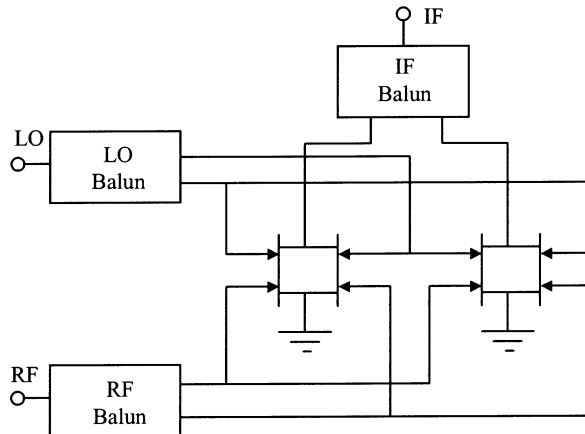

FIGURE 6   Doubly balanced dual-gate FET mixer.

the use of separate gates, provide isolation between the RF and LO. Because the circuit is symmetrical, coupling from the LO to the RF (and RF to LO) must be the same in all devices. The LO leakage through the FETs is coupled equally to both the +RF and −RF terminals of the balun and as result the resulting LO output at the RF port is (ideally) zero.

2 H-40 PROCESS OF GEC MARCONI

The materials' technology foundry of GEC Marconi has developed an advanced GaAs technology, which is used exclusively for designing Monolithic Microwave Integrated Circuits (MMICs) and affords a remarkable repeatability and reliability. The H-40 process provides a complete smart library, which contains linear and nonlinear models of pHEMTs and models of different structures of capacitors, inductors and resistors.

The gate length of the pHEMTs of H-40 process is 0.25 μm and its cut-off frequency is above 40 GHz [1]. The linear models of the HEMTs are based on measurements and are valid only for certain dc bias points and certain gate widths. As a matter of fact they are tables of the s-parameters of the pHEMTs *vs.* frequency. The gate of a pHEMT is divided in multiple fingers, while each finger has the same length. There are several models for different numbers of fingers and lengths. These models provide a linear output power *vs.* input power, independent of the value of the input power. Therefore the compression point can not be defined. The nonlinear models should be used if the compression point should be defined or if the extrapolation of the $I-V$ curves is necessary. It is obvious that in our case (design of mixers) the nonlinear models were used.

The H-40 process supports two kinds of capacitors: nitride capacitors and polyimide capacitors. They have square form, while their dimensions should be between 50 μm × 50 μm and 350 μm × 350 μm. The range of values for the polyimide capacitors is between 0.027 pF and 2.64 pF, while for the nitride capacitors is between 0.52 pF and 58 pF.

The rectangular spiral inductors are fabricated on the second metal layer. There are different kinds of inductors, while each of them has a different line spacing. An inductor should not have more than 10 and less than 1 spirals.

There are two kinds of resistors: the mesa resistors and the nichrome resistors. Given that the resistivity of the two materials is 300 Ω/sq and 50 Ω/sq, respectively, it can be estimated that the values of the mesa resistors are between 10 Ω and 10 kΩ, while the values of the nichrome resistors are between 5 Ω and 2 kΩ.

Finally transmission lines can be fabricated on first metal layer as well as on second metal layer. The second metal layer is usually used because it has a significantly less resistivity than the first layer. Moreover the smart library contains a number of elements like T-junctions and cross-junctions, vias and DC- and RF-pads.

3 DOWN-CONVERTER

3.1 Introduction

Dual-gate FET mixers have one major advantage over single-gate: the LO and RF signals can be applied to separate gates and the mixer has good RF-to-LO isolation. Thus, it is often practical to use a single-device dual-gate FET mixer in applications where a balanced mixer would otherwise be needed (*e.g.* in integrated circuits, where the elimination of a hybrid or a filter saves a significant amount of expensive substrate area).

Dual-gate FETs are best examined as two single-gate FETs in series and their parameters are obtained from measurements of equivalent single-gate devices. GEC Marconi does not

provide the dual-gate FETs technology and as a result we did not only analyze the circuit using this approach but we also designed it using two different single-gate FETs. The LO is applied to the gate of the upper device and the RF to the gate of the lower device. This mode of operation is illustrated in Figure 7. An important property of this topology is that both devices can remain in current-saturation operation over a narrow range of gate-bias voltages. Supposing that we have two identical devices this happens only when $V_{gs1} \approx V_{gs2}$. However applying an LO voltage to the gate of the upper device varies V_{gs2} over a wide range of voltages, so it is impossible for both FETs to remain current-saturated throughout the LO cycle.

It has been well established [2] that the best mode of operation of such a topology is one in which the LO drives the lower FET into and out of current-saturation over the LO cycle. This occurs as the lower FET's drain voltage is forced alternately low and high by the LO. When the drain voltage of the lower FET is low, its transconductance is low and its drain-to-source conductance is relatively high. When this voltage rises, the lower FET enters its current-saturated region, the transconductance is then relatively great and drain-to-source conductance is low. The pumping of these two parameters, g_{ds} and g_m, provides frequency mixing in the lower FET.

The upper FET is in current saturation over the most of the LO cycle. Thus it operates simultaneously as a source-follower amplifier for the LO and a common-gate amplifier for the IF. As with the single-gate mixer, the drain of the upper FET should be short-circuited at the LO frequency. This short-circuit keeps the drain voltage of the pair of FETs constant and guarantees that the upper FET remains in saturation over the most of the LO cycle.

The operation of the lower FET as both a conductance and transconductance mixer has a cost. It can be shown [3] that allowing the FET to enter current saturation causes the average value of $g_{ds}(t)$ to be relatively great. This average conductance is in parallel with the lower FET's channel and causes power loss. Second, because $V_{ds1}(t)$ never reaches zero, the peak value of $g_m(t)$ is not as great as in a single device mixer, and its waveform is also very different. As a result the fundamental-frequency component of $g_m(t)$ is much smaller than in a single-device mixer. Although the operation of the upper FET as a common-gate IF amplifier may make up for these deficiencies to some degree, the loss and thermal noise introduced by the conductance and the degradation of the transconductance are invariably deleterious.

This topology has another fundamental weakness. The upper FET operates as a common-gate amplifier and such amplifiers invariably have poor stability. The unavoidable use of the upper FET as a common-gate amplifier introduces the possibility of unstable operation. It is not unusual for the RF input impedance of the FET at the lower gate to have a negative real part, regardless of the mixer's IF load impedance. Often, the only way to stabilize the mixer in such circumstances is to add a resistance in series with the FET's source and to suffer a reduction in the mixer's conversion gain.
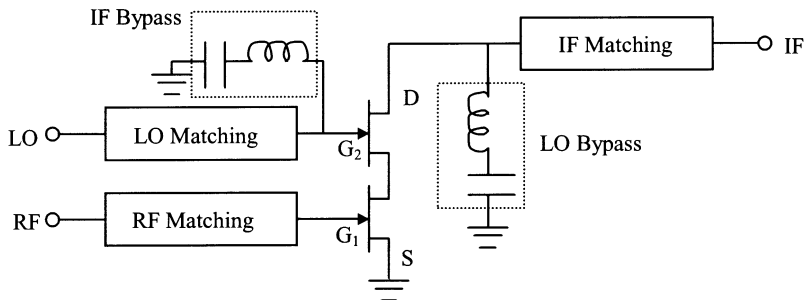

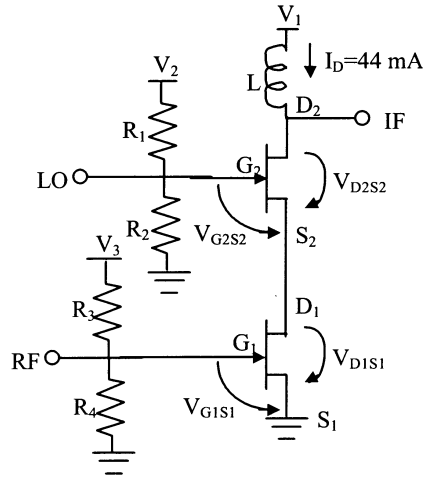FIGURE 7   A mixer topology of two single-gate FETs.

FIGURE 8 DC biased circuit.

3.2 Designing and Simulation Results

For the design of the mixer the nonlinear model of the 4×60 pHEMT of the H40 process of GEC Marconi was used. The lower pHEMT is biased at $V_{D1S1} = 0.7\,V$, $V_{G1S1} = -0.1\,V$ and $I_D = 44\,mA$, while the upper pHEMT is biased at $V_{D2S2} = 3.3\,V$, $V_{G2S2} = -0.45\,V$ and $I_D = 44\,mA$. Therefore the lower pHEMT can easily be driven into and out of the current saturation over the LO cycle, while the upper pHEMT is in current saturation over the entire LO cycle. Given that $V_{D1S1} = 0.7\,V$ and $V_{G2S2} = -0.45\,V$ we determine that $V_{G2S1} = V_{D1S1} + V_{G2S2} = 0.25\,V$ and $V_{D2S1} = V_{D2S2} + V_{D1S1} = 4\,V$. Consequently the necessary voltages are $V_D = V_{D2S1} = 4\,V$, $V_{G2} = V_{G2S1} = 0.25\,V$ and $V_{G1} = V_{G1S1} = -0.1\,V$. Considering that the external dc voltages are $V_1 = +4\,V$, $V_2 = +0.5\,V$ and $V_3 = -0.25\,V$ the necessary voltages can be produced as it is shown in Figure 8.
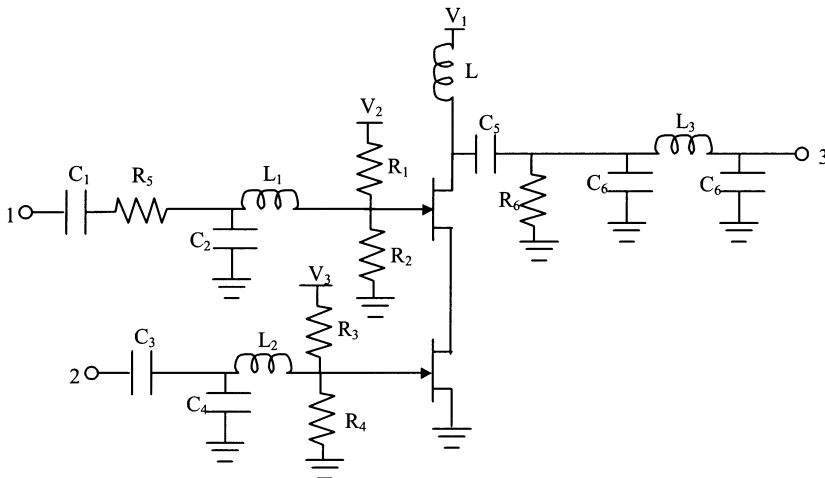

FIGURE 9 DC biased and matched circuit.

TABLE I   Frequency Ranges Where the Reflection
Coefficient of Each Port is Less Than −10 dB.

IF port	dc − 2.35 GHz
LO port	8.2 GHz–11.8 GHz
RF port	9.8 GHz–10.9 GHz

The drain of the upper pHEMT is connected to the dc voltage supply through an inductor, which is not included into the integrated circuit so as it does not occupy a large area of the substrate.

The circuit that is shown in Figure 8 does not have matched ports. It is obvious that the optimum performance of the circuit requires matched ports (Fig. 9). To minimize the occupied area of the substrate, the simplest sub-circuits were used in the design. Table I shows the frequency ranges where the reflection coefficient of each port is less than −10 dB.

In Figure 9, except for the matching sub-circuits, a filter at the IF port can be seen. It is a low-pass filter, it consists of two capacitors and an inductor, its losses are only 0.5 dB (at low frequency) and its passband is 2.1 GHz. The stopband begins at 8.5 GHz where the attenuation is more than 40 dB.

Some simulation results will be presented. Figure 10 shows the conversion gain *vs.* the power of the LO signal and it is obvious that for $P_{LO} \approx 6$ dBm the conversion gain reaches its maximum value. Figure 11 shows the conversion gain *vs.* the power of the RF signal (considering $P_{LO} = 5$ dBm) and it can be seen that the 1 dB input compression point is $P_{RF} = -8$ dBm.

The curves, which are shown in Figure 12, are quite interesting. The conversion gain *vs.* the RF power is presented again while the LO power varies. It can be seen that a positive 1 dB input compression point is attainable when the LO power is greater than 15 dBm. However the conversion gain is then less. A positive 1 dB input compression point could have been succeeded if we had used 4×80 pHEMTs instead of the 4×60. However in this case the
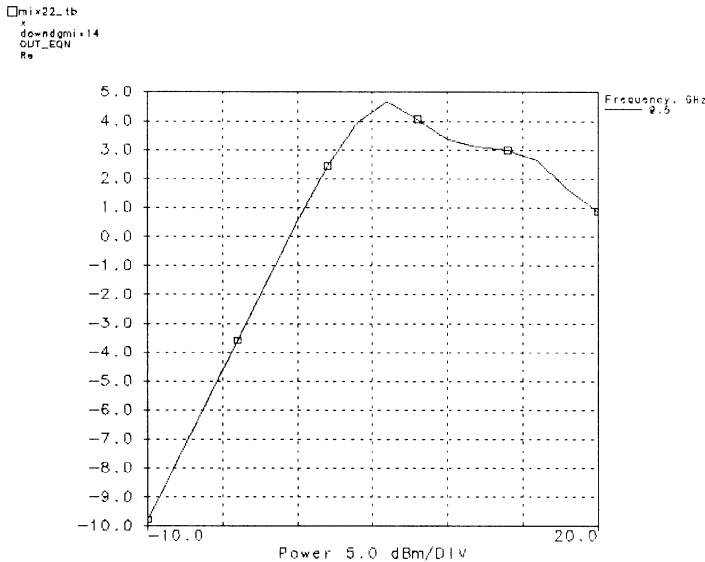

FIGURE 10   Conversion gain *vs.* the power of the LO signal.

□mix22_tb
×
downdgmi,14
OUT_EQN
Rs

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 5.0                                                                    Frequency, GHz
                                                                         9.5
 4.0 ╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌
 3.0 ╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌
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 1.0 ╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌
 0.0 ╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌
-1.0
-2.0
-3.0
-4.0
-5.0
-6.0
-7.0 ─────────────────────────────────────────
    -30.0                                    10.0
         Power 10.0 dBm/DIV
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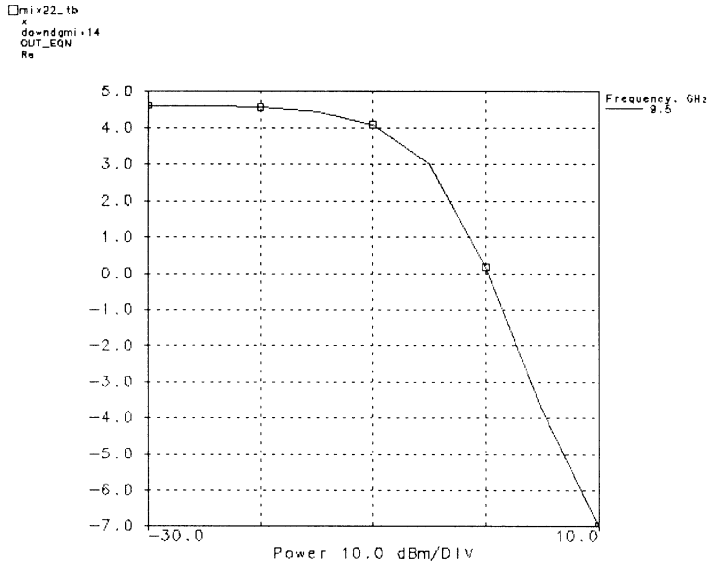
FIGURE 11   Conversion gain *vs.* the power of the RF signal (considering $P_{LO} = 5$ dBm).

drain current would have been greater and the dc consumption much greater than it is now. If the IF output point of the mixer was the drain of the lower pHEMT then a positive 1 dB input compression point could easily be achieved (even more than 7 dBm), while the conversion gain would have a negative value (conversion loss).

The isolation between the ports can be determined obtaining the power spectrum at each port of the mixer (Tab. II). Moreover the suppression of the second and third LO harmonics
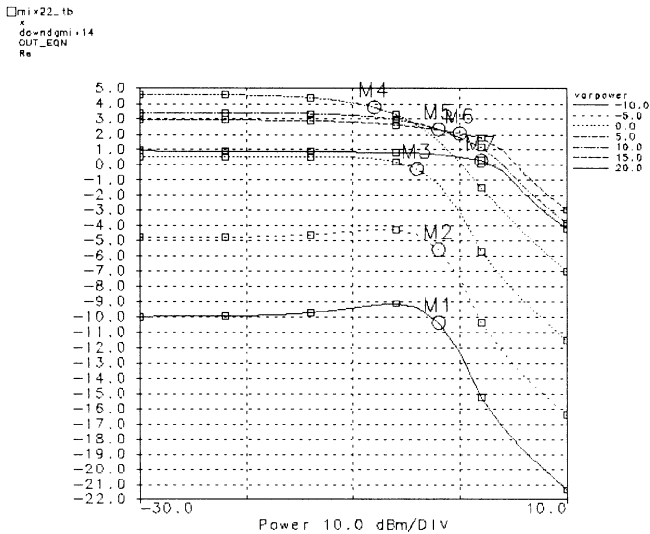
□mix22_tb
×
downdgmi,14
OUT_EQN
Rs

```
  5.0                          M4                      varpower
  4.0                                                    -10.0
  3.0                            M5M6                     -5.0
  2.0                                                      0.0
  1.0                          M3                          5.0
  0.0                                                     10.0
 -1.0                                                     15.0
 -2.0                                                     20.0
 -3.0
 -4.0
 -5.0                          M2
 -6.0
 -7.0
 -8.0
 -9.0                          M1
-10.0
-11.0
-12.0
-13.0
-14.0
-15.0
-16.0
-17.0
-18.0
-19.0
-20.0
-21.0
-22.0 ─────────────────────────────────────────
     -30.0                                   10.0
          Power 10.0 dBm/DIV
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FIGURE 12   Conversion gain *vs.* the RF power while the LO power varies.

TABLE II   Isolation Between the Ports of the Down-converter.

LO-RF isolation	>15 dB
IF-RF isolation	>35 dB
RF-LO isolation	>5 dB
IF-LO isolation	>45 dB
LO-IF isolation	>25 dB
RF-IF isolation	>25 dB

($f = 2f_{LO} = 19$ GHz and $f = 3f_{LO} = 28.5$ GHz, respectively) at the output port is more than 45 dB and 40 dB, respectively.

The final layout of the mixer is shown in Figure 13. The carrier signal, having a frequency of $f_{LO} = 9.5$ GHz, enters into the pad no.1, the RF input signal enters into the pad no.2, while the IF output comes out from the pad no.3. The +4 V dc voltage is connected through an inductor with the pad no.4, while +0.5 V and −0.25 V dc voltages are connected directly with the pads no.5 and no.6 respectively. The integrated circuit measures $817 \, \mu m \times 956 \, \mu m$ and as a result the occupied surface is $0.78 \, mm^2$.

3.3   Measurements

In order for the measurements to be performed, a coaxial test-jig was developed, because otherwise we would need several microwave probe heads in on wafer probe testing environment. The substrate, which was used, is the low cost R04003 Rogers teflon-like material, gold plated, on which thermosonic, gold ball wirebonding was performed at 100°C by a Wedge Border. High purity (99.9999%), 25 μm in diameter Au wire has been used for making the appropriate connections. In Figure 14 the integrated circuit, connected on the test-jig can be seen.

Figure 15 shows the input return losses (s_{11} for LO port and s_{22} for RF port). Both, RF and LO ports, are appropriately matched.

Figure 16 shows the conversion gain *vs.* the power of the LO signal and it is obvious that for $P_{LO} = 3.5$ dBm the conversion gain reaches its maximum value. The conversion gain *vs.*
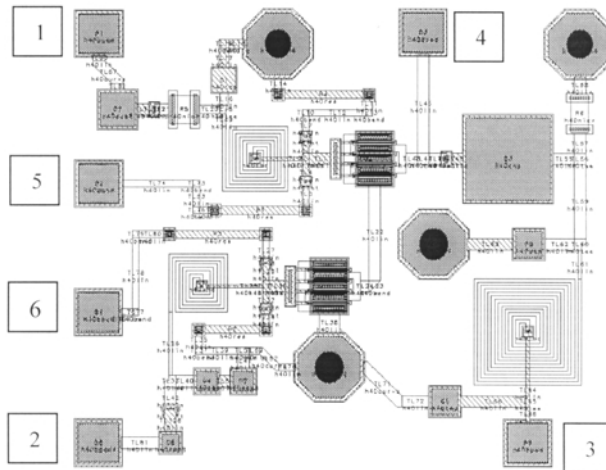

FIGURE 13   Final layout of the down-converter.
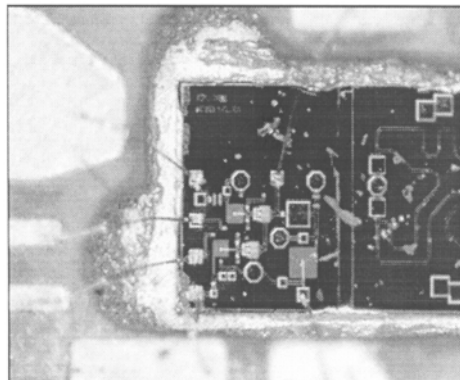
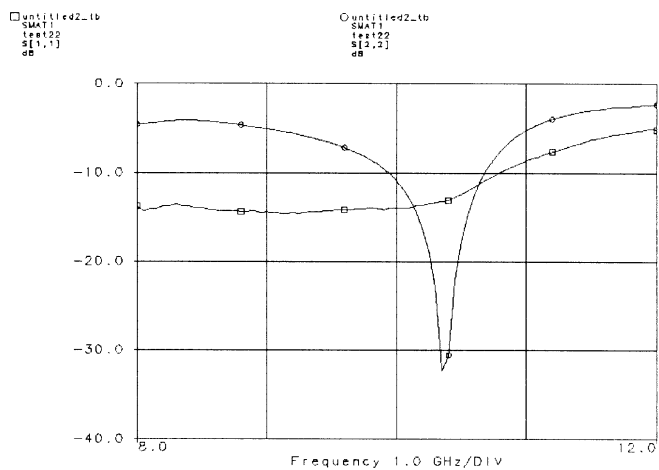FIGURE 14   Photo of the chip.

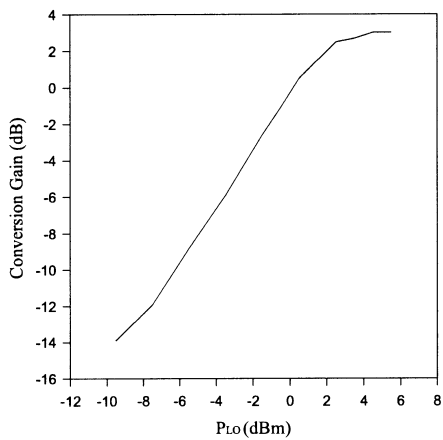FIGURE 15   Input return losses (s_{11} for LO port and s_{22} for RF port).

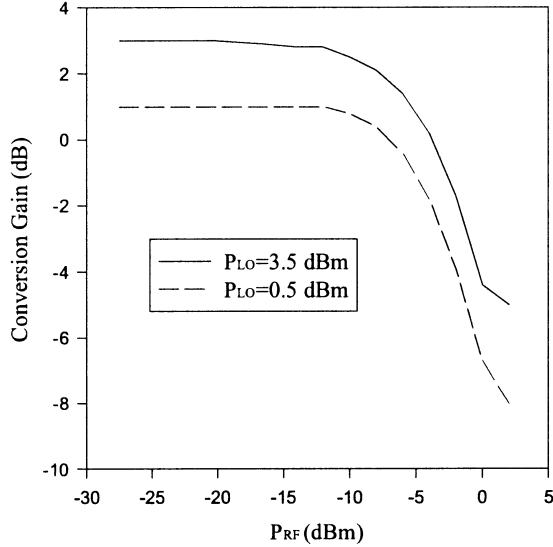FIGURE 16   Conversion gain *vs.* the P_{LO}.

FIGURE 17   Conversion gain *vs.* the P_{RF}.

TABLE III   Down-converter's Specifications.

Conversion gain	3.5 dB
1 dB input compression point	-7 dBm
IIP3	-1 dBm
NF (SSB)	11 dB
Input return losses at RF port	<-10 dB
($9.95\,GHz < f_{RF} < 10.65\,GHz$)	
Input return losses at LO port	<-10 dB
($8.00\,GHz < f_{LO} < 10.65\,GHz$)	
Output return losses at IF port	<-10 dB
($f_{IF} < 2\,GHz$)	
LO-IF isolation	>28 dB
RF-IF isolation	>15 dB

the power of the RF signal is shown in Figure 17 and it can be seen that the 1 dB input compression point is $P_{RF} = -7$ dBm.

Moreover it was measured that IIP3 $= -1$ dBm and NF (SSB) $= 11$ dB. The results are shown in Table III. Very good accordance between the simulation and experimental results has been obtained.

4   UP-CONVERTER

4.1   Introduction

Figure 18 shows a doubly balanced, single-gate mixer, which is exactly the topology that was used for the up-converter. An IF balun is used to drive the lower pHEMTs of the pairs out of phase and as result the drains of the upper devices must be interconnected in the relatively complex manner shown. The points where the upper pHEMTs' drains are connected are virtual grounds for both the RF and LO signals, so the optimum termination is provided
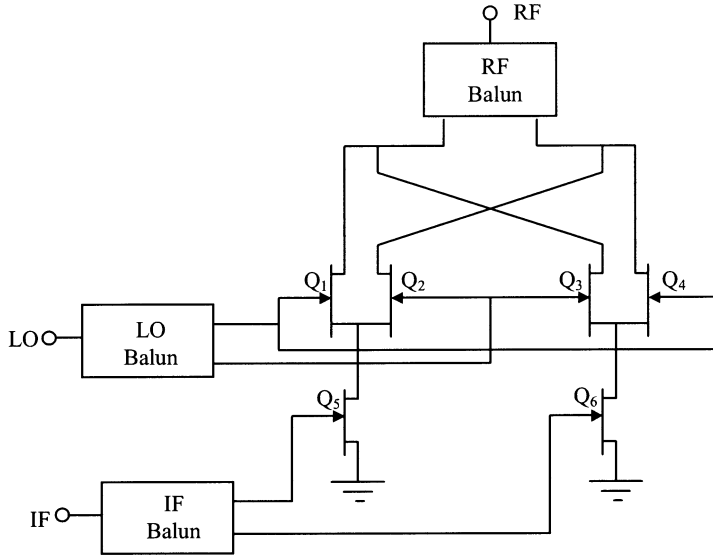
FIGURE 18   Doubly balanced pHEMT mixer using single-gate pHEMTs.

to the devices without the need for any additional filtering. Another advantage of this circuit is that the parallel combination of the drains causes the RF output impedance to be half that of the singly balanced version, providing an impedance that is more practical to match to the RF load.

The circuit that was designed does not contain the IF balun while it contains both RF and LO baluns. Some details of these baluns will be following discussed.

4.2   RF Balun

As it has been already noticed a microwave 180-deg hybrid coupler is used for the combination of the drains of Q_1, Q_2, Q_3 and Q_4 pHEMTs. A microwave 180-deg hybrid coupler is a four port device having a special set of characteristics: (1) all ports are matched, (2) RF power applied to any one port is split equally between two of the other ports, (3) the signals at the output ports have an 180-deg phase difference and (4) the remaining port is isolated. Therefore an ideal 180-deg hybrid has the S matrix

$$S_{180} = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & -1 & 1 & 0 \\ -1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix} \tag{3}$$

Equation (3) implies specific phase shifts between the input and output ports. In real hybrids, the input-to-output phase shift is rarely important, but the phase difference between the two output ports is critical. Real hybrids differ from the ideal hybrid described above in several ways: the most important nonidealities are phase and amplitude balance, loss and VSWR. Balance refers to the matching of phase and power levels at any two output ports. Phase balance is the deviation in phase from the ideal phase difference between any pair of outputs, and amplitude balance is the difference in output amplitude, usually expressed in dB.
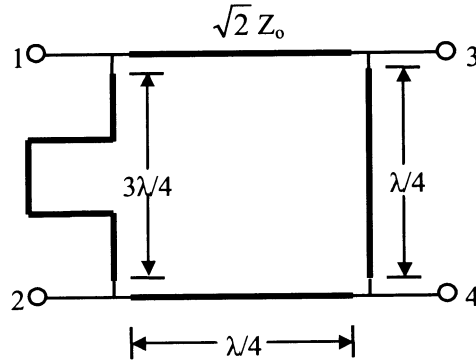
FIGURE 19   A microwave 180-deg hybrid coupler.

Isolation is the ratio of power at the isolated port to that applied at the input. Isolation and balance are usually frequency-dependent and may be different for different pairs of ports. They are generally the same only if the hybrid has a symmetrical structure. Like all other real components, microwave hybrids introduce some dissipative power loss, which is usually specified as loss above the unavoidable 3 dB of coupling loss.

One of the simplest 180-deg coupler to design is the so-called "rat-race" or ring hybrid (Fig. 19). It consists of four transmission line parts; three of them are 0.25 wavelengths while the fourth is 0.75 wavelengths. The characteristic impedance of these parts is $\sqrt{2}\, Z_o$ where Z_o is the port impedance (usually $50\,\Omega$).

It can easily be calculated that the lengths of the transmission line parts, which are required for our application are $(\lambda/4) = 2750\,\mu m$ and $(3\lambda/4) = 8250\,\mu m$, which are extremely long for a MMIC. It is known that a distributed inductance connected with a distributed shunt capacitance is a very good model of a transmission line. Therefore a sorter transmission line would have smaller inductance and capacitance. The reduction of the inductance can easily be balanced using increased characteristic impedance, while the reduction of the capacitance can be balanced using two lumped, shunt capacitances at either end (Fig. 20).

The relations between Z, Z_o, C and θ can easily be determined [4]:

$$Z = \frac{Z_o}{\sin\theta} \quad \text{and} \quad \omega C = \frac{\cos\theta}{Z_o} \tag{4}$$

Equations (4) show that electrical length can be smaller if the values of the characteristic impedance Z and the capacitors C are increased. This topology is very convenient for MMIC

(a)   (b)
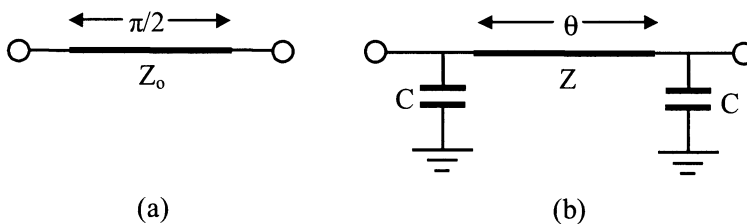
FIGURE 20   (a) $\lambda/4$ wavelength transmission line, (b) equivalent topology using a transmission line of electrical length $\theta < \pi/2$ and characteristic impedance $Z > Z_o$ and two shunt capacitors C.
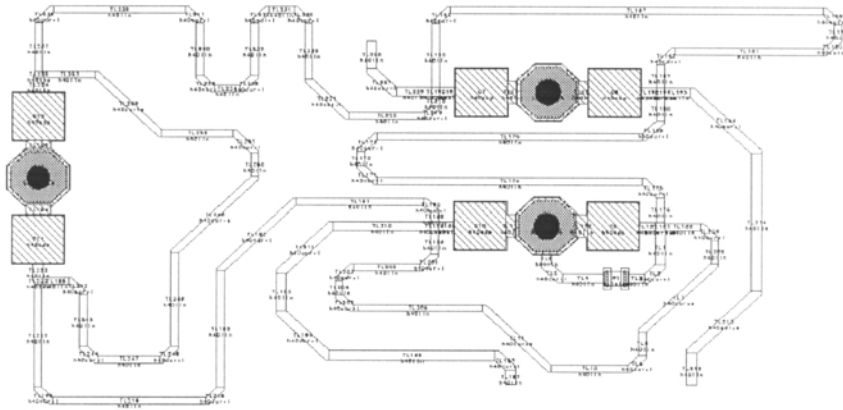
FIGURE 21   The 180-deg coupler's final layout.

designs because the required lumped capacitors can easily be realized. This technique was used so as a much smaller area to be occupied by the 180-deg coupler. The quarter-wavelength transmission sections were replaced by the equivalent circuit of Figure 20(b), while three such circuits in series were used for the replacement of the 0.75-wavelength transmission section.

Figure 21 shows the 180-deg coupler's final layout. It occupies the smallest possible area and at the same time it is placed in such a way that can be easily connected with the other sub-circuits of the design. Only three ports can be recognized because the fourth is terminated with a $50\,\Omega$ impedance.

In Figure 22 the transmission coefficients ($|s_{21}|$ and $|s_{31}|$) and the isolation ($|s_{23}|$) between the output ports can be seen. In Table IV the exact values of all important s-parameters of the coupler into the desired frequency range are presented.
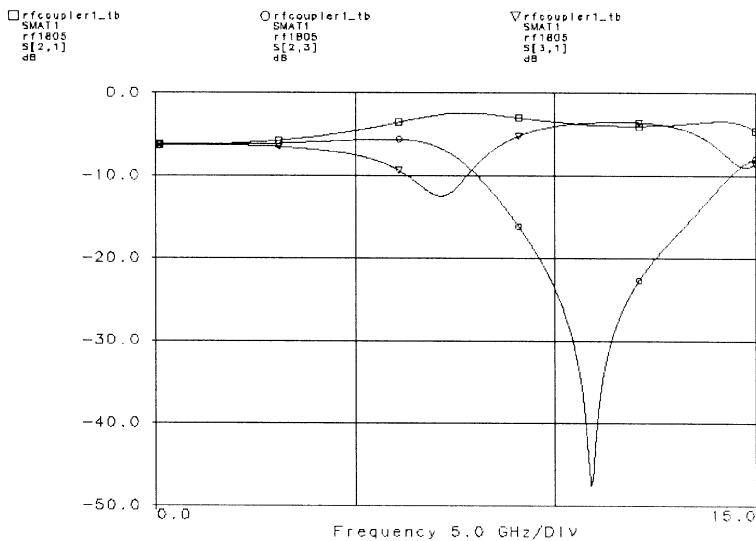

FIGURE 22   Transmission coefficients ($|s_{21}|$ and $|s_{31}|$) and isolation ($|s_{23}|$) between the output ports.

TABLE IV Exact Values of All Important s-parameters Into the Desired Frequency Range.

Frequency (GHz)	s-parameters (dB)					
	$|s_{11}|$	$|s_{22}|$	$|s_{33}|$	$|s_{23}|$	$|s_{21}|$	$|s_{31}|$
10.15	−21.0	−19.7	−16.3	−25.4	−3.56	−3.94
10.45	−21.7	−21.2	−16.5	−30.1	−3.69	−3.76
10.75	−22.1	−22.1	−16.7	−38.9	−3.80	−3.64

The phase difference between the two output ports at the central frequency is almost 181°, while the total deviation of its value for a 200 MHz frequency range around the central frequency is smaller than 2°.

It is known that the appropriate operation of the up-converter depends a lot on the accurate operation of the coupler. In order to be sure that the coupler has the desired performance, it was fabricated and measured using a probe station separately. Table V shows the exact measured values of all important s-parameters into the desired frequency range.

The phase difference between the two output ports at the central frequency is almost 202°, while the total deviation of its value for a 800 MHz frequency range around the central frequency is smaller than 2°.

It is obvious that simulation and measured results are not identical, although the reflection coefficients at each port are still very good. The transmission coefficients have losses that are about 1.5 dB, while, and this is more important, there is an amplitude balance that is almost 1 dB. The measured results for the isolation coefficient ($|s_{23}|$) are also quite different from the simulated results. That means that the isolation between the two output ports is hardly more than 10 dB. A significant difference between the simulated and the measured value of the phase difference is noticed. The measured value of the phase difference is 202°, that is 20° higher than the desired result.

One possible reason could be that the models of the capacitors and transmission line sections are not as accurate as we would like and the fact that we used a lot of small transmission line sections in order to design the 180-deg coupler made this problem even bigger. Coupling between the different sections must have played a key role. A lot of small sections were used and placed quite near each other so as the design to have as compact form as possible. A quite different phase difference than 180° was expected and that is why numerous simulations were performed, before the fabrication of the circuit, trying to see the effects that these differences would have to the total performance of the up-converter. The effects will not be disastrous. The total gain of the up-converter will not be reduced more than 1.5 dB from the theoretical value, while the suppression of the LO signal at the output of the mixer will remain quite good.

TABLE V Exact Measured Values of All Important s-parameters Into the Desired Frequency Range.

Frequency (GHz)	s-parameters (dB)					
	$|s_{11}|$	$|s_{22}|$	$|s_{33}|$	$|s_{23}|$	$|s_{21}|$	$|s_{31}|$
10.15	−17.5	−13.2	−19.4	−9.7	−4.50	−5.89
10.45	−18.1	−11.9	−26.7	−10.8	−4.60	−5.22
10.75	−17.1	−10.1	−19.2	−12.0	−4.43	−4.89

4.3 LO Balun

As it has already been noticed a microwave 180-deg hybrid coupler is needed for the appropriate application of the LO signal to the gates of Q_1, Q_2, Q_3 and Q_4 pHEMTs. The LO coupler could look like the RF coupler that was presented to the previous paragraph. Given that the LO frequency is lower than the RF frequency it is obvious that the LO coupler would occupy a much larger area than the RF coupler. It must be noticed here that the LO coupler operates as a power divider and not as a power combiner. As a result the ordinary passive coupler can be replaced by an active coupler. Not only is the occupied area smaller, but can also the 3 dB coupling loss be avoided. Unfortunately an active coupler suffers from a number of problems:

— It is often not possible to optimize its noise figure simultaneously with broad bandwidth and good phase and amplitude balance.
— Constraints on the design, introduced by the need for good balance and broad bandwidth, may make it impossible to design the coupler to achieve low IM distortion.
— Amplitude and phase balance of the coupler are often poor.
— The coupler's impedances at frequency response are often different at its outputs.

Figure 23 shows an active divider. It uses the well-known property of a transistor amplifier in which the signals at its drain and source have, ideally, a 180-deg phase difference. In practice, this property exists only in low frequencies, and the voltage gain between the input and the two outputs is, in general, unequal. In our application the divider should operate only for a specific frequency and as result good phase and amplitude balance and good matching of all ports can easily be succeeded.

For the design of the coupler the nonlinear model of the 4×40 pHEMT was used. Given that the drain as well as the source of the pHEMT are considered as outputs, the transistor is biased at $V_{DS} = 3.1\,V$, $V_{GS} = -0.3\,V$ and $I_D = 37\,mA$. A $50\,\Omega$ impedance is connected to the source so as matching can easily be achieved while the voltage drop has such a value that the external required dc voltage is $V_D = 5\,V$. Moreover the required dc voltage at the gate is $V_G = 1.55\,V$ and can be produced by a voltage divider as it is shown in Figure 24.

In Figure 25 in addition to the DC-bias sub-circuits, the matching sub-circuits can be seen. Table VI shows the values of the s-parameters into the desired frequency range. It can be seen that the reflection coefficients of all ports (input and outputs) have appropriate values, while the transmission coefficients presents gain that is more than 0.5 dB. The amplitude balance is extremely good for an active coupler. The phase difference between the two output ports at the central frequency is almost $179°$, while the total deviation of its value for a 1 GHz frequency range around the central frequency is smaller than $1.5°$.
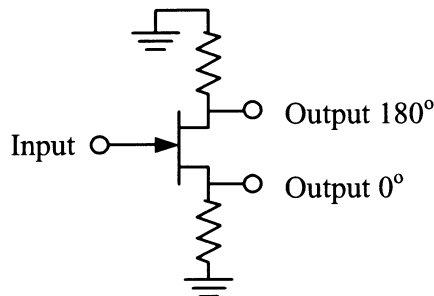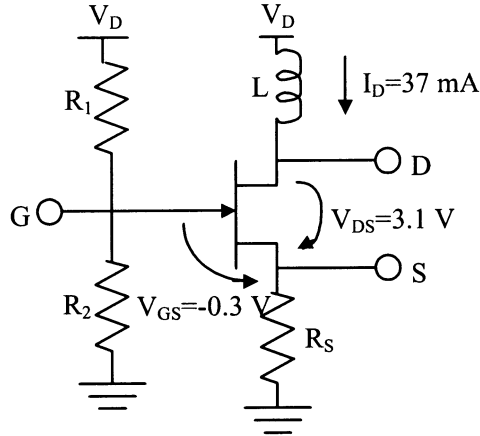

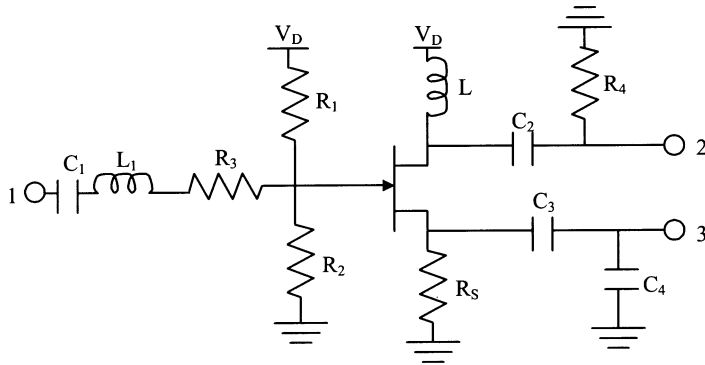FIGURE 23   Active coupler.

FIGURE 24   DC biased circuit.

FIGURE 25   DC biased and matched circuit.

TABLE VI   Exact Values of the s-parameters Into the Desired Frequency Range.

	s-parameters (dB)				
Frequency (GHz)	$\lvert s_{11} \rvert$	$\lvert s_{22} \rvert$	$\lvert s_{33} \rvert$	$\lvert s_{21} \rvert$	$\lvert s_{31} \rvert$
9.0	− 14.2	− 11.8	− 10.0	0.70	0.53
9.5	− 18.4	− 11.2	− 11.3	0.59	0.26
10.0	− 18.5	− 10.6	− 12.3	0.38	− 0.12

Another difference between an active and a passive coupler is that the active one is not a completely linear device. That means that the conversion gain is reduced when the power of the input signal is greater than a certain value. Figure 26 shows the transmission gains of both outputs *vs.* the power of the input signal. It is quite impressive that both curves have the same form and it can be seen that the 1 dB input compression point is $P_{LO} = 9$ dBm. Therefore the coupler has a linear behaviour as long as the power of the input signal is less than 9 dBm.

The final layout of the active coupler is shown in Figure 27. The carrier signal, having a frequency of $f_{LO} = 9.5$ GHz, enters into the port no. 1, while at ports no. 2 and no. 3 two
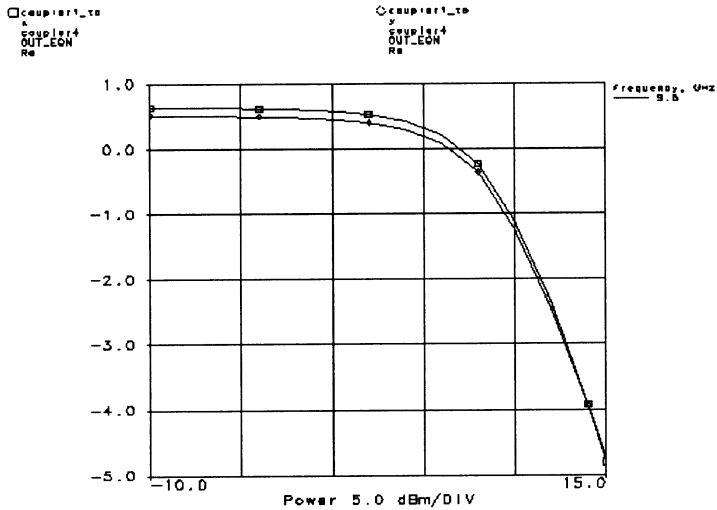
FIGURE 26   Transmission gain *vs.* the power of the LO input signal.

identical signals are produced having an 180-deg phase difference. The $+5\,\mathrm{V}$ dc voltage is connected to both no. 4 and no. 5 pads.

4.4   Designing and Simulation Results

For the design of the active part of the up-converter the nonlinear model of the 4×40 pHEMT was used. As it has already been mentioned Q_5 and Q_6 pHEMTs are the current sources while Q_1, Q_2, Q_3 and Q_4 operate as switches (Fig. 28). Therefore the latter pHEMTs must be biased near the cut-off region while Q_5 and Q_6 pHEMTs must be biased at a point where their dc current is double of the dc current of the rest four pHEMTs. It was chosen
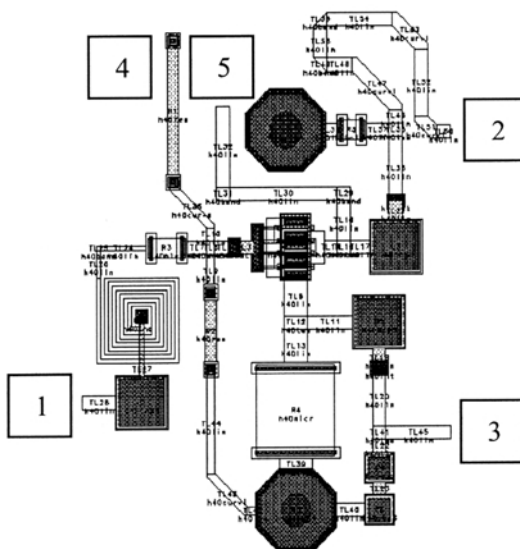

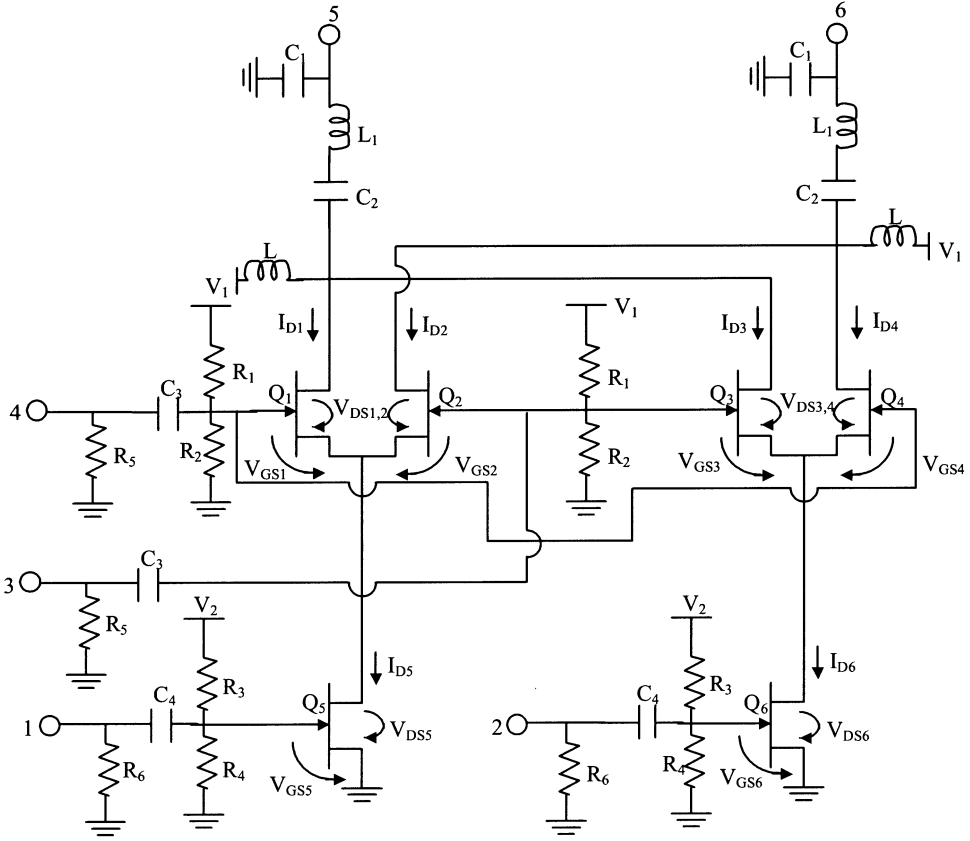FIGURE 27   Final layout of the active coupler.

FIGURE 28   Matched and dc biased active part of the up-converter.

$V_{DS1} = V_{DS2} = V_{DS3} = V_{DS4} = 2.5 \text{ V}$ and $V_{GS1} = V_{GS2} = V_{GS3} = V_{GS4} = -0.75 \text{ V}$ and therefore the dc current is $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 9 \text{ mA}$. As a result the dc bias point of the other two pHEMTs has $V_{DS5} = V_{DS6} = 2.5 \text{ V}$ and $V_{GS5} = V_{GS6} = -0.6 \text{ V}$ so as the dc current to be $I_{D5,6} = 2I_{D1,2,3,4} = 18 \text{ mA}$.

Given that $V_{DS5,6} = 2.5 \text{ V}$ and $V_{GS1,2,3,4} = -0.75 \text{ V}$ it can easily be calculated that $V_{G1,2,3,4} = V_{DS5,6} + V_{GS1,2,3,4} = 1.75 \text{ V}$. Moreover $V_{D1,2,3,4} = V_{DS1,2,3,4} + V_{DS5,6} = 5 \text{ V}$ which means that the required dc external voltages are $V_{D1,2,3,4} = 5 \text{ V}$, $V_{G1,2,3,4} = 1.75 \text{ V}$ and $V_{G5,6} = -0.6 \text{ V}$. Considering that only $V_1 = +5 \text{ V}$ and $V_2 = -1.5 \text{ V}$ are the available external dc voltages, the required dc voltages can be produced by voltage dividers. In Figure 28 in addition to the pHEMTs and the voltage dividers, the matching sub-circuits can be seen.

In this paragraph some simulation results will be presented. The design does not include an IF coupler. Therefore an ideal model of an IF coupler was used that features no power loss, except for the 3 dB coupling loss. Figure 29 shows the conversion gain *vs.* the power of the LO signal and it is obvious that for $P_{LO} \approx 7 \text{ dBm}$ the conversion gain reaches its maximum value.

Figure 30 shows the conversion gain *vs.* the power of the IF signal (considering $P_{LO} = 7 \text{ dBm}$) and it can be seen that the 1 dB input compression point is $P_{IF} = 5 \text{ dBm}$.

Obtaining the power spectrum at each port of the mixer we determine the isolation between the ports (Tab. VII). Moreover the suppression of the second and third LO harmonics
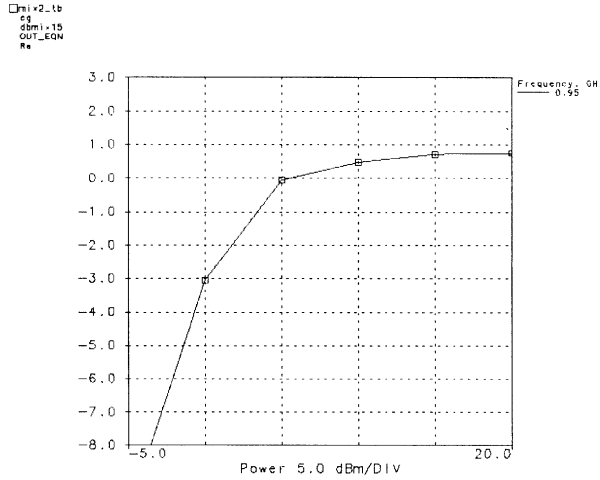
FIGURE 29   Conversion gain *vs.* the power of the LO signal.

($f = 2f_{\text{LO}} = 19$ GHz and $f = 3f_{\text{LO}} = 28.5$ GHz, respectively) at the output port is more than 35 dB and 55 dB, respectively.

The final layout of the mixer is shown in Figure 31. The carrier signal, having a frequency of $f_{\text{LO}} = 9.5$ GHz, enters into the pad no. 1, while the RF output comes out from the pad no. 4. The IF signal and its reverse (there is an 180-deg phase difference between them) enter into the pads no. 2 and no. 3., respectively. The $+5$ V dc voltage is connected with the pads no. 5, no. 6, no. 7, no. 8 and no. 9, while -1.5 V dc voltage is connected directly with the pads no. 10 and no. 11. The integrated circuit measures $1831\,\mu\text{m} \times 2107\,\mu\text{m}$ and as a result the occupied surface is $3.86\,\text{mm}^2$.
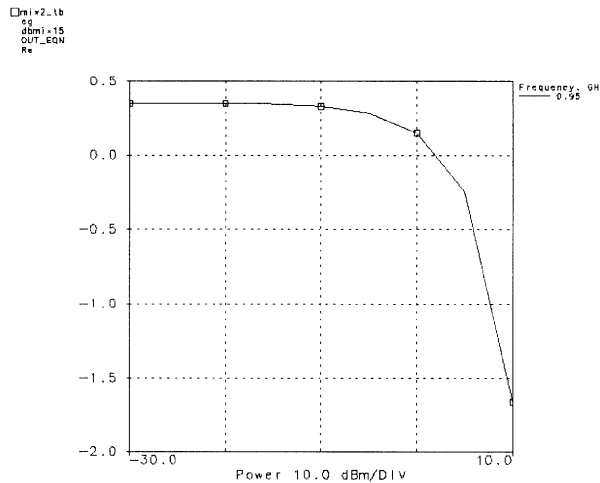

FIGURE 30   Conversion gain *vs.* the power of the IF signal (considering $P_{\text{LO}} = 7$ dBm).

TABLE VII   Isolation Between the Ports of the Up-converter.

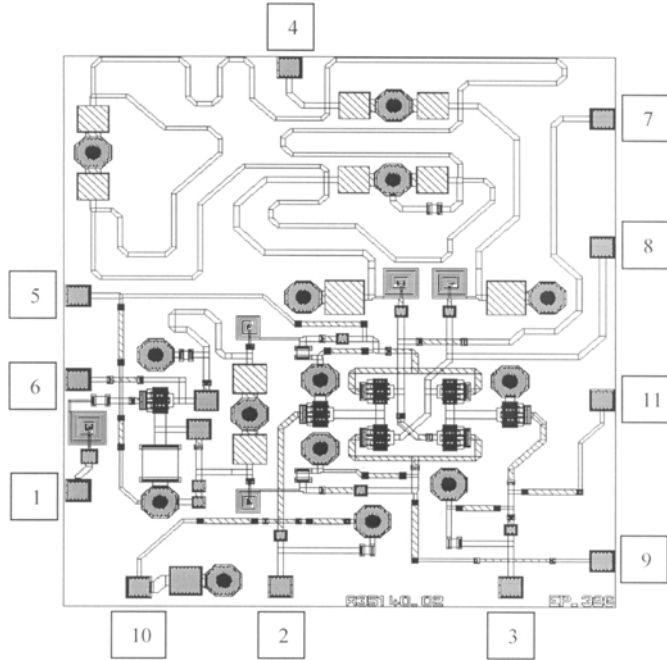|	
LO-IF isolation	$>50\,\text{dB}$
RF-IF isolation	$>40\,\text{dB}$
IF-LO isolation	$>100\,\text{dB}$
RF-LO isolation	$>45\,\text{dB}$
LO-RF isolation	$>40\,\text{dB}$
IF-RF isolation	$>35\,\text{dB}$

FIGURE 31   Final layout of the up-converter.

4.5. Measurements

In order for the measurements to be performed, a coaxial test-jig was developed, similar to that, which was used for the measurements of the down-converter. The same substrate was used and thermosonic, gold ball wirebonding was performed. In Figure 32 the integrated circuit, connected on the test-jig can be seen.

Figure 33 shows the input and output return losses (s_{11} for LO input port and s_{22} for RF output port). Both, RF and LO ports, are appropriately matched.

Figure 34 shows the conversion loss vs. the power of the LO signal and it is obvious that for $P_{LO} = 6$ dBm the conversion loss reaches its minimum value. The conversion loss vs. the power of the IF signal is shown in Figure 35 and it can be seen that the 1 dB input compression point is $P_{IF} = 2$ dBm.

Comparing Figures 29 and 34 it is clear that there is a difference of 6 dB between the simulated and measured results. These losses are due to the imperfect operation of the external
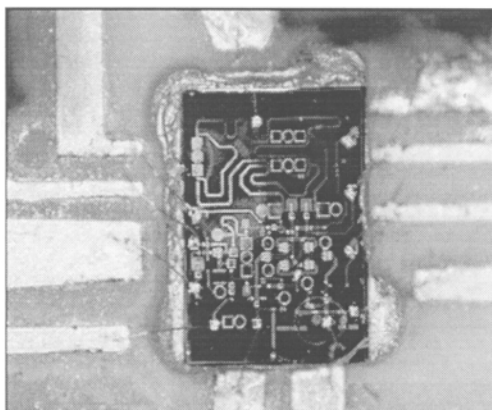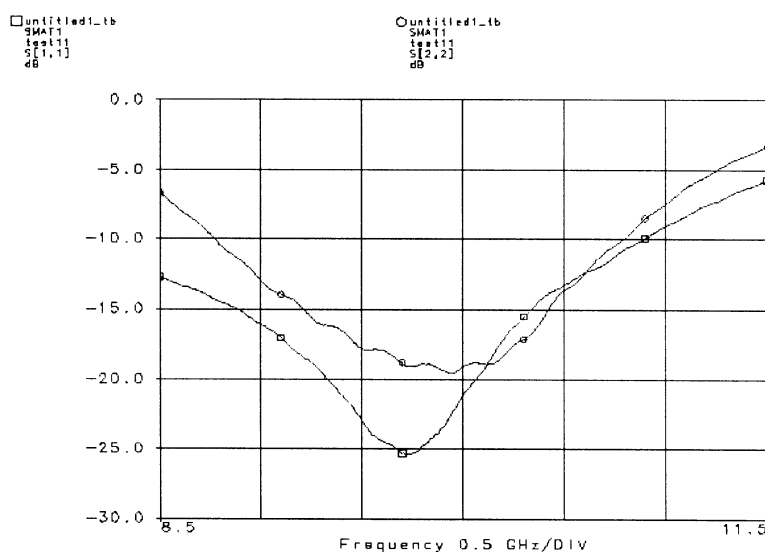
FIGURE 32   Photo of the chip.

FIGURE 33   Input and output return losses (s_{11} for LO input port and s_{22} for RF output port).

dc sub-circuits, which were used during the measurements. A more careful design of these external sub-circuits would minimize the difference.

5   CONCLUSION

Two active MMIC mixers have been designed and implemented using the H-40 process of GEC Marconi. Both mixers present conversion gain, very low input and output return losses, very good isolation between all of their ports and the required LO power is quite low, while the up-converter contains on chip, except for the dc-bias and matching sub-circuits, the required LO and RF baluns. Very good agreement between the simulation and experimental results has been demonstrated.
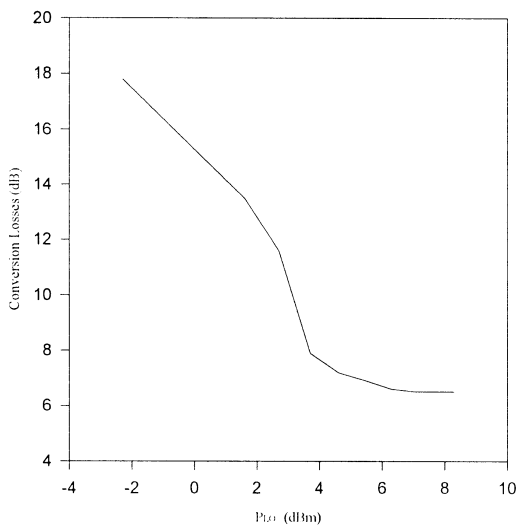
FIGURE 34   Conversion loss vs. the P_{LO}.
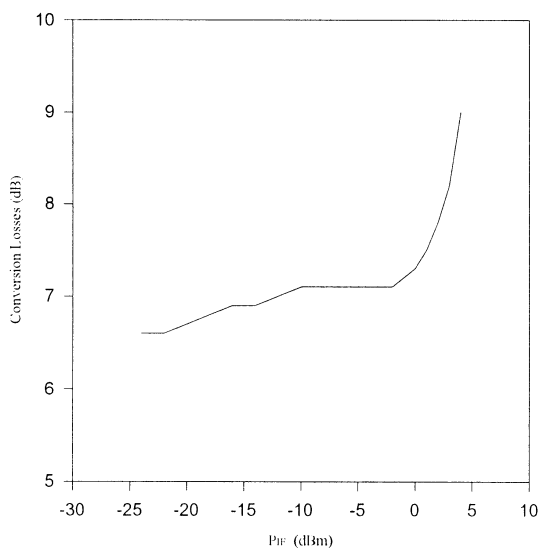
FIGURE 35   Conversion loss vs. the P_{IF}.

Acknowledgement

References

[1] H-40 Process' manual of GEC Marconi.
[2] Tsironis, C., Meirer, R. and Stahlmann, R. (1984). Dual-gate MESFET mixers. *IEEE Trans. Microwave Theory Tech.*, **MTT-35**, 248.
[3] Maas, S. A. (1993). *Microwave Mixers*, 2nd edn. Artech House.
[4] Rajesh Mongia, Inder Bahl, Prakash Bhartia. (1999). *RF and Microwave Coupled-line Circuits*. Artech House.

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