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Research Article

SBT Approach towards Analog Electronic Circuit Fault Diagnosis

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An approach for the fault diagnosis of single and multiple faults in linear analog electronic circuits is proposed in this paper. The simulation-before-test (SBT) diagnosis approach proposed in this write up basically consists of obtaining the frequency response of fault free/faulty circuit. The peak frequency and the peak amplitude from the error response are observed and processed suitably to extract distinct signatures for faulty and nonfaulty conditions under maximum tolerance conditions for other network components. The artificial neural network classifiers are then used for the classification of fault. Networks of reasonable dimensions are shown to be capable of robust diagnosis of analog circuits including effects due to tolerances. This is a unique contribution of this paper. Fault computation time is drastically reduced from the traditional analysis techniques. This results in a direct dollar savings at test time. A comparison of the proposed work with the previous works which also employ preprocessing techniques, reveals that our algorithm performs significantly better in fault diagnosis of analog circuits due to our proposed preprocessing techniques.

1. INTRODUCTION

The fault diagnosis process in digital systems has successfully reached a point of automation; however, for analog electronic circuits the diagnosis approach relies heavily on the test engineer's experience and intuition. The detailed knowledge of the circuit operational characteristics is required for developing test strategies. Owing to this, analog fault detection and identification task is still iterative and time consuming. The present state in electronic circuit manufacturing has introduced analog and analog/digital hybrid circuits where the circuit under test is quite large. Hence a systematic approach to automate the fault diagnostic task in these circuits wherein intuition and experience may no longer be sufficient [1–3] is highly required.

Several researches [2, 4, 5] have addressed the issue of fault diagnosis of analog electronic circuits at the system board and chip level. The research areas in this domain [6] encompass computational complexity, automatic test pattern generation, and design for testing process. Analog fault diagnosis is complicated by poor mathematical model, component tolerances, nonlinear behavior of components, and limited accessibility to internal nodes of the circuit under test. The general analog diagnosis algorithm falls under two categories (simulation after test and simulation before test). Simulation after test diagnosis technique uses traditional artificial intelligence and reasoning methods. The disadvantage of this method is that it increases the time spent on diagnosis at the production time. On the other hand, the simulation-before-test approach develops a fault data dictionary with which the test data is compared and the corresponding state of the system is reported. This approach, though requires more initial computation cost, can provide faster diagnosis at the production time.

The difficulties encountered in analog fault diagnosis make the use of artificial neural network (ANN) quite appealing. The research presented here attempts to exploit the signature analysis capabilities of artificial neural networks [7] to provide fault diagnosis with minimal computational cost. The proposed method is a form of SBT with ANN serving the role of the classifier [8]. The SBT approach basically consists of obtaining the standard frequency response of the fault free/faulty circuit topology. The peak frequency and the peak amplitude from the error response are extracted and preprocessed to deduce distinct signatures to be fed into ANN for classification.

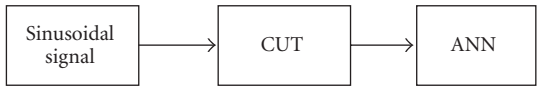

Figure 1: General testing framework.

The paper is organized as follows. Section 2 introduces the general analog circuit frame work. The proposed algorithm is given in Section 3. Section 4 details the preprocessor and ANN. The experiments results are demonstrated in Section 5. Section 6 covers with a brief discussion on the comparison of the proposed technique with certain notable contributions made in this area by the researches. Section 7 concludes the paper.

2. GENERAL TESTING FRAMEWORK

Figure 1 shows the basic diagnostic system for the circuit under test (CUT). A sinusoidal signal of the unit amplitude is applied to the CUT and the frequency response of the circuit is analyzed for faulty and nonfaulty circuital conditions.

The maximum and minimum limits of error amplitude of the faulty circuits at the appropriate test frequency are listed for all faults. Under faulty conditions if the output falls within these maximum limits suitable signature is fed into the ANN which is suitably trained for fault classification.

3. PROPOSED FAULT DIAGNOSIS ALGORITHM

(1) The transfer function model, $G(s)$, of the CUT is derived for nominal value of the circuit components.
(2) The frequency response of the CUT is simulated under different faulty conditions and peak frequency ω_p peak amplitude $M(\omega_p)$ is obtained. This peak frequency will serve as the test frequency for fault diagnosis.
(3) Obtain the extreme fault bounds for various faults at corresponding test frequencies, that is, finding the upper fault limit (X_H), with the faulty component at $\pm 50\%$ ($R \pm 50\%R$) and all the other network components at the maximum positive tolerance limit error magnitude is determined. Similarly the lower bound (X_L) is determined for the maximum negative tolerance value for the other network components.
(4) The extreme bounds (X_H and X_L) for each of fault conditions are stored in an array.
(5) The CUT is tested at various test frequency and if the error magnitude lies within the corresponding predetermined limits, suitable signature is fed to the ANN classifier which does the fault classification.

The block diagram for the proposed approach is given in Figure 2.

4. PREPROCESSOR AND ANN CLASSIFIER

4.1. Preprocessor

Owing to the presence of noise, a complete fault dictionary containing all feasible conditions cannot obviously be generated. This problem is solved by giving inputs to the neural network in terms of bits—a "0" is assigned if the value observed for a specific test frequency is out of bounds; a "1" is assigned if the value observed for a specific test frequency is within bounds. that is, if $X_L \le X_m \le X_H$ implies ANN input = 1, else ANN input = 0.

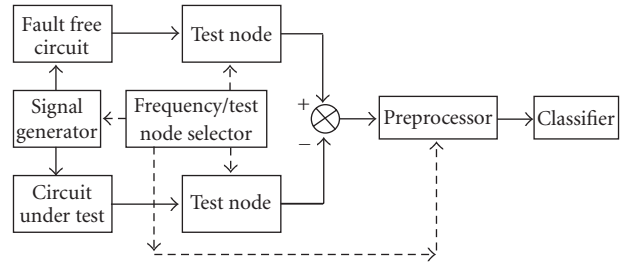

Figure 2: Block diagram of the proposed multiple fault diagnosis.

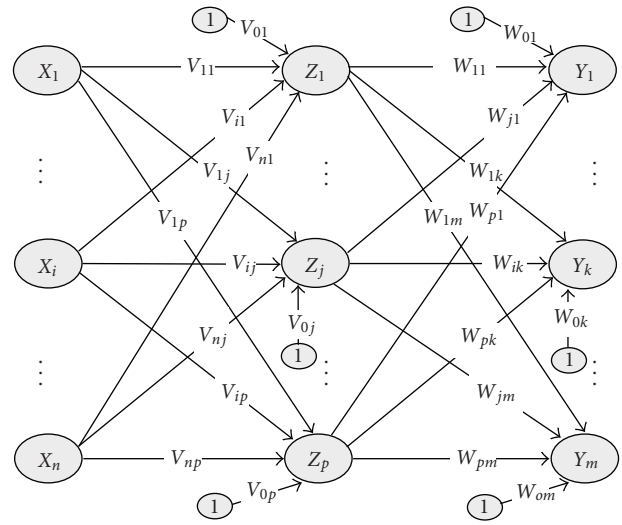

Figure 3: Two-layer BPN network topology.

4.2. Artificial neural network classifier

Artificial neural network can provide an adaptive mechanism for the pattern classification [9]. They are capable of robust classification in following environments: ill-defined model, noisy input environments, and nonlinearity. In this paper, the back propagation network (BPN) structure [10] provides best results for the classification task. A comparison of five network architectures is outlined in [11]. Many other works have also had success using the BPN network. Examples include classification of sonar targets [12], speech recognition [13], and sensor interpretation [14]. Recent successes have applied ANNs to process fault detection in chemical processes [15]. Direct applications of ANNs for fault diagnosis can be found in [16–18]. Typical BPN have two or three layers of interconnecting weights. Figure 3 shows a standard two-layer BPN network topology. Each input node is connected to a hidden layer node. Each hidden node is connected

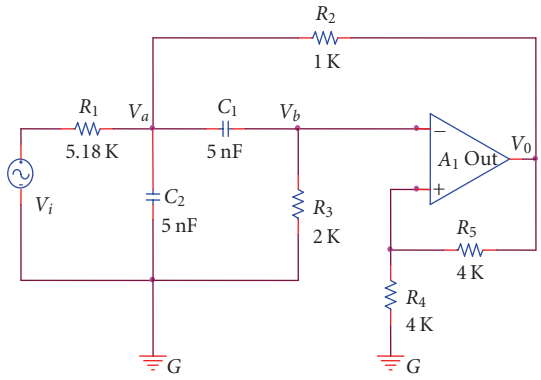

FIGURE 4: Sallen-key bandpass filter circuit.

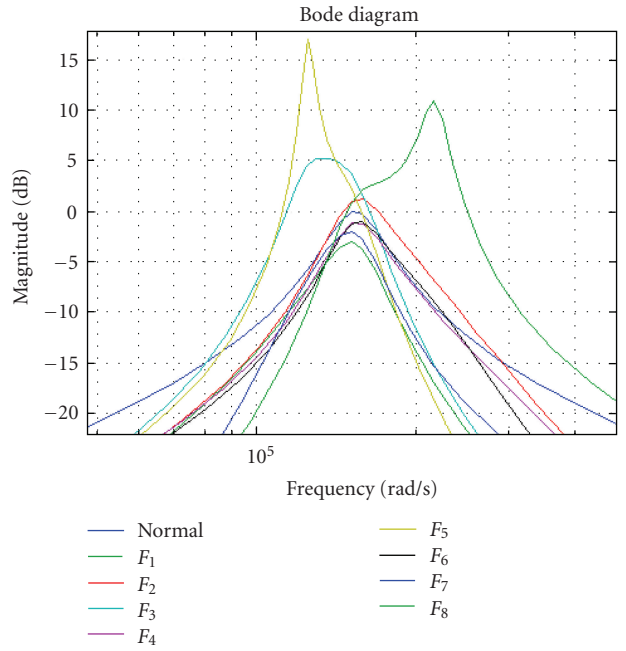

FIGURE 5: Response of the single components faults at the output node.

to an output node in a similar fashion .This makes BPN a fully connected network topology.

Here, $X_1 \cdots X_i \cdots X_n$ indicates the input neurons of artificial neural network, $Z_1 \cdots Z_j \cdots Z_p$ the hidden layer neurons of artificial neural network, $Y_1 \cdots Y_k \cdots Y_m$ the output neurons of artificial neural network, V_{ij} weight from ith input neuron to jth hidden neuron, W_{jk} weight from jth hidden neuron to kth output neuron, V_{0j} weight from bias to jth hidden neuron, W_{0k} weight from bias to kth output neuron.

The supervised learning in BPN takes place by propagating the node activation function of input pattern to output nodes. These outputs are compared with the desired target values, and an error signal (δ) is produced. The network weights are adapted so as to minimize the error. The generalized delta rule does the weight adaptation given by $\Delta_p\omega_{ij} = \epsilon\delta_{pj}x_{pi}$, where ϵ is the learning rate, δ_{pj} is the error at the jth node due to pattern p, x_{pi} is the ith element of the output pattern p. The error signal for the output node is $\delta_{pj} = (t_{pj} - o_{pj})\, f_j(\text{net}_{pj})$, where t_{pj} and o_{pj} are target and output values, respectively. The number of nodes in a layer and the activation function will affect the learning rate, the computational complexity, and the usefulness of the network for a specific problem wherein the best results always come from intuition and experience.

5. SIMULATION RESULTS

The feasibility of this method is validated through two benchmark circuits. The first circuit considered is a standard Sallen key bandpass filter circuit and the second circuit considered is a standard state variable filter circuit. Both single as well as multiple component fault scenarios are applied to this circuit and the results obtained are graphically plotted.

5.1. *Sallen key bandpass filter circuit*

The circuit shown in Figure 4 is the Sallen Key bandpass filter circuit [3, 6] with the component values correspond to a nominal center frequency of 25 kHz. Each resistor has a tolerance of 5% and capacitor has a tolerance of 10%.

The transfer function of the Sallen-key bandpass filter circuit is

$$G(s) = \frac{sA_0G_1C_1}{s^2C_1C_2 + s(G_3C_1 + G_3C_2 + G_1C_1 + C_1G_2[1-A_0]) + G_3(G_1+G_2)}, \quad (1)$$

where $A_0 = 1 + (R_5/R_4)$, $G_1 = (R_1)^{-1}$, $G_2 = (R_2)^{-1}$, $G_3 = (R_3)^{-1}$, $Y_1 = sC_1$, and $Y_2 = sC_2$.

To study the testability of the circuit, the frequency response is plotted for various fault conditions. We consider the case of only one test point, that is, the output node. The sensitivity of the output signal with respect to single and multiple faults along with the frequency response of the nominal circuit is given in Figure 5.

The test frequency for the single faults of the filter circuit is obtained by incrementing the faulty component at ±50% and obtaining the frequency response of the circuit. In the process, all the other components are kept at their nominal values. The test frequency for each of the fault conditions is given in Table 1. There are totally $2n$ single faults where n is the nunber of components in the circuit for which the sensitivity analysis is done.

For multiple faults, there are $n\,(n-1)/2$ double faults, $n\,(n-1)/3$ triple faults, and $n\,(n-1)/4$ of quadruple faults. Totally 11 fault conditions are analyzed. The fault component value is 50% higher than the nominal values. These faults are observed at the output node by plotting the frequency response. The frequency response of the Sallen Key bandpass filter under multiple faults is shown in Figure 6. The test results are shown in Table 2. The fault free case is given the ID number F_{20}.

Table 1: Test frequencies of the single faults for test circuit.

Fault ID	Fault components	Test frequency in KHz	Error magnitude in volts
F_1	$R_2 + 50\%$	24.1915	0.7052
F_2	$R_2 - 50\%$	24.5099	1.1475
F_3	$R_3 + 50\%$	21.0084	1.8339
F_4	$R_3 - 50\%$	24.1915	0.8744
F_5	$C_1 + 50\%$	20.0535	7.0309
F_6	$C_1 - 50\%$	26.7380	0.7973
F_7	$C_2 + 50\%$	24.1915	0.7945
F_8	$C_2 - 50\%$	34.5366	3.53

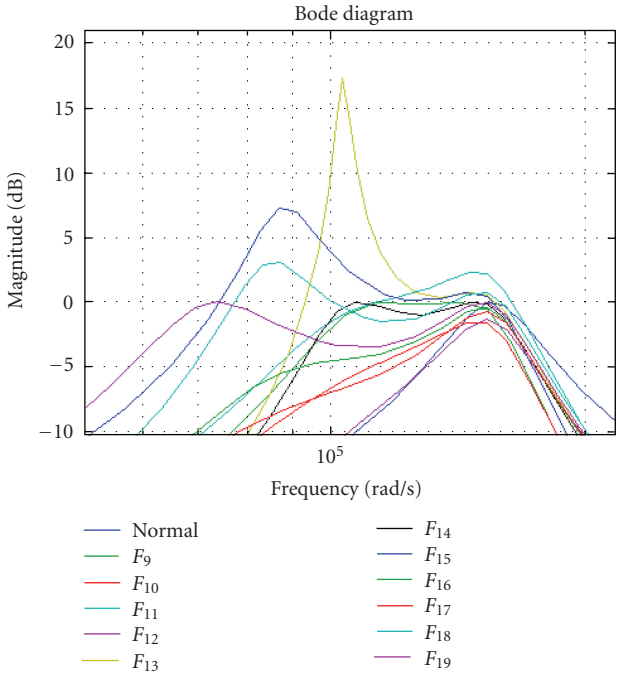

Figure 6: Response of the multiple faults at the output node.

Table 2: Test frequencies for the multiple faults for test circuit.

Fault ID	Fault components	Test frequency in KHz	Error magnitude in volts
F_9	R_2, R_3	17.9845	0.9813
F_{10}	C_1, R_2	24.1915	0.8317
F_{11}	C_1, R_3	23.0774	1.2969
F_{12}	C_2, R_2	24.5099	0.8554
F_{13}	C_2, R_3	16.3929	7.2424
F_{14}	C_1, C_2	16.8704	0.9963
F_{15}	R_2, R_3, C_1	13.5282	2.1735
F_{16}	R_2, R_3, C_2	20.0535	0.7052
F_{17}	C_1, C_2, R_2	20.0535	0.6316
F_{18}	C_1, C_2, R_3	13.5282	1.4374
F_{19}	R_2, R_3, C_1, C_2	13.5282	0.8379
F_{20}	Fault Free	24.5099	—

Table 3: Fault bounds.

Fault ID	Lower limits (X_L)	Upper limits (X_H)
F_1	0.54	0.77
F_2	1.1	1.5
F_3	1.5	2.1
F_4	0.82	0.89
F_5	6.1	7.8
F_6	0.75	0.83
F_7	0.77	0.8
F_8	2.9	4.1
F_9	0.95	1.5
F_{10}	0.81	0.88
F_{11}	1.21	2
F_{12}	0.8	0.87
F_{13}	6.1	7.4
F_{14}	0.89	1.2
F_{15}	1.9	2.9
F_{16}	0.65	0.99
F_{17}	0.59	0.79
F_{18}	1.2	1.8
F_{19}	0.89	1.2
F_{20}	0.80	1.2

5.1.1. *Obtaining the fault bounds for the various faults*

To obtain the fault bounds for R_2 (fault ID-F_1 case), the test frequency is set to 24.1915 kHz. The resistor R_2 is incremented by 50% and other components R_3 and C_1, C_2 are kept at −5% and −10% tolerant values, respectively. The sensitivity, $S(R_2)$, which is the error in magnitude between fault-free circuit output and faulty circuit output, is determined. This number serves as the lower limit (X_L) of the fault. A similar approach is carried out for calculating the upper limit (X_H) on the sensitivity value by keeping R_3 at +5% and C_1, C_2 at +10%. The above procedure is repeated for all fault conditions at the appropriate test frequencies. The limits are stored in an array which is given in Table 3.

5.1.2. *Pattern classifier*

Since the test pattern for the Sallen Key bandpass filter circuit has 20 inputs (19 faults plus 1 fault-free condition), the ANN has 20 neurons in the input layer and 5 neurons in the output layer. The 5 neurons in the output layer can classify a total of 32 faults (2^5) and will be sufficient for classifying 19 plus 1 possible condition in our work. The number of neurons in the hidden single layer is 12. So the ANN structure boils down to 20 : 12 : 5.

For all faults F_1 through F_{20}, the corresponding subscripts (1 through 20) indicate the fault IDs. The pattern for a specific fault is generated by testing the CUT at all test frequencies under permissible tolerances for other network components. The ANN is adaptively trained to update the weights and the bias by gradient descent method by the mean-square-error performance.

Table 4: Few random tested patterns of the classifier.

Component value (R_i in "Kohm", C_i in nF)				Classifier input (equivalent decimal value)	Classifier output (equivalent decimal value)	Fault ID
R_2	R_3	C_1	C_2			
1	3	5	7.5	2176	13	F_{13}
1.5	3	5	5	2128	9	F_9
1.5	2	7.5	5	66840	10	F_{10}
1	3	7.5	7.5	16468	18	F_{18}
1	2	7.5	7.5	80	14	F_{14}

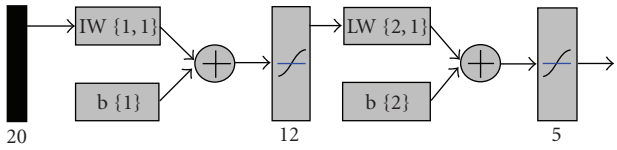

Figure 7: Classifier for test circuit.

The classifier structure for the circuit and the training pattern for 100 epochs are shown in Figures 7 and 8, respectively. In the classifier for test circuit, the first block indicates the input layer comprising 20 neurons, the centre block indicates the hidden layer comprising 12 neurons, and the last block indicating the output layer comprising 5 neurons, respectively. The blocks in between the input layer and the middle layer indicate the weight factor (IW $\{1, 1\}$) associated with input node, and bias input (b $\{1\}$) acts on a neuron like an offset. The blocks in between the middle layer and the output layer indicate the weight factor (LW $\{2, 1\}$) associated with hidden layer, and bias input (b $\{2\}$) acts on a neuron like an offset.

For few randomly generated test patterns for the filter circuit, classifier results are shown in Table 4. The results agree well within the corresponding fault ID.

As a case study, for fault F_{13}, X_9, and X_{13} carry a logical 1 whereas all the remaining neurons carry a binary 0. This means that the analog circuit when tested for all frequencies produce output voltage lying within the permissible limits only for the test frequencies 17.9845 KHz and 16.3929 KHz, respectively—this corresponds 2176_{10}. The output of ANN for this condition has a high logical in Y_2, Y_3, and Y_5 remaining output neurons have low logical in Y_1 and Y_4. This bit combination corresponds to 13_{10} signifying F_{13} condition. Similarly, we deduce ANN classifier inputs and outputs for all fault cases. A few more test cases, namely, F_9 and F_{10} along with F_{13}, is detailed in Table 5.

5.2. State variable filter circuit

The circuit shown in Figure 9 is the state variable filter circuit [19] with the component values corresponding to a nominal center frequency of 25 kHz. Each resistor has a tolerance of 5% and each capacitor has a tolerance of 10%.

The transfer function of the state variable filter circuit is

$$\frac{V_{LP}}{V_i} = \frac{R_3(R_1 + R_6)}{s^2(R_1R_4R_5C_1C_2[R_2 + R_3]) - R_1R_2 + R_3R_6}. \quad (2)$$

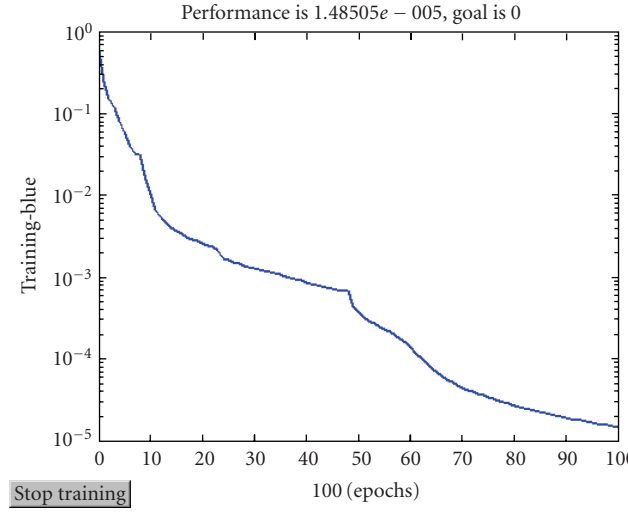

Figure 8: Performance plot for the classifier.

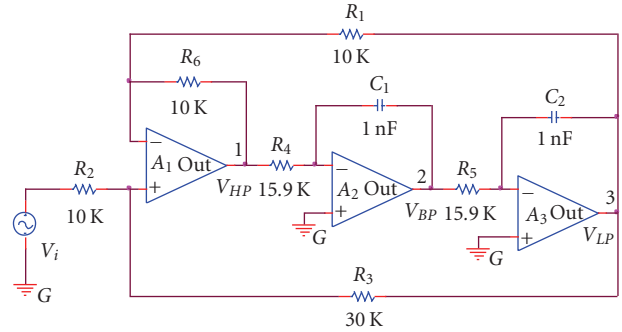

Figure 9: State variable filter circuit.

To study the testability of the circuit, the frequency response is plotted for various fault conditions. We consider the case of three test points. The sensitivity of the output signal with respect to single faults along with the frequency response of the nominal circuit is given in Figure 10.

The test frequency for the single faults of the filter circuit is obtained by incrementing the faulty component at ±50% and obtaining the frequency response of the circuit. In the process, all the other components are kept at their nominal values. The test frequency for each of the fault conditions is given in Table 6. There are totally $2n$ single faults where n is the number of components in the circuit for which the sensitivity analysis is done.

Table 5: ANN inputs and outputs for test cases F_{13}, F_9, and F_{10}.

	Fault ID F_{13}		Fault ID F_9		Fault ID F_{10}	
Testing frequency (in KHz)	Error magnitude (volts)	Input NN	Error magnitude (volts)	input NN	Error magnitude (volts)	Input NN
24.1915	1.0651	0	0.9432	0	0.8317	0
24.5099	0.9634	0	0.8235	0	0.7511	0
21.0084	1.0436	0	0.9813	0	0.7283	0
24.1915	1.0651	0	0.9432	0	0.8317	1
20.0535	1.0778	0	0.9821	0	0.6755	0
26.7380	0.7143	0	0.5724	0	0.5463	0
24.1915	1.0651	0	0.9432	0	0.8317	0
34.5366	0.2003	0	0.1149	0	0.1252	0
17.9845	1.0436	1	0.9813	1	0.7283	0
24.1915	1.0651	0	0.9432	0	0.8317	1
23.0774	1.0881	0	0.9982	0	0.8388	0
24.5099	1.0394	0	0.9100	0	0.8121	1
16.3929	7.2424	1	0.8761	0	0.4957	0
16.8704	3.9331	0	0.9327	1	0.5211	0
13.5282	0.5823	0	0.5077	0	0.3579	0
20.0535	1.0778	0	0.9821	1	0.6755	1
20.0535	1.0778	0	0.9821	0	0.6755	1
13.5282	0.4906	0	0.4668	0	0.3398	0
13.5282	0.2114	0	0.2804	0	0.2381	0
24.5099	0.7574	0	0.4366	0	0.3599	0
Equivalent decimal value		2176		2128		66840
Output of NN		$Y_1Y_2Y_3Y_4Y_5$ 0 1 1 0 1		$Y_1Y_2Y_3Y_4Y_5$ 0 1 0 0 1		$Y_1Y_2Y_3Y_4Y_5$ 0 1 0 1 0
Equivalent decimal value		13		9		10

Table 6: Test frequencies of the single faults (dashes mean no access to nodes).

Fault ID	Fault components	At node-1 Test frequency in KHz	At node-2 Test frequency in KHz	At node-3 Test frequency in KHz
1	$R_1 + 50\%$	4.9975	4.9975	4.9975
2	$R_1 - 50\%$	7.0824	7.0824	7.0824
3	$R_2 + 50\%$	—	—	5.7773
4	$R_2 - 50\%$	8.4670	8.4670	8.4670
5	$R_3 + 50\%$	7.9896	—	7.9896
6	$R_3 - 50\%$	4.4722	4.4722	4.4722
7	$R_5 - 50\%$	—	—	9.9790
8	$R_6 + 50\%$	9.3583	9.3583	—
9	$R_6 - 50\%$	3.5332	3.5332	3.5332
10	$C_1 + 50\%$	—	7.1620	—
11	$C_2 + 50\%$	7.0824	—	—
12	$C_2 - 50\%$	—	10.0108	—

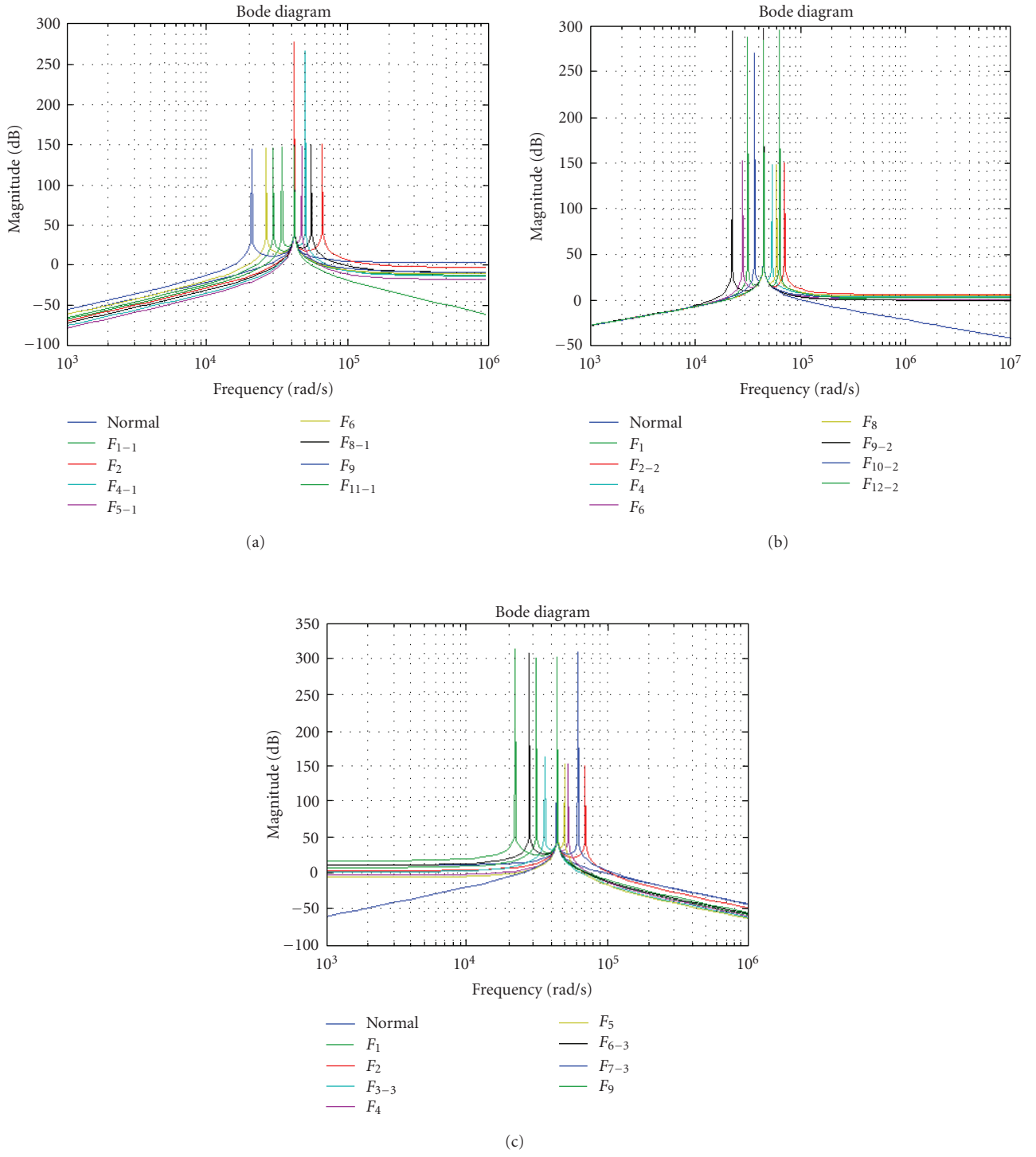

FIGURE 10: Response of the single faults (a) at node 1, (b) at node 2, and (c) at node 3.

For multiple faults, there are $n\ (n-1)/2$ double faults, $n\ (n-1)/3$ triple faults, and $n\ (n-1)/4$ of quadruple faults. Totally 28 fault conditions are analyzed among which only 13 faults are observable. The fault component value is 50% higher than the nominal values. These faults are observed at the output node by plotting the frequency response. The frequency response of the state variable filter under multiple faults is shown in Figure 11. The test results are shown in Table 7.

5.2.1. *Obtaining the fault bounds for the various faults*

To obtain the fault bounds for R_2 (fault ID-1 case), the test frequency is set to 24.1915 KHz. The resistor R_2 is

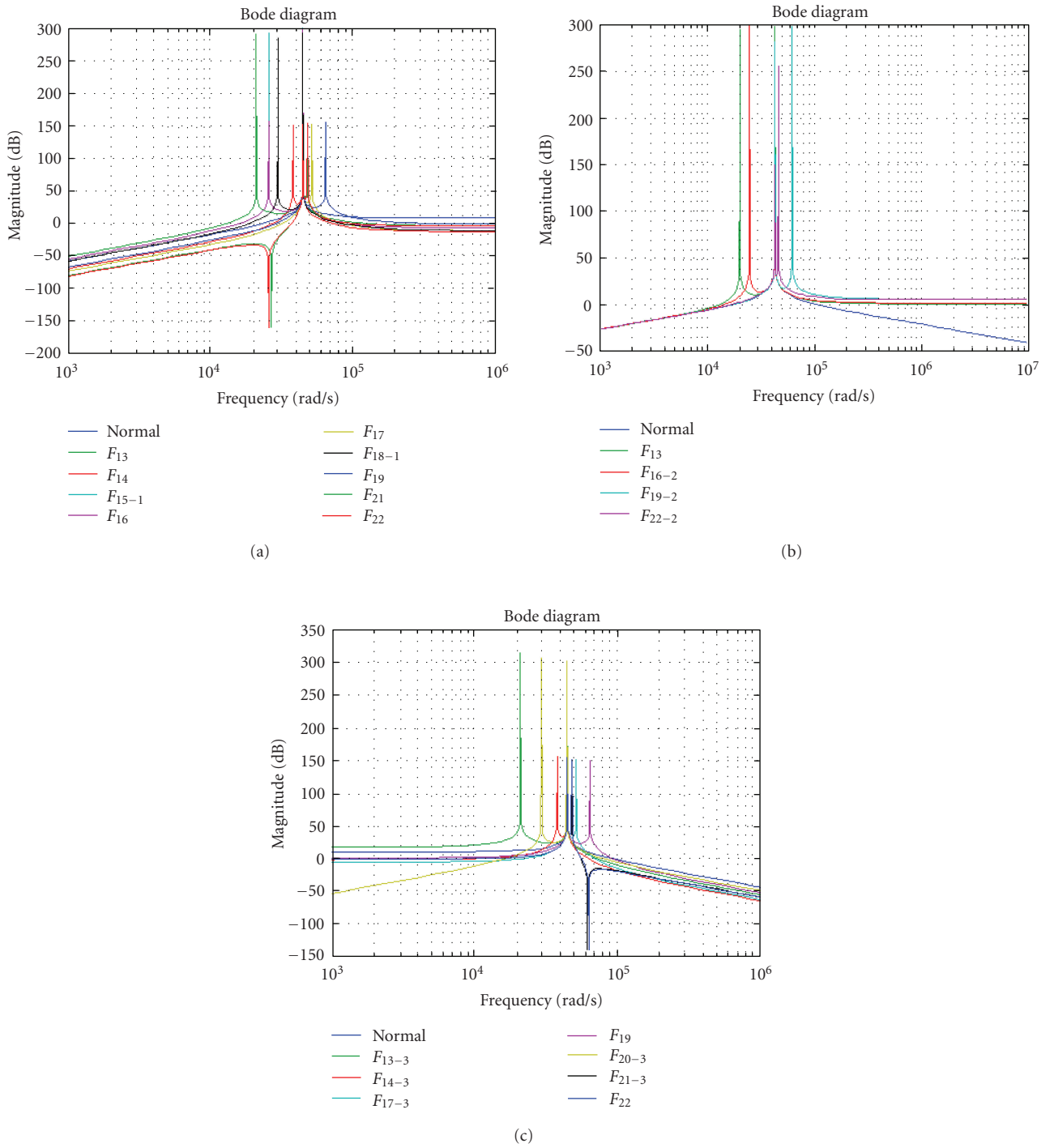

FIGURE 11: Response of the multiple faults at (a) node 1, (b) node 2, (c) node 3.

incremented by 50% and other components R_3 and C_1, C_2 are kept at −5% and −10% tolerant values, respectively. The sensitivity, $S(R_2)$, which is the error in magnitude between fault-free circuit output and faulty circuit output is determined. This number serves as the lower limit (X_L) of the fault. A similar approach is carried out for calculating the upper limit (X_H) on the sensitivity value by keeping R_3 at +5% and C_1, C_2 at +10%. The above procedure is repeated for all fault conditions at the appropriate test frequencies. The limits are stored in an array which is given in Table 8.

5.2.2. *Pattern classifier*

Since the test pattern for the state variable filter circuit has 23 inputs. The ANN has 23 neurons in the input layer and 5 neurons in the output layer. The 5 neurons in the output layer

Table 7: Test frequencies of the multiple faults (dashes mean no access to nodes).

Fault ID	Fault components	At node-1 Test frequency in KHz	At node-2 Test frequency in KHz	At node-3 Test frequency in KHz
13	R_1R_2	3.3422	3.3422	3.3422
14	R_1R_3	6.0320	—	6.0320
15	R_1C_1	4.0903	—	—
16	R_1C_2	7.0824	6.0320	—
17	R_2R_6	8.1806	—	8.1806
18	R_2C_2	4.7110	—	—
19	R_3R_6	10.2337	10.2337	10.2337
20	R_4R_5	—	—	4.6951
21	R_5R_6	4.2653	—	9.8358
22	R_6C_2	6.0320	7.6394	10.0108

Table 8: Fault bounds.

Fault ID	Lower limits (X_L)	Upper limits (X_H)
1	74.9	76
2	21	23
3	7.81	7.83
4	220	222
5	198.1	199
6	3.8	3.84
7	4.2	4.3
8	256.5	258
9	5.4	5.8
10	102.5	104
11	141	144
12	12	13
13	2.6	2.7
14	9.7	9.8
15	74	75
16	9	11
17	9	10.1
18	94.5	96
19	21	21.9
20	4.15	4.25
21	4.3	4.4
22	33	34.4
23	13	14

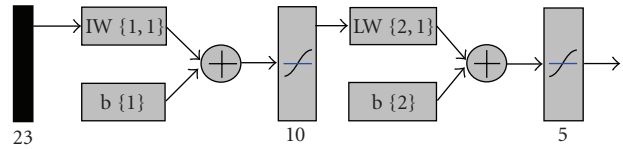

Figure 12: Pattern classifier.

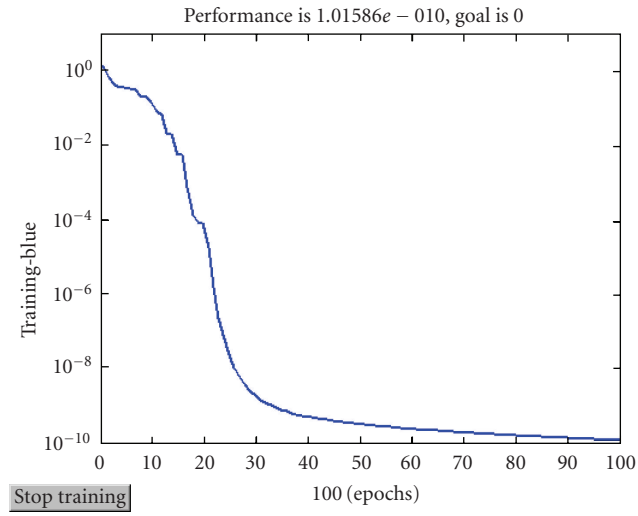

Figure 13: Training performance plot for the classifier.

can classify a total of 32 faults (2^5) and will be sufficient for classifying all condition in our work. The number of neurons in the hidden single layer is 10. So the ANN structure boils down to 23 : 10 : 5.

The pattern for a specific fault is generated by testing the CUT at all test frequencies under permissible tolerances for other network components. The ANN is adaptively trained to update the weights and the bias by gradient descent method by the mean-square-error performance.

The classifier structure for the circuit and the training pattern for 100 epochs are shown in Figures 12 and 13, respectively. In the classifier for test circuit, the first block indicates the input layer comprising 23 neurons, the centre block indicates the middle layer comprising 10 neurons and the last block indicating the output layer comprising 5 neurons, respectively. The blocks in between the input layer and the middle layer indicate the weight factor (IW $\{1,1\}$) associated with input node, and bias input (b $\{1\}$) acts on a neuron like an offset. The blocks in between the middle layer and the output layer indicate the weight factor (LW $\{2,1\}$) associated with middle layer, and bias input (b $\{2\}$) acts on a neuron like an offset.

For few randomly generated test patterns for the filter circuit, classifier results are shown in Table 9. The results agree well within the corresponding fault ID.

Table 9: Few tested patterns.

Components value (R_i in "Kohm", C_i in "nF")								Classifier input	Classifier output	Fault ID
R_1	R_2	R_3	R_4	R_5	R_6	C_1	C_2			
15	10	30	15.9	15.9	10	1.5	1	1536	15	15
10	15	30	15.9	15.9	10	1	1	1057289	3	3
10	10	30	15.9	15.9	15	1	1.5	68	21	21
10	10	45	15.9	23.9	15	1	1	8276	19	19
10	10	30	24	24	10	1	1	65672	20	20
10	10	30	15.9	15.9	10	1	0.5	67592	12	12

Table 10: ANN inputs and outputs for test cases F_{15}, F_3, and F_{21}.

	Fault ID F_{15}		Fault ID F_3		Fault ID F_{21}	
Testing frequency (in KHz)	Error magnitude (volts)	Input NN	Error magnitude (volts)	input NN	Error magnitude (volts)	Input NN
4.9975	113.93	0	71.149	0	102.01	0
7.0824	28.606	0	25.578	0	33.831	0
5.7773	7.7493	0	7.8241	1	7.8868	0
8.4670	366.1	0	226.1	0	313.01	0
7.9896	323.72	0	201.88	0	279.55	0
4.4722	3.7833	0	3.8479	0	3.9028	0
9.9790	4.4436	0	4.3054	0	4.198	0
9.3583	458.56	0	279.3	0	384.56	0
3.5332	5.2948	0	4.9621	0	7.7213	0
7.1620	104.45	0	103.43	1	108.95	0
7.0824	153.58	0	95.092	0	136.22	0
10.0108	25.392	0	23.183	0	30.699	0
3.3422	2.6689	1	2.7273	0	2.7773	0
6.0320	9.7138	1	9.791	1	9.8554	0
4.0903	75.458	0	47.425	0	68.153	0
4.0903	5.9792	0	5.5744	0	8.7647	0
8.1806	10.252	0	10.148	0	10.064	1
4.7110	100.87	0	63.139	0	90.589	0
10.2337	25.917	0	23.571	0	31.233	0
4.6951	4.1425	0	4.2087	1	4.2647	0
9.8358	4.6204	0	4.4854	0	4.3801	1
7.6394	29.627	0	28.463	0	34.33	1
7.0824	14.377	0	13.379	1	18.838	0
Equivalent decimal value		1536		1057289		70
Output of NN		$Y_1Y_2Y_3Y_4Y_5$ 0 1 1 1 1		$Y_1Y_2Y_3Y_4Y_5$ 0 0 0 1 1		$Y_1Y_2Y_3Y_4Y_5$ 1 0 1 1 0
Equivalent decimal		15		3		22

As a case study, faults F_{13}, X_{13}, and X_{14} carry a logical 1 whereas all the remaining neurons carry a binary 0. This means that the analog circuit when tested for all frequencies produce output voltage lying within the permissible limits only for the test frequencies 3.3422 KHz and 6.0320 KHz, respectively—this corresponds 1536_{10}. The output of ANN for this condition has a high logical in Y_2, Y_3, Y_4, and Y_5, remaining output neurons have low logical in Y_1. This bit combination corresponds to 15_{10} signifying F_{15} condition. Similarly we deduce ANN classifier inputs and outputs for all fault cases. A few more test cases, namely, F_3 and F_{21} along with F_{15}, is detailed in Table 10.

6. RESULT AND DISCUSSION

In this section, a comparison is made with the size and performance of the proposed neural network to show the significance of the technique. To perform a diagnosis of the faults

described in Section 5.1, for the Sallen Key bandpass filter circuit, the work presented in [6] requires a three-layer back propagation neural network. This network has 49 inputs, 10 first layers, and 10 second layers (49 : 10 : 10). Their trained network was able to classify only single faults. The work presented in [3] requires three-layer back propagation network with 5 inputs, 5 neurons in layer 1, and 1 neuron in the output layer (5 : 5 : 1). The trained network was able to classify only 8 single faults. The proposed neural network structure has 20 inputs, 12 first layers, and 5 second layers (5 : 12 : 15), and can classify 8 single faults and 11 multiple faults. The real advantage of preprocessing becomes evident when applied to more complex state variable filter circuit shown in Section 5.2. The work presented in [19] can classify 17 single fault scenarios including the fault-free condition. The proposed method can classify 23 fault scenarios, consists of 12 single faults, 10 multiple faults, and 1 fault-free condition.

The results of proposed method clearly indicate that through appropriate preprocessing of an analog circuit output, one can train a neural network to correctly diagnose all faults unless the circuit's outputs are similar for some fault cases. This study indicates that the proposed preprocessing techniques have a significant impact on analog fault diagnosis due to the selection of an optimal number of relevant features. This leads to neural network architecture with minimum size that can be trained and carry out fault diagnosis with a high degree of accuracy. The main contribution of this work is the formulation and solving of fault diagnosis problem completely in frequency domain. This work is novel in the sense that the classical frequency domain concepts and nonmathematical neural networks are brought together on a unified platform of fault diagnosis. Currently, one limitation of this approach is the amount of simulation-before-test (SBT) process which must take place before. The method does not guarantee that in every case the faulty components will be identified. Some times the set of possibly faulty elements obtained by the method is larger than the really faulty elements. This can especially occur if ambiguity groups appear. Hence in general, the method gives correct results and works effectively as illustrated via numerical examples.

7. CONCLUSION

A frequency response approach for analog electronic circuit testability analysis is proposed in this paper. By performing the frequency response test of the CUT under faulty and nonfaulty conditions, test frequency for every category of faults is selected. Using suitable decision making preprocessor, the corresponding faulty signature is fed into the ANN which does the fault classification. The result of the proposed method applied to the Sallen key bandpass filter circuit and state variable filter circuit is quite encouraging.

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