

## Research Article

# Electronically Tunable Sinusoidal Oscillator Circuit

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Received 29 March 2012; Accepted 4 June 2012

Academic Editor: Winai Jaikla

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This paper presents a novel electronically tunable third-order sinusoidal oscillator synthesized from a simple topology, employing current-mode blocks. The circuit is realized using the active element: Current Controlled Conveyors (CCCIIs) and grounded passive components. The new circuit enjoys the advantages of noninteractive electronically tunable frequency of oscillation, use of grounded passive components, and the simultaneous availability of three sinusoidal voltage outputs. Bias current generation scheme is given for the active elements used. The circuit exhibits good high frequency performance. Nonideal and parasitic study has also been carried out. Wide range frequency tuning is shown with the bias current. The proposed theory is verified through extensive PSPICE simulations using 0.25  $\mu\text{m}$  CMOS process parameters.

## 1. Introduction

The sinusoidal oscillators constitute an important building block which finds numerous applications in analogue signal processing. This electronic function provides standard test and carrier signals for communication and instrumentation circuits and also acts as the starting signal for generation of several other types of test signals. Similarly, the multiphase oscillators also find interesting applications in communication and instrumentation systems. For these highly precise processes, third-order sinusoidal oscillators are best suited because they enjoy lower harmonic distortions as compared to the second-order sinusoidal oscillators [1].

When the repertoire of technical literature is surveyed, many oscillator circuits are available based on one or the other type of active devices [2–4], but the third-order oscillators are not available in profusion. The third-order oscillators were first proposed in [5] using operational transconductance amplifiers (OTAs), but the dynamic range of the circuits based on OTAs is very limited [6]. Also, the frequency of oscillation cannot be controlled without affecting the condition of oscillation. The reported third-order oscillator in [7] provided four quadrature current outputs, all at high impedance, which makes it suitable for current-mode

analogue signal processing. Two current-mode third-order sinusoidal oscillators are proposed in [8] which require three OTAs and three grounded capacitances. In the second oscillators circuit, the frequency of oscillation cannot be controlled without affecting the condition of oscillation. Also, for a large variation in the bias current, it gives a relatively less variation in the frequency of oscillation. The circuit proposed in [9] has limited upper frequency because of external resistor termination at X-terminals, which when reduced would increase the frequency errors due to the parasitic X-resistance becoming appreciable in comparison with the external ones. The circuit proposed in [10] provided two quadrature current outputs and required fewer components. The third-order oscillator proposed in [11] provided four quadrature voltage outputs but it required three floating resistors. The reported circuit in [12] uses CMOS CCCII and grounded capacitors, provides both quadrature current as well as voltage outputs, and also enjoys electronic tunability. Lastly, the quadrature oscillator reported in [13] requires three CDTAs and three grounded capacitors. This quadrature oscillator, despite being third-order, imparts very high THD values. One work based on two multioutput DVCCs and two grounded capacitors provide high impedance current outputs, but falls in second

TABLE 1: Transistor aspect ratios of CMOS CCCII.

Transistors	$W$ ( $\mu\text{m}$ )	$L$ ( $\mu\text{m}$ )
$M_5, M_9$	10	0.5
$M_6, M_{10}$	16	0.5
All other NMOS	6	0.5
All other PMOS	10	0.5

order category [14]. Recently, novel oscillator circuit for voltage outputs using new active element (DO-CIBA) and grounded capacitors has been reported, which also requires a number of floating resistors [15]. Another very novel work reported multiphase oscillator circuit operating in current mode and was based on log-domain approach [16].

In this paper, a third-order sinusoidal oscillator is synthesized from the simple topology employing cascaded first-order low-pass filters coupled with gained feedback. The active element used is CMOS Current Controlled Conveyors (CCCIs). The frequency of oscillation can be electronically tuned independently of the condition of oscillation. This circuit offers the advantages of the simultaneous availability of three sinusoidal voltage outputs and the use of grounded passive components which makes it suitable for IC implementation.

## 2. Proposed Circuit

The newly proposed third-order sinusoidal oscillator is based on the use of cascaded current-mode first order low pass filters coupled with gain block in feedback. The basic block diagram of this topology is shown in Figure 1. For the realization of the sinusoidal oscillator, the current-mode low pass filter is used and the value of “K” is taken to be negative; which can be realized using a current-mode inverting amplifier. The basic block diagram is shown in Figure 1. The basic blocks of Figure 1 are realized using CCCIs and grounded components. The CCCII was proposed in [17] and ever since its introduction, it has been used for the realization of numerous useful and high performance analogue circuits [17–21]. This device possesses the advantages of the electronic tunability through the parasitic resistance appearing at the terminal X, good dynamic range, and greater linearity. As far as the basic scheme of employing low-pass filters for multiphase oscillators is concerned, the same was first introduced and used for OTA-based realizations [22, 23]. The CMOS implementation of CCCII is shown in Figure 2 and the aspect ratios of all the MOS transistors used are listed in Table 1.

The CCCII is described by the following current and voltage relationships:

$$\begin{aligned} V_X &= V_Y + I_X R_X, \\ I_Y &= 0, \quad I_{Z+} = I_X, \quad I_{Z-} = -I_X. \end{aligned} \quad (1)$$

Here,

$$R_X \approx \frac{1}{\sqrt{8\mu C_{\text{ox}}(W/L)I_B}}, \quad (2)$$

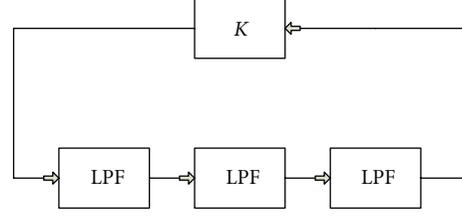


FIGURE 1: Block Diagram of the topology for third-order oscillator.

where  $\mu$ ,  $C_{\text{ox}}$ ,  $W$ , and  $L$  are, respectively, the surface mobility, oxide capacitance, channel width, and length of the transistors  $M_9$  and  $M_{10}$ , assuming that both transistors are matched.

The circuit diagram of the newly proposed third-order sinusoidal oscillator, based on the topology shown in Figure 1, is given in Figure 3. The circuit requires four CCCIs, three capacitors, and a resistor. On performing the routine analysis using the properties of CCCII defined in (1), the characteristic equation of the proposed third-order sinusoidal oscillator shown in Figure 3 is given by

$$as^3 + bs^2 + cs + d = 0, \quad (3)$$

where  $a = R_{X1}R_{X2}R_{X3}C_1C_2C_3$ ,  $b = R_{X1}R_{X2}C_1C_2 + R_{X1}R_{X3}C_1C_3 + R_{X2}R_{X3}C_2C_3$ ,  $c = R_{X1}C_1 + R_{X2}C_2 + R_{X3}C_3$ ,  $d = (R_1 + R_{X4})/R_{X4}$ .

One simple design is possible by assuming  $C_1 = C_2 = C_3 = C$  and  $R_{X1} = R_{X2} = R_{X3} = R_X$ , that is,  $I_{B1} = I_{B2} = I_{B3} = I_B$ . Substituting  $s = j\omega$ , and equating real and imaginary parts on the two sides of (3), we get the frequency and condition of oscillation a

$$\begin{aligned} \text{F.O. : } \omega_0 &= \frac{\sqrt{3}}{R_X C} \\ \text{C.O. : } R_1 &= 8R_{X4}. \end{aligned} \quad (4)$$

It is evident from (4) that  $\omega_0$  can be varied independent of the condition of oscillation by varying  $I_B$ . It may be noted that three current outputs can further be obtained by using additional Z+ stages in CCCII (1–3). Incorporation of Z– stages in each of these conveyors will further add to the three more outputs as their phase inverted version, so as to make six distinct current outputs. It is worth mentioning that the new proposed circuit differs from one CCCII-based work [21] which also presents a multiphase oscillator, by way of using grounded X terminals, contrary to the available work, where each X-terminal has capacitive terminations. It is a well-known fact that current conveyors-based circuits with capacitive terminations at X-port have limited frequency performance, which is also evident from [21], where maximum oscillation frequency is well below 1 MHz. The proposed work, in contrast, can provide signal frequencies in tens of MHz, as would be evident from the later sections.

## 3. Bias Current Generation

As evident from (4), the circuit requires frequency control through  $R_X$ , which in turn needs  $I_B$  control. In practice,

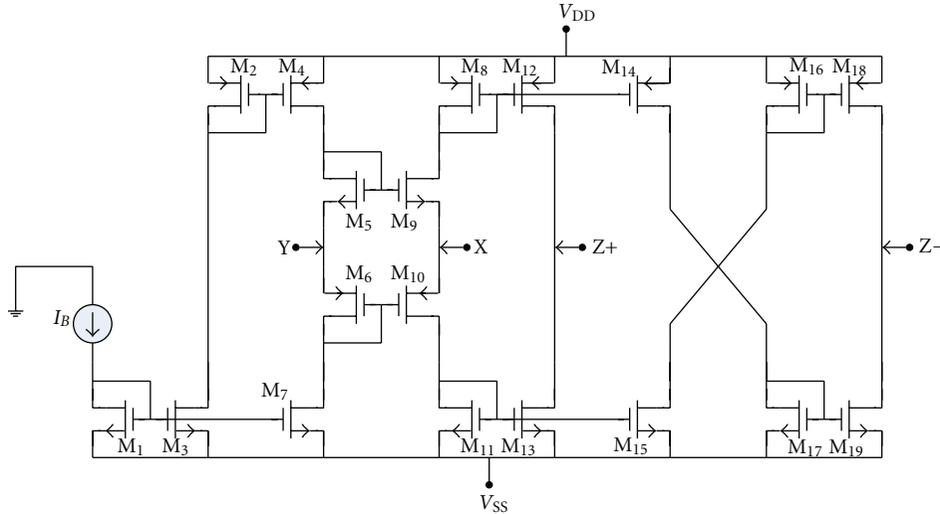


FIGURE 2: CMOS implementation of CCCII.

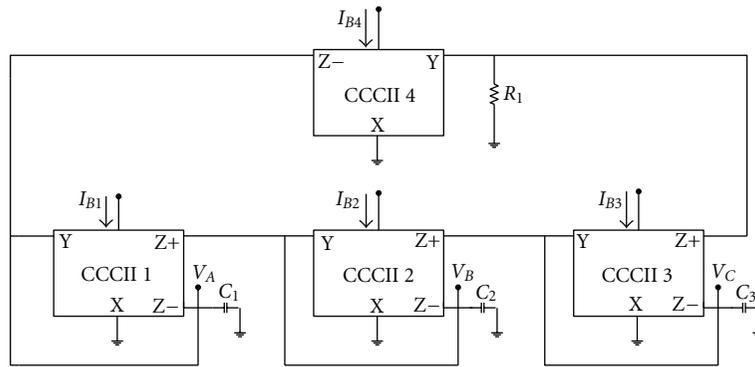


FIGURE 3: Third-order sinusoidal oscillator.

such an equal bias current for the three conveyors can be generated using the transistorized circuitry. The scheme for generation of same bias current  $I_B$  for CCCII (1–3) is shown in Figure 4. The bias current is mirrored through an NMOS current mirror and then three current sources are realized using the PMOS current mirror and steering transistors. It may be noted that the current mirror transistors use matched aspect ratio. The circuitry of Figure 4 allows the variation of frequency of oscillation through a single bias current.

#### 4. Nonideal Analysis

The performance of any current conveyor-based circuit may deviate from the ideal one due to nonidealities of the active elements. The non-ideal CCCII is described by the following current & voltage relationships:

$$\begin{aligned} V_X &= \beta_k V_Y + I_X R_X, \\ I_Y &= 0, \quad I_{Z+} = \alpha_k I_X, \quad I_{Z-} = -\alpha_k I_X, \end{aligned} \quad (5)$$

where  $\beta_k = 1 - \varepsilon_{V_k}$ ,  $\alpha_k = 1 - \varepsilon_{I_k}$ .

Here,  $\varepsilon_{V_k}$  ( $|\varepsilon_{V_k}| \ll 1$ ) and  $\varepsilon_{I_k}$  ( $|\varepsilon_{I_k}| \ll 1$ ) represent the voltage tracking error from Y-terminal to X-terminal and

current tracking error from X-terminal to Z-terminal of the  $k$ th CCCII, respectively. Generally, these tracking factors remain constant and frequency independent in low- to-medium frequency range. But, at higher frequencies, these tracking factors become frequency dependent.

On reanalyzing the circuit shown in Figure 3 using the nonideal equations of CCCII given in (5), the simplified expressions for frequency of oscillation (FO) and condition of oscillation (CO), assuming matched CCCIIs exhibiting same current and voltage transfer gains (denoted as  $\alpha$  and  $\beta$ , resp.) are given by

$$\text{F.O. : } f_o = \frac{\alpha\beta\sqrt{3}}{2\pi R_X C}, \quad \text{C.O. : } R_1 = \frac{8R_X^4}{\alpha\beta}. \quad (6)$$

Clearly, the frequency of oscillation is modified due to the nonidealities of CCCII, but as the values of  $\alpha$  and  $\beta$  remain close to unity till tens of MHz, the performance of the circuit is not severely affected. It is also worth mentioning that some frequency deviations would also be expected due to the current mirror transfer errors used in the bias current generation circuitry.

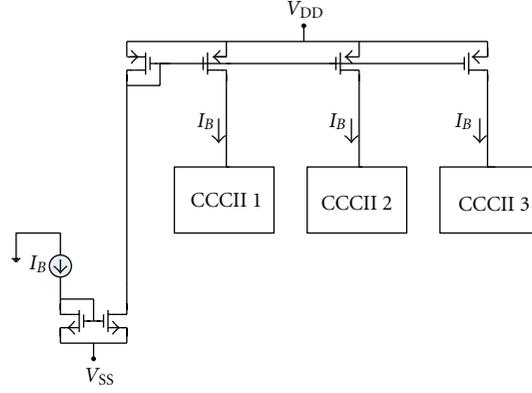


FIGURE 4: Bias current generation scheme for CCCII (1–3).

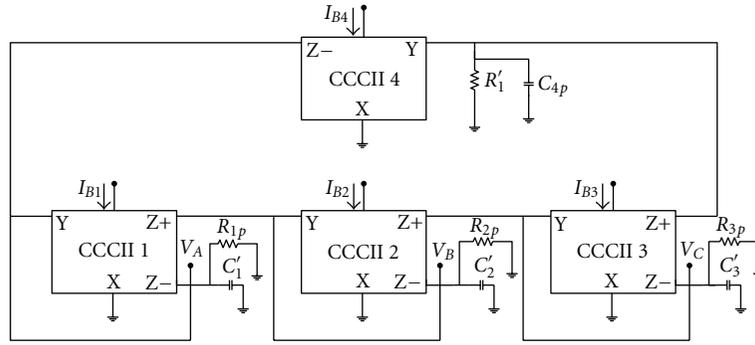


FIGURE 5: Third-order sinusoidal oscillator including parasitics.

## 5. Parasitic Study

The performance of any circuit is also affected due to the presence of various parasites at the terminals of the device. In the presence of the parasites of CCCII, the circuit given in Figure 3 modifies to Figure 5 where  $C'_1 = C_1 \parallel C_{y1} \parallel C_{z1} \parallel C_{z4}$ ,  $C'_2 = C_2 \parallel C_{y2} \parallel C_{z2} \parallel C_{z1}$ ,  $C'_3 = C_3 \parallel C_{y3} \parallel C_{z3} \parallel C_{z2}$ ,  $C_{4p} = C_{y4} \parallel C_{z3}$ ,  $R_{1p} = R_{y1} \parallel R_{z1} \parallel R_{z4}$ ,  $R_{2p} = R_{y2} \parallel R_{z2} \parallel R_{z1}$ ,  $R_{3p} = R_{y3} \parallel R_{z3} \parallel R_{z2}$ ,  $R'_{1p} = R_1 \parallel R_{y4} \parallel R_{z4}$ .

On analyzing the circuit shown in Figure 5 considering the parasites outlined above, the expression for the frequency of oscillation is as given below:

$$\text{F.O. : } \omega_0 = \sqrt{\frac{a + b + c}{C'_1 C'_2 C'_3 (R_{1p} R_{2p} R_{3p} R_{1p}' R_{X4} / R_{X3})}}, \quad (7)$$

$$\begin{aligned} \text{C.O. : } (a + b + c) & \left[ C'_1 C'_2 \left( \frac{R_{1p} R_{2p} R_{3p} R_{1p}' R_{X4}}{R_{X3}} \right) \right. \\ & + C'_1 C'_3 \left\{ \left( \frac{R_{1p} R_{3p} R_{1p}' R_{X4}}{R_{X3}} \right) \left( 1 + \frac{R_{1p}}{R_{X1}} \right) \right\} \\ & \left. + C'_2 C'_3 \left\{ \left( \frac{R_{2p} R_{3p} R_{1p}' R_{X4}}{R_{X3}} \right) \left( 1 + \frac{R_{2p}}{R_{X2}} \right) \right\} \right] \end{aligned}$$

$$\begin{aligned} & = \left\{ C'_1 C'_2 C'_3 \left( \frac{R_{1p} R_{2p} R_{3p} R_{1p}' R_{X4}}{R_{X3}} \right) \right\} \\ & \times \left[ \left( \frac{R_{1p}' R_{3p} R_{X4}}{R_{X3}} \right) \left\{ 1 + \left( \frac{R_{2p}}{R_{X2}} \right) + \left( \frac{R_{1p} R_{2p}}{R_{X1} R_{X2}} \right) \right\}, \right. \\ & \left. + \left( \frac{R_{1p} R_{2p} R_{3p}}{R_{X1} R_{X2} R_{X3}} \right) \right], \quad (8) \end{aligned}$$

where  $a = C'_1 \{ (R_{1p} R_{3p} R_{1p}' R_{X4} / R_{X3}) (1 + R_{1p} / R_{X1}) \}$ ,  $b = C'_1 \{ (R_{2p} R_{3p} R_{1p}' R_{X4} / R_{X3}) (1 + R_{2p} / R_{X2}) \}$ ,  $c = C'_3 \{ (R_{3p} R_{1p}' R_{X4} / R_{X3}) \{ 1 + (R_{1p} / R_{X1}) + (R_{1p} R_{2p} / R_{X1} R_{X2}) \} \}$

It may be clarified here, that the above defined variables are not the same as used in Section 2.

It is apparent from this analysis that despite including the effect of parasitics, the order of the characteristic equation of the oscillator has not changed. This is due to the fact that the X-terminal of all the CCCII is grounded. This leads to the interpretation that the higher order distortions are not introduced in the circuit within the desired frequencies of operation. This is an additional advantage of this circuit. A careful investigation of (7) reveals that the effects of various parasites can be compensated by selecting little deviated values of the input bias currents from their calculated values.

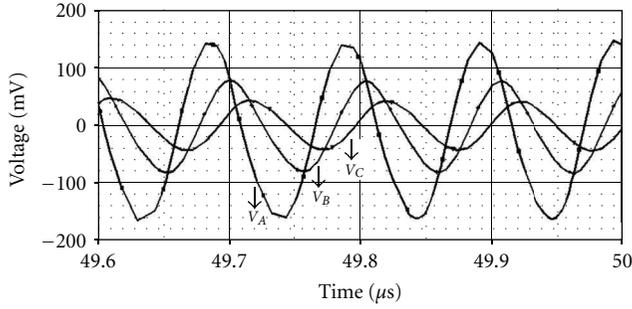


FIGURE 6: Output waveforms of sinusoidal oscillator.

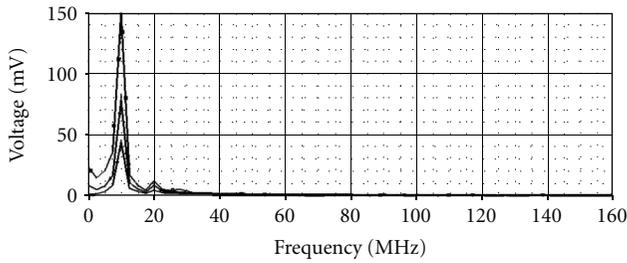
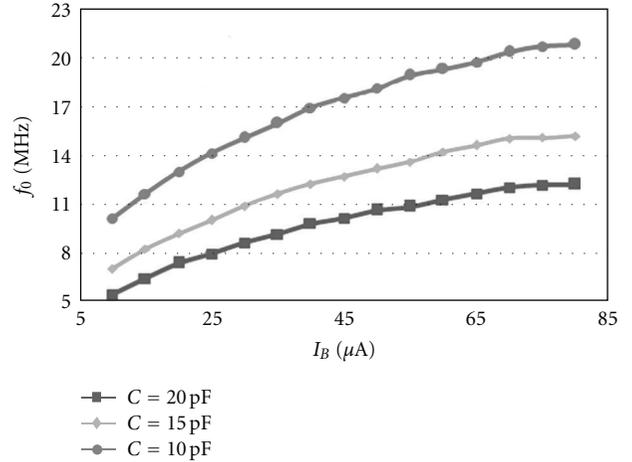


FIGURE 7: Fourier spectrum of output voltages.

## 6. Simulation Results

In order to prove the practical utility of the proposed circuit, the PSPICE simulations using the Level 3 model of TSMC MOSIS 0.25  $\mu\text{m}$  CMOS process parameters [24] are performed. The supply voltages used are  $V_{DD} = -V_{SS} = 1.25\text{ V}$ . The third-order sinusoidal oscillator based on the circuit in Figure 3 is designed for frequency of 10 MHz by selecting  $C_1 = C_2 = C_3 = C = 20\text{ pF}$ ,  $R_1 = 16\text{ K}$ ,  $I_{B1} = I_{B2} = I_{B3} = I_B = 40\text{ }\mu\text{A}$ , and  $I_{B4} = 13\text{ }\mu\text{A}$ . The three output sinusoidal waveforms of the oscillator circuit are shown in Figure 6. The simulated frequency of oscillation is around 9.78 MHz, thereby giving 0.2% error, which is quite low and acceptable. It may be noted that the three outputs have different amplitudes because of the basic structure being based on low-pass filters. Additionally, it is well known that the oscillators can be augmented for automatic amplitude control using diodes and resistor network, which are also popularly called the limiter circuits [25]. The simulated THD value is obtained to be 2.9%, which is moderately low. The Fourier spectrum of the voltage outputs is shown in Figure 7, where the second harmonic seems to be the main contributor to distortions, while higher harmonics are almost negligible. The frequency of oscillation can be varied by changing the input bias current  $I_B$ , independent of the condition of oscillation. The graph showing the variation in frequency of oscillation with the variation in bias current  $I_B$  for different values of capacitance “C” is given in Figure 8. The frequency of oscillation shows almost two and a half-fold variations for the variation in bias current from 10  $\mu\text{A}$  to 80  $\mu\text{A}$ .

FIGURE 8: Variation in  $f_0$  with  $I_B$  for different values of capacitors.

## 7. Conclusions

In this paper, a novel electronically tunable third-order sinusoidal oscillator using CCCIs and grounded components is proposed. This new circuit is synthesized from a simple topology employing cascaded first-order low-pass filters coupled with gained feedback. This circuit offers the advantages of the simultaneous availability of three sinusoidal voltage outputs and the use of grounded passive components which makes it suitable for IC implementation. The frequency of oscillation can be electronically tuned independently of the condition of oscillation through the bias currents of the active element. The generation circuitry of appropriate bias currents for the oscillator is given. Nonideal and parasitic considerations are included. The proposed circuit shows good high frequency performance and a wide-range electronic tuning of frequency. The proposed circuit is the novel addition to the already vast repertoire of literature on the subject and its IC implementation is a natural future problem.

## Acknowledgment

The authors thank reviewers for recommending the paper with some interesting suggestions, which made the paper more elegant. The authors are also thankful to the Associate Editor, Dr. Winai Jaikla for recommending this paper.

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