

## Research Article

# A Novel Pseudo-PMOS Integrated ISFET Device for Water Quality Monitoring

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The paper presents a performance analysis of novel CMOS Integrated pseudo-PMOS ISFET (PP-ISFET) having zero static power dissipation. The main focus is on simulation of power and performance analysis along with the comparison with existing devices, which is used for water quality monitoring. The conventional devices, generally used, consume high power and are not stable for long term monitoring. The conventional device has the drawbacks of low value of slew rate, high power consumption, and nonlinear characteristics, but in this novel design, due to zero static power, less load capacitance on input signals, faster switching, fewer transistors, and higher circuit density, the device exhibits a better slew rate and piecewise linear characteristics and is seen consuming low power of the order of 30 mW. The proposed circuit reduces total power consumption per cycle, increases the speed of operation, is fairly linear, and is simple to implement.

## 1. Introduction

Water is vital for all known forms of life. With the expansion of industrial production and increase in the population every year, wastewater produced by industry is discharged into rivers and lakes due to which the quality of water is degraded. Hence, it is the most urgent to take an effective measure to monitor and protect the water resources. The supervision of water quality is generally done by taking and analysing some liquid samples in the laboratory. This method is very expensive and tedious, and it can take several weeks to get tests result. Many research works have contributed to design quality measuring devices [1]. But it is always a challenge to select a more precise and accurate device for monitoring the quality. In today's scenario, as most of the complex functions are realized, due to which there is a growing demand for high density VLSI circuits resulting in scaling  $V_{dd}$  and an exponential increase of leakage or static power in deep submicron technology becomes essential to be taken care off. Therefore, reducing static power consumption of portable devices for water quality monitoring applications is highly desirable for a long term monitoring. As the size of the transistor decreases (i.e., technology), the transistors

density per unit chip Increases. The scaling of the device and very large integration of the transistors will lead to an increase in temperature and higher power consumption [2]. This increase in temperature will lead the increase in the overall cooling cost and complicated packaging techniques. The total power consumption in high performance digital circuits is mainly due to leakage currents. Leakage power makes up to 40% of the total power consumption in today's high performance monitoring circuits. Hence, leakage power reduction is very necessary for a low power design. The leakage power dissipation is given by the following equation:

$$P_{\text{static}} = I_{\text{leak}} * V_{\text{dd}}, \quad (1)$$

where  $I_{\text{leak}}$  is the leakage current when it is in OFF and  $V_{\text{dd}}$  is the supply voltage. The leakage current consists of following components:

- (1) gate leakage,
- (2) subthreshold leakage,
- (3) reverse-biased junction leakage,
- (4) gate-induced drain leakage.

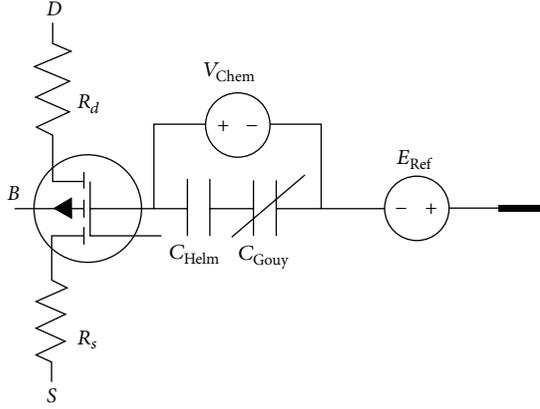


FIGURE 1: Subcircuit block of ISFET macromodel.

Out of these, subthreshold leakage and gate-leakage are dominant. The subthreshold leakage current of an MOS device can be given by:

$$I_{\text{sub}} = I_0 \exp \left[ \frac{(V_{\text{gs}} - V_t)}{(nV_T)} \right] \left[ 1 - \exp \left( \frac{-V_{\text{ds}}}{V_T} \right) \right], \quad (2)$$

$$I_0 = \mu_{\text{eff}} C_{\text{ox}} \left( \frac{W}{L} \right) V_T^2,$$

where  $W$  and  $L$  are the width and length of the channel, respectively,  $V_t$  is the threshold voltage,  $\mu_{\text{eff}}$  is the electron/hole mobility,  $C_{\text{ox}}$  is the gate oxide capacitance per unit area,  $n$  is the subthreshold swing coefficient,  $V_T$  is the thermal voltage,  $V_{\text{gs}}$  is the transistor gate to source voltage, and  $V_{\text{ds}}$  is the drain to source voltage.

**1.1. ISFET.** An ISFET is an ion-sensitive field-effect transistor which has a property of measuring ion concentrations in solution; when the ion concentration (such as  $\text{H}^+$ ) changes, the current through the transistor will change accordingly. Here, the solution is used as the gate electrode. A voltage between substrate and oxide surfaces arises due to an ions' sheath. The ISFET has similar structure as that of the MOSFET except that the poly gate of MOSFET is removed from the silicon surface and is replaced with a reference electrode inserted inside the solution, which is directly in contact with the hydrogen ion ( $\text{H}^+$ ) sensitive gate electrode [3] The Subcircuit block of ISFET macromodel is shown in Figure 1.

At the interface between gate insulator and the solution, there is an electric potential difference that depends on the concentration of  $\text{H}^+$  of the solution, or the so-called pH value. The variation of this potential caused by the pH variation will lead to modulation of the drain current. As a result, the  $I_d$ - $V_{\text{gs}}$  transfer characteristic of the ISFET, working in triode region, can be observed similar with that of MOSFET as follows:

$$I_{\text{ds}} = \frac{\mu C_{\text{ox}} W}{L} \left[ (V_{\text{gs}} - V_{\text{th(ISFET)}}) V_{\text{DS}} - \frac{1}{2} (V_{\text{ds}})^2 \right]. \quad (3)$$

The threshold voltage is only different in case of MOSFET. In ISFET, defining the metal connection of the reference electrode as a remote gate, the threshold voltage is given by

$$V_{\text{th(ISFET)}} = E_{\text{Ref}} + \Delta\Phi^{1j} - \Psi_{\text{eol}} + \chi^{\text{sol}} + \frac{-\phi_s}{q} - \frac{Q_{\text{ox}} + Q_{\text{ss}}}{C_{\text{ox}}} + \gamma \{2\phi\epsilon\}^{1/2} + 2\Phi_{\text{f}}, \quad (4)$$

where  $E_{\text{Ref}}$  is the potential of reference electrode,  $\Delta\Phi^{1j}$  is the potential drop between the reference electrode and the solution, which typically has a value of 3 mV [4].  $\Psi_{\text{eol}}$  is the potential which is pH independent; it can be viewed as a common-mode input signal for an ISFET interface circuit in any pH buffer solution and can be nullified during system calibration and measurement procedures with a typical value of 50 mV [5].  $\chi^{\text{sol}}$  is the surface dipole potential of the solvent being independent of pH; the terms in the parentheses are mostly the same as those of the MOSFET threshold voltage except that of the absence of the gate metal function. The other terms in the above equation are a group of chemical potentials, among which the only chemical input parameter shown has to be a function of solution pH value. This chemical dependent characteristic has already been explained by Hal and Eijkel's theory which is elaborated using the general accepted site-binding model and the Gouy-Chapman-Stern model. Conventional water quality monitoring applications are made up of voltage mode circuits (VMC) based on op-amps and OTA's. These applications suffer from low band widths (BW's) arising due to stray and circuit capacitances. Also, the need for low voltage and low power circuits makes these circuits not suitable for water quality monitoring as these circuits required the minimum bias voltage depending on the threshold voltage of the MOSFETs [6]. However, with the advancement in the analog VLSI new analog devices are developed called current mode circuits (CMC's). These circuits have a significant advantage of low power and low voltages and can operate over a wide dynamic range. These circuits, CMC, can offer to the designer large bandwidths, greater linearity, wider dynamic range, simple circuitry, and low power consumption. Current feedback op-amps (CFOAs), operational floating conveyors (OFCs), current conveyors (CCs), and so forth are popular CMC configurations and, the most widely used structure among them is CC-II. Hence, one can use the CC-II for the design prospective.

## 2. Pseudo-PMOS Logic

Pseudo-NMOS logic is a ratioed logic which uses a grounded PMOS load as a pull-up network and an NMOS driver circuit as pull-down network that realizes the logic function. The main advantage of this logic is that it uses only  $N + 1$  transistors and Vs  $2N$  transistors for CMOS, also this logic has less load capacitance on input signals, faster switching, and higher circuit density. In pseudo-NMOS logic, the high output voltage level for any gate is  $V_{\text{dd}}$ , and the low output

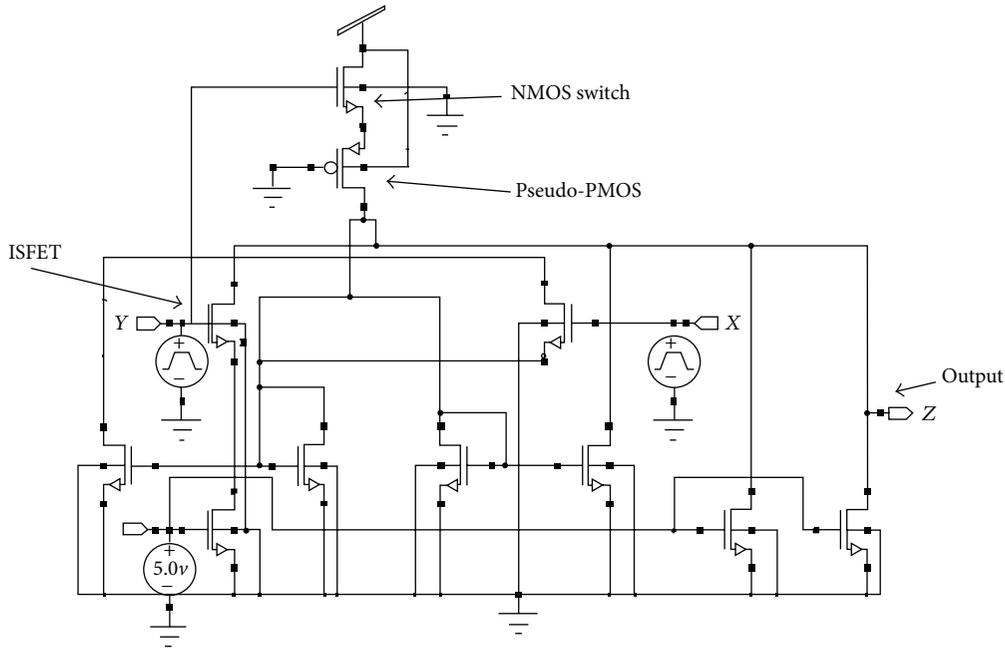


FIGURE 2: Circuit diagram of PP-ISFET.

voltage level is not 0 volt [7]. The only one main drawback of this logic is the very high static power consumption as there exists a direct path between  $V_{dd}$  and the ground through the PMOS transistor. In order to make low output voltage as small as possible, the PMOS device should be sized much smaller than the NMOS pull-down devices. But to increase the speed particularly when driving many other gates, the PMOS transistor size has to be made larger. Therefore, there is always a tradeoff between the parameters noise margin, static power dissipation, and propagation delay.

### 3. Device Description and Analysis

For the integrated sensor, the measurement circuit tracks the threshold voltage (or the flat-band voltage) of the ISFET as the electrolyte pH is varied. A practical solution to integrate the sensor with electronics is to view the ISFET sensor as a circuit component in an integrated circuit rather than as an add-on sensor whose output signals are further processed. In this paper, the ISFET is used as one of the input transistors in the differential stage of the current conveyor as shown in Figure 2. The circuit functions are as follows: when the PP-ISFET is configured as a voltage follower, the output voltage ( $V_o$ ) is equal to the input voltage ( $V_{in}$ ); any difference in threshold voltages and bias currents between the two input transistors at the differential input stage will also appear at the output. The distinct advantages of pseudo-PMOS which are less load capacitance on input signals, faster switching due to fewer transistors, and higher circuit density motivate us to implement this novel design. The only disadvantage of this logic is that pull up is always on due to which there is a significant static power dissipation. There are several methods already discussed above to reduce the static power

dissipation, but there is no method so far developed to completely avoid this drawback. In this novel design, the circuit has zero static power dissipation. The given circuit is designed in a pseudo-PMOS technology in which the gate of PMOS is grounded. There is one NMOS just above the grounded PMOS which acts as a switch and on only when input is applied, otherwise off. Since the circuit is only on when the input signal is applied, hence there is no direct path from  $V_{dd}$  to the ground which prevents the circuit from the static power dissipation.

### 4. Transient Analysis

Transient analysis of the PP-ISFET is observed on Tanner tool Version 15, and it is found that the output is fairly linear with respect to input with the passage of time as shown in Figure 3.

*4.1. Mathematical Regression Analysis.* In the regression statistics including multiple  $R$ ,  $R$  square, and adjusted  $R$  square, the standard error obtained during experiment is shown in Table 1. The ANOVA analysis (or analysis of variance) for the above device is shown in Table 2.

On plotting a linear trend line between  $V_y$  and  $V_z$ , the coefficient of determination  $R^2$  is found to be 99.7% with standard error of 0.081 as shown in Figure 4. The coefficient of determination  $R^2$  is useful because it gives the proportion of the variance (fluctuation) of one variable that is predictable from the other variable. It is a measure that allows us to determine how a certain one can be used in making predictions from a certain model. The coefficient of determination is a measure of how well the regression line represents the data. If the regression line passes exactly through every point on the scatter plot, it would be easy

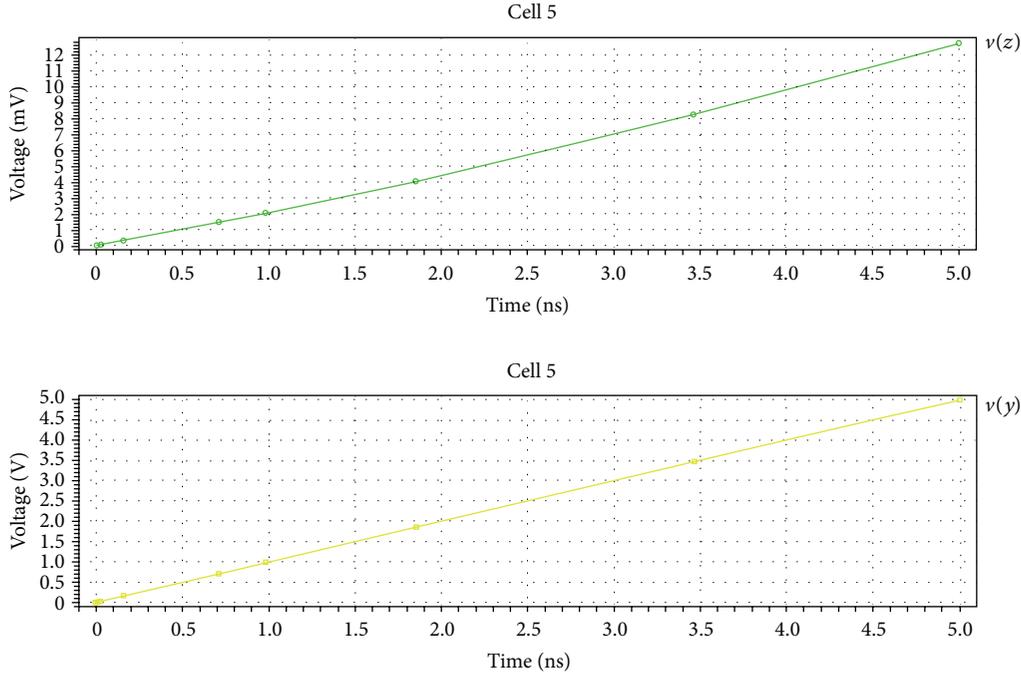


FIGURE 3: Transient analysis.

TABLE 1: Regression statistics.

Regression statistics	
Multiple R	0.998428255
R square	0.99685898
Adjusted R square	0.996662667
Standard error	0.08121496
Observations	18

TABLE 2: ANOVA analysis.

	df	ANOVA			Significance F
		SS	MS	F	
Regression	1	33.49	33.492	5077.88	$1.86E - 21$
Residual	16	0.10	0.0065		
Total	17	33.59			

to explain all the variations. The standard error is the error that would be expected between the predicted and actual dependent variable. The least value of standard error shows how close the predicted and actual readings are.

ANOVA is a simple analysis of variance on data for two or more samples.

The ANOVA table gives the following information:

- (1) degrees of freedom (df),
- (2) the sum of the squares (SS),
- (3) the mean square (MS),

(4) the  $F$  ratio ( $F$ ),

(5) the significance  $F$ .

The analysis provides a test of the hypothesis that each sample is drawn from the same underlying probability distribution against the alternative hypothesis that underlying probability distributions are not the same for all samples. A high  $F$  value, 5077.88, shows that most of the means are fairly similar, but one of the means happens to be far removed from the other means; that is, the standard error is the least, and the device is accurate.

**4.2. Residual Plot.** A residual plot between output and input determines if the regression model is a good fit to your data. When plotted, the residuals should be random. There should be no recognizable pattern. Good regression models give uncorrelated residuals. The residual plot for the device is plotted and shown in given Figure 5.

**4.3. Normal Probability Plot.** The normal probability plot is a special case of the probability plot. The points on this plot form a nearly linear pattern, which indicates that the normal distribution is a good model for this data set. The normal probability plot for the device is plotted and shown in Figure 6.

## 5. Result Analysis

The various results obtained are summarized in this section. Figures 7 and 8 show the component count and the power consumption comparisons.

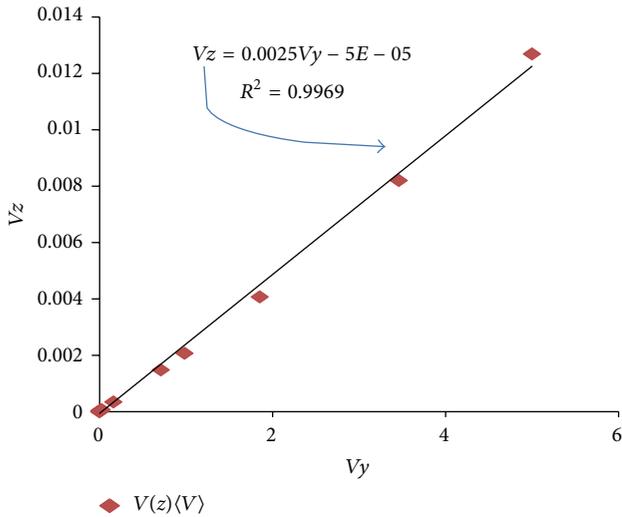


FIGURE 4: Trend line between  $V_y$  and  $V_z$  obtained from SPICE model readings with the coefficient of determination.

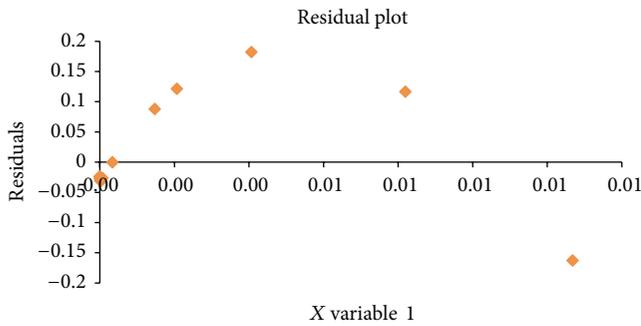


FIGURE 5: Residual plot.

On comparing the new design with the existing design, we arrive at following results.

- (a) The number of MOSFETs is 27 in [1], 16 in [2] for conventional devices; only 9 are used in the new device, later deploys 17% of components over 52% [8] and 31% [9] used in the previous devices.
- (b) Static power is almost zero.
- (c) No capacitor is used in the new technique.
- (d) The number of current sources deployed is 4-3 in conventional device and 0 in the new device.
- (e) The numbers of n-MOS and p-MOS required are as follows: 17 and 10 in [8] and 10 and 6 in [9] for conventional devices and 8 and 1 for the new device.
- (f) No resistor is required in the new technique.
- (g) Voltage sources required for proper operation of the devices are 4 in [8] and 2 in [9] for conventional devices and 1 in the new device.

From Table 3, we can figure out that there is a significant saving in terms of Components. Hence, we came to a conclusion that the circuit proposed here meets all our requirements

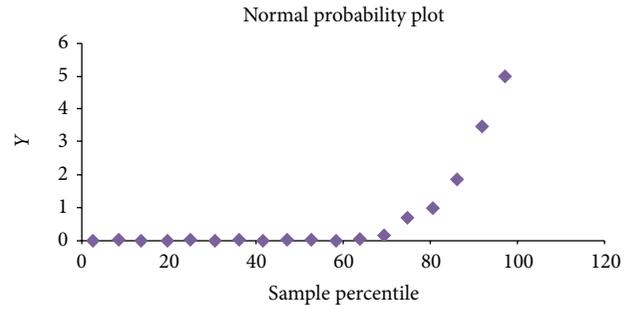


FIGURE 6: Normal probability plot.

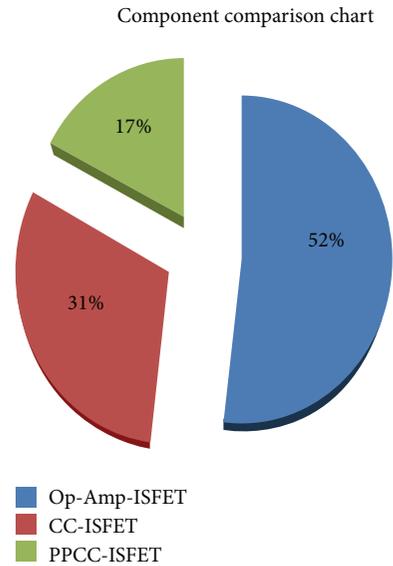


FIGURE 7: Component comparison chart.

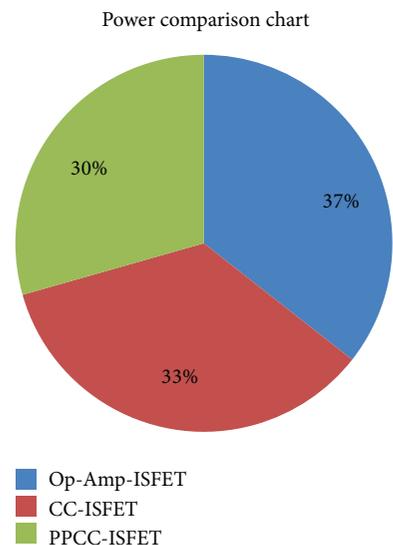


FIGURE 8: Power comparison chart.

TABLE 3: Comparative analysis with existing devices.

Parameters	Op-Amp-ISFET [8]	CC-ISFET [9]	PP-ISFET
Technology	CMOS	CMOS	Pseudo-PMOS
Power supply	0 V–5 V	0 V–5 V	0 V–5 V
No. of MOSFETs	27	16	9
Capacitor	2	2	0
Current source	4	3	0
NMOS	17	10	8
PMOS	10	6	1
Resistor	5	5	0
Voltage source	4	2	1
Max power (W)	$3.63e - 002$	$3.57e - 002$	$3.00e - 002$
Min power (W)	$2.13e - 005$	$0.13e - 005$	$0.00e + 000$
Stability analysis	Closed loop Stable	Closed loop Stable	Closed loop Stable

in terms of component saving, that is, miniaturization and power efficiency.

## 6. Conclusion

In this novel design, a new device employing PP-ISFET is proposed. The PP introduced is a convenient building block that provides a simplified approach to the design of linear analog systems. It also consumes considerably low power. There is a significant improvement in the slew rate. The output observed is highly linear. A significant advantage of the proposed design is its simple architecture and low component count. Therefore, it is very suitable for water quality monitoring applications. This study may be extended for further improvements in terms of power and size, besides the wiring and layout characteristics level.

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