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Research Article

A Novel Power Electronic Inverter Circuit for Transformerless Photovoltaic Systems

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Capacitive leakage current is one of the most important issues for transformerless photovoltaic systems. In order to deal with the capacitive leakage current, a new power electronic inverter circuit is proposed in this paper. The inverter circuit consists of six switches and operates with constant common mode voltage. Theoretical analysis is conducted to clarify the circuit operation principle and the common mode characteristic. The performance evaluation test is carried out, and test results demonstrate that the capacitive leakage current can be significantly minimized with the proposed power electronic inverter circuit.

1. Introduction

Photovoltaic (PV) power systems are very attractive and widely used in recent years. In order to integrate the PV systems into grid, a power electronic component should be required to convert DC energy source generated by PV arrays to AC component [1], which is fed into grid. In general, a transformer is installed between PV arrays and grid for galvanic isolation. The transformer is heavy with large volume, along with the copper and iron losses during transformer operation [2, 3]. Therefore, the transformerless PV system is popular and received more and more attention [4–12], due to its low cost, small size, and high efficiency. However, a technical challenge arises for transformerless PV systems. More specifically, the capacitive leakage current is generated between photovoltaic modules and the ground [13]. In practice, this capacitive leakage current is very difficult to handle, because the capacitance between photovoltaic modules and ground is usually highly unpredictable, and it varies significantly with temperature or humidity [14]. The presence of leakage currents is very harmful, since they could put the life of a photovoltaic module installer at risk if he touches the photovoltaic module [15]. Additionally, they will bring high-frequency harmonics, which may lead to problems with electromagnetic compatibility [16]. Therefore, it is important to deal with the capacitive leakage current problem in the transformerless PV system.

The objective of this paper is to present a novel power electronic inverter circuit for transformerless photovoltaic system. The capacitive leakage current can be minimized with the proposed inverter circuit.

2. Circuit Description

The schematic diagram of the proposed power electronic inverter circuit is illustrated in Figure 1. It should be noted that the parasitic capacitance between ground and positive terminal of dc bus point is one of the factors for the system stray capacitance. In this case, considering the entire stray capacitances of C_{pv}, the parasitic capacitance between ground and positive terminal of the inverter dc bus point will be $C_{pv}/2$ and so is the capacitance of ground-negative terminal, as shown in Figure 1. The capacitance value depends on the PV panel frame structure, weather conditions, humidity, and so on. Therefore, it is usually highly unpredictable. In order to clarify the capacitive leakage current minimization

Table 1: Operation modes and voltages.

	S_1	S_2	S_3	S_4	S_5	S_6	U_{an}	U_{bn}	U_{cm}
Mode 1	1	0	0	1	0	1	V_d	0	$V_d/2$
Mode 2	0	0	0	0	0	1	$V_d/2$	$V_d/2$	$V_d/2$
Mode 3	0	1	1	0	1	0	0	V_d	$V_d/2$
Mode 4	0	1	0	0	0	0	$V_d/2$	$V_d/2$	$V_d/2$

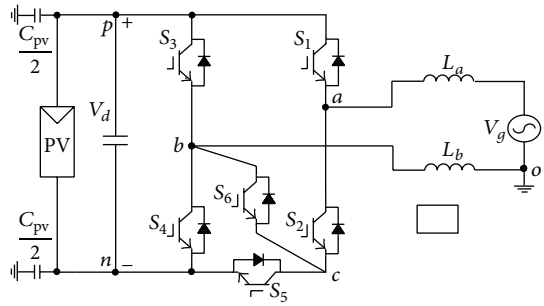


Figure 1: Schematic diagram of proposed power electronic inverter circuit.

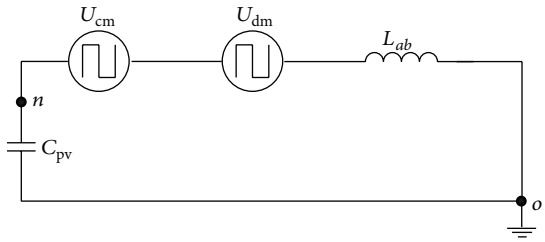


Figure 2: System's common mode model [17].

mechanism, the system's common mode model is built, as shown in Figure 2, where U_{cm} is the common mode voltage and U_{dm} is defined as follows:

$$U_{cm} = \frac{U_{an} + U_{bn}}{2}, \tag{1}$$

$$U_{dm} = \frac{U_{ab}(L_a - L_b)}{2(L_a + L_b)}, \tag{2}$$

$$L_{ab} = \frac{L_a L_b}{L_a + L_b}. \tag{3}$$

In practice, the filter inductors L_a and L_b are designed with the equal value; that is, $L_a = L_b$. So, the differential mode voltage U_{ab} does not contribute to the capacitive leakage current, as shown in (2) and Figure 2.

On the other hand, if the common mode voltage U_{cm} is time varying, the capacitive leakage current will arise and flow in the loop, as shown in Figure 2.

In order to deal with the capacitive leakage current, it is of great importance that the common mode voltage U_{cm} in Figure 2 should be kept constant. The following will present this objective achieved by the proposed power electronic inverter circuit.

The proposed inverter circuit operates in four modes, as shown in Figure 4 and Table 1.

In Mode 1, the switches S_1, S_4, and S_6 are turned on, and other switches are turned off. The differential mode voltage U_{ab} is V_d, while the common mode voltage can be expressed as

$$U_{cm} = \frac{1}{2}(U_{an} + U_{bn}) = \frac{1}{2}(V_d + 0) = \frac{V_d}{2}. \tag{4}$$

In Mode 2, only the switch S_6 is turned on, and other switches are turned off. The current flows through S_6 and diode of S_2. In this case, the differential mode voltage U_{ab} is 0, while the common mode voltage remains unchanged as

$$U_{cm} = \frac{1}{2}(U_{an} + U_{bn}) = \frac{1}{2}\left(\frac{V_d}{2} + \frac{V_d}{2}\right) = \frac{V_d}{2}. \tag{5}$$

In Mode 3, the switches S_2, S_3, and S_5 are turned on, and other switches are turned off. The differential mode voltage U_{ab} is $-V_d$, while the common mode voltage can be expressed as

$$U_{cm} = \frac{1}{2}(U_{an} + U_{bn}) = \frac{1}{2}(0 + V_d) = \frac{V_d}{2}. \tag{6}$$

In Mode 4, only the switch S_2 is turned on, and other switches are turned off. The current flows through S_2 and diode of S_6. In this case, the differential mode voltage U_{ab} is 0, while the common mode voltage U_{cm} remains unchanged as

$$U_{cm} = \frac{1}{2}(U_{an} + U_{bn}) = \frac{1}{2}\left(\frac{V_d}{2} + \frac{V_d}{2}\right) = \frac{V_d}{2}. \tag{7}$$

In summary, the above analysis reveals that the common mode voltage can be kept constant as $V_d/2$ all the time. Therefore, the capacitive leakage current can be significantly minimized, according to theoretical analysis of Figure 2. The following will present the test results.

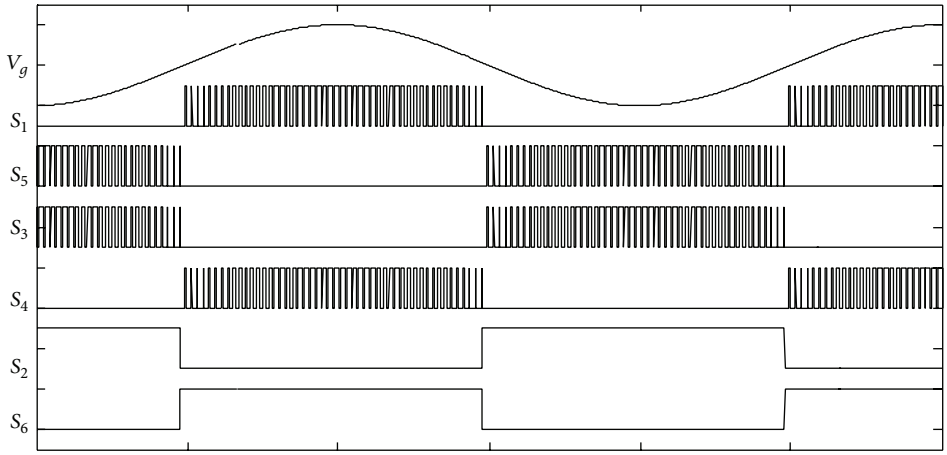
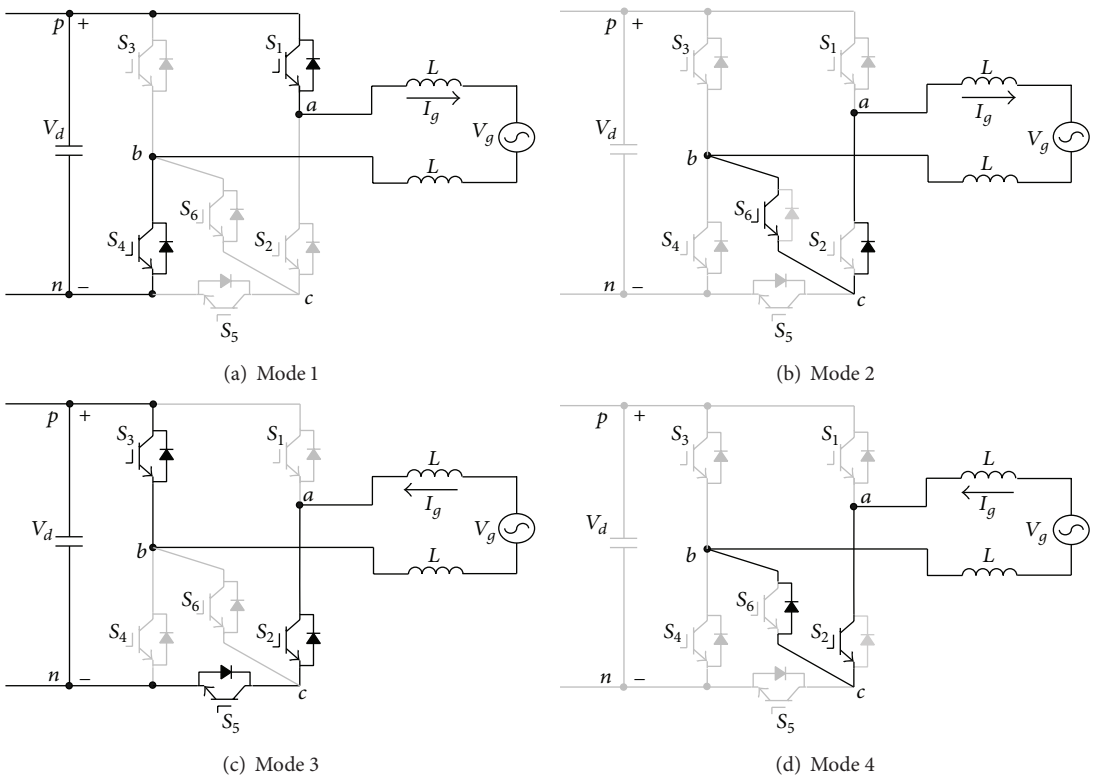


Figure 3: Switching state of the proposed inverter circuit.



(a) Mode 1

(b) Mode 2

(c) Mode 3

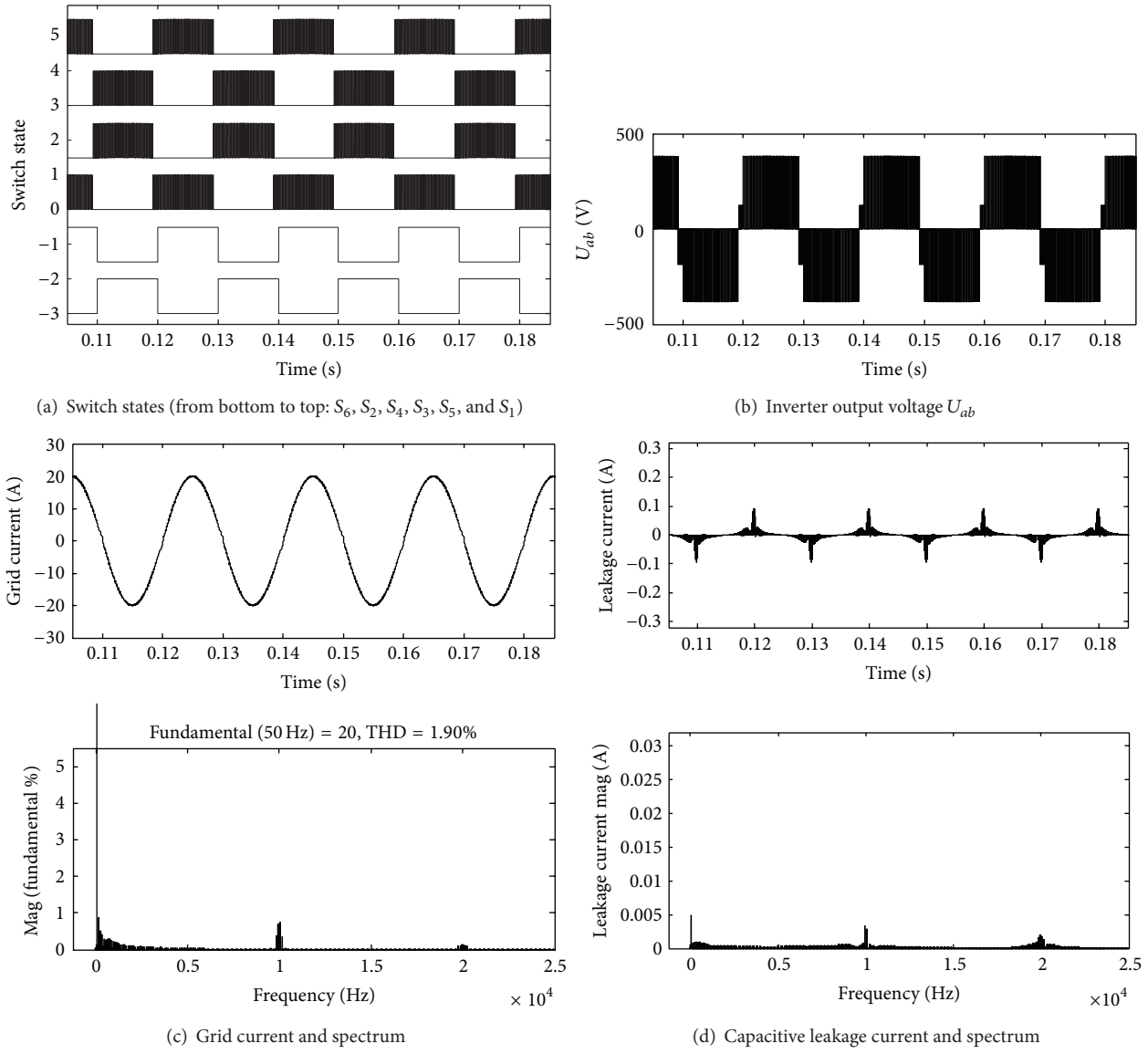
(d) Mode 4

Figure 4: Operation modes of the proposed inverter.

3. Performance Evaluation

In order to verify the effectiveness of the proposed power electronic inverter circuit, the inverter circuit is designed in MATLAB/Simulink. The circuit components and parameters are listed as follows: system power is 3 kW, dc bus voltage V_d is 400 V, grid voltage V_g is 220 Vac, grid frequency is 50 Hz, inverter circuit switching frequency is 10 kHz, circuit filter inductor $L_a = L_b = 3$ mH, and parasitic capacitor $C_{\text{PV}} = 100$ nF; see Figure 3.

Figure 5(a) shows the test waveform of the switch states; it can be observed that, at any given time, only two switches operate in high-frequency mode and the other four switches operate in low-frequency mode, so the high efficiency can be achieved. On the other hand, the inverter output voltage waveform is shown in Figure 5(b), where three-level output



(a) Switch states (from bottom to top: S_6, S_2, S_4, S_3, S_5, and S_1)

(b) Inverter output voltage U_{ab}

(c) Grid current and spectrum

(d) Capacitive leakage current and spectrum

Figure 5: Test results.

voltage is achieved. It is beneficial to the grid current ripple reduction. Figure 5(c) shows the grid current waveform and its spectrum analysis. It can be seen that the grid current is sinusoidal with the total harmonic distortion of 1.9%, which is well below 5% specified in IEEE Std. 929-2000 [18].

Figure 5(d) shows the capacitive leakage current waveform and its spectrum analysis. It can be seen that the leakage current is well below 300 mA specified in VDE 0126-1-1, thanks to the proposed power electronic inverter.

4. Conclusion

This paper has presented a new power electronic inverter circuit. Its unique feature lies in that the proposed circuit can keep the system's common mode voltage constant all the time, and thus the capacitive leakage current can be significantly minimized, which complies with the international standard IEEE Std. 929-2000 and VDE 0126-1-1. Therefore, it is attractive to the transformerless photovoltaic system applications. It should be noted that other different inverter circuits are also interesting and can be used for the transformerless photovoltaic system applications; please refer to [19, 20] for further reading.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

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