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*Research Article*

# Design of a 2 GHz Linear-in-dB Variable-Gain Amplifier with 80-dB Gain Range

**Zhengyu Sun and Yuepeng Yan**

*Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China*

Correspondence should be addressed to Zhengyu Sun; szy7888@gmail.com

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A broadband linear-in-dB variable-gain amplifier (VGA) circuit is implemented in 0.18 $\mu$m SiGe BiCMOS process. The VGA comprises two cascaded variable-gain core, in which a hybrid current-steering current gain cell is inserted in the Cherry-Hooper amplifier to maintain a broad bandwidth while covering a wide gain range. Postlayout simulation results confirm that the proposed circuit achieves a 2 GHz 3-dB bandwidth with wide linear-in-dB gain tuning range from −19 dB up to 61 dB. The amplifier offers a competitive gain bandwidth product of 2805 GHz at the maximum gain for a 110-GHz $f_t$ BiCMOS technology. The amplifier core consumes 31 mW from a 3.3 V supply and occupies active area of 280 $\mu$m by 140 $\mu$m.

## 1. Introduction

The telecommunication industry continues to drive forward with gigabit-class high-speed data transmission in microwave, millimeter-wave, and optical communication systems. Higher data rate transmission requires wider bandwidth and larger dynamic range for the receiver system. For example in the 60 GHz standards such as IEEE 802.11ad [1], the spectrum is about 2 GHz. And the signal strength at the receiver input can change dramatically which is common in short-range wireless systems. VGA as a key component in the automatic gain control (AGC) loop provides constant signal strength to the baseband processor to maximize the dynamic range of the receiver system and compensates gain variations caused by process, voltage, and temperature (PVT) variations. Research in SiGe and CMOS circuits in the broadband VGA is an active topic in optical, wireline, and millimeter-wave receivers [2–6]. Among various broadband techniques, Cherry-Hooper amplifier [7] has had numerous applications in AGC and limiting amplifiers. Solutions employing Cherry-Hooper amplifier [8] can achieve a 3-dB bandwidth above 2 GHz and satisfy bandwidth requirements such as 60 GHz short-range wireless systems. However, their gain range is not sufficient to meet the target of more than 80 dB if additional margin is needed for the receiver. Moreover, a linear-in-dB control signal for VGA will simplify the system level design for AGC.

In this paper, a VGA circuit is presented for high-speed data communication systems. In Section 2, a new variable gain core is designed by combining a hybrid current-steering cell with the Cherry-Hooper amplifier. Section 3 describes the VGA system which is made up of variable gain core introduced in Section 2 and other circuits. Section 4 shows the postlayout simulation results. Finally, Section 5 draws the conclusions.

## 2. Variable Gain Core Design

The schematic of the proposed variable gain core is shown in Figure 1. In order to maintain a broad bandwidth while covering a wide gain range, a hybrid current-steering (HCS) current gain cell is inserted in the Cherry-Hooper amplifier. The HCS cell is featured with a constant DC current output and an ability to have same AC characteristics with classical current-steering (CS) cell. The gain is varied through only the HCS cell without degrading the broadband characteristic of Cherry-Hooper amplifier with constant gain.

*2.1. Broadband Amplifier Topology.* If the current gain cell is removed from the gain core shown in Figure 1 the topology

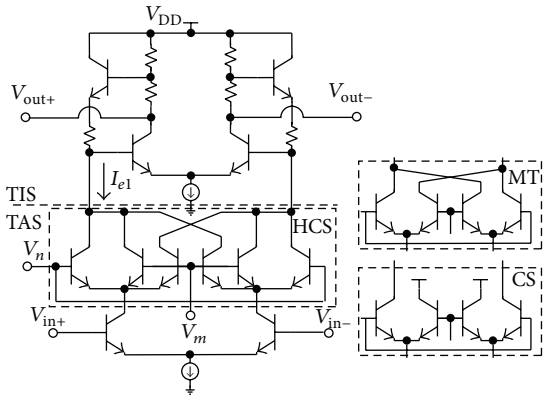


Figure 1: Proposed variable gain core with hybrid current-steering cell.

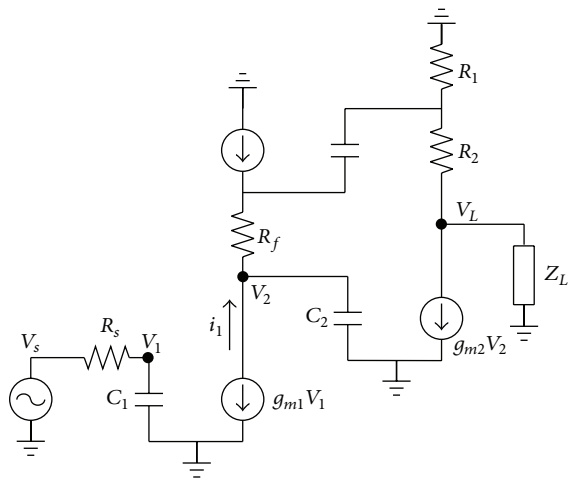


Figure 2: Small signal equivalent circuit for the TAS-TIS combination.

is a differential Cherry-Hooper (CH) amplifier with emitter-follower feedback [9]. The Cherry-Hooper amplifier is a cascading combination of a transadmittance stage (TAS) with a transimpedance stage (TIS). The strong mismatch between the two stages results in a large bandwidth [7]. This topology has the advantage of extending the bandwidth by moving the dominant poles from lower pole determined by load capacitance and the output resistance to the much higher poles. The shunt-shunt feedback employs an emitter follower which isolates the bias currents through the TAS and TIS. Both the emitter follower and the resistor in the feedback loop help to raise the gain at high frequency.

Because of the symmetry, the differential Cherry-Hooper amplifier with emitter-follower feedback can be analyzed through single-ended part. Figure 2 is the small signal equivalent circuit for the TAS-TIS combination including major parasitic parameter. Since the TIS is usually followed by transconductor stage or emitter follower, the load of Cherry-Hooper amplifier can be approximately assumed to be a capacitor $C_L$. Thus, the input impedance of TIS stage can be derived as

$$Z_{\text{in}} = \frac{v_2}{i_1} = \frac{R_f}{1 + g_{m2}R_1} \cdot \left( \left(1 + sC_L\left(R_1 + R_2\right)\right) \times \left(1 + \frac{C_2R_f + C_L\left(R_1 + R_2\right)}{1 + g_{m2}R_1}s + \frac{C_2C_LR_f\left(R_1 + R_2\right)}{1 + g_{m2}R_1}s^2\right)^{-1}\right). \tag{1}$$

The transimpedance gain of TIS stage can also be derived as

$$Z_t = \frac{v_L}{i_1} = -\frac{g_{m2}}{C_2C_L\left(s^2 + \left(w_0/Q\right)s + w_0^2\right)}, \tag{2}$$

where

$$w_0 = \sqrt{\frac{1 + g_{m2}R_1}{C_2C_LR_f\left(R_1 + R_2\right)}}, \tag{3}$$

$$Q = \sqrt{\frac{C_2C_LR_f\left(R_1 + R_2\right)\left(1 + g_{m2}R_1\right)}{\left(C_2R_f + C_LR_1 + C_LR_2\right)^2}}. \tag{4}$$

From (2) and (3), there is a trade-off between DC gain and bandwidth through resistors $R_f$ and $R_2$. Increasing $R_2$ or $R_f$ will raise the DC gain while reducing bandwidth.

From (1), the input impedance of TIS stage is $(1 + g_{m2}R_1)$ times less than $R_f$ and is relatively low impedance compared to the output impedance of TAS stage. Therefore, the overall voltage gain of TAS-TIS combination can be approximately seen as the product of transadmittance gain and transimpedance gain as

$$A_v = \frac{v_L}{v_s} = \frac{i_1}{v_s} \cdot \frac{v_L}{i_1} = G_mZ_t, \tag{5}$$

with the transadmittance gain as

$$G_m = \frac{i_1}{v_s} = \frac{g_{m1}}{1 + sC_1R_s}, \tag{6}$$

where $R_s$ is the output impedance of preceding stage.

Since the input impedance of TAS stage is usually much larger than the $R_s$, the pole of TAS stage is much larger than of TIS stage. Therefore, the dominant pole of the Cherry-Hooper amplifier is mostly contributed by the poles of TIS stage.

The output impedance of TIS stage can also be derived as

$$Z_{\text{out}} = \frac{R_1 + R_2}{1 + g_{m2}R_1} \cdot \frac{1 + sC_2R_f}{1 + s\left(C_2R_f/\left(1 + g_{m2}R_1\right)\right)}, \tag{7}$$

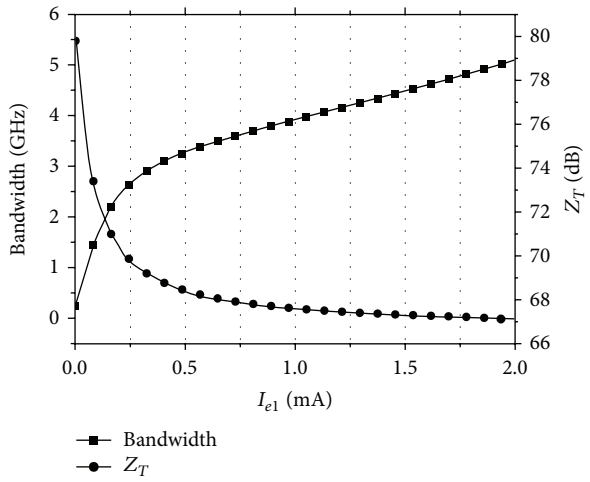


Figure 3: Transimpedance gain and its bandwidth versus bias current $I_{e1}$.

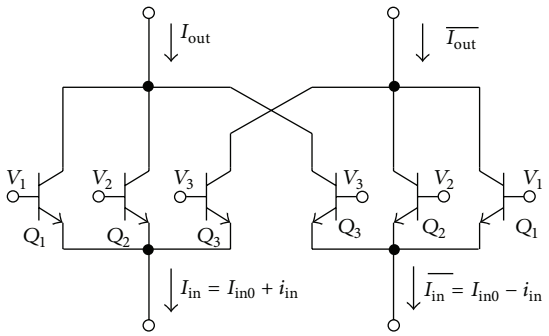


Figure 4: Generalized hybrid current-steering current gain cell.

which shows relatively low impedance that can drive the following stage.

For broadband amplifier design, the bias currents through the TAS and TIS are constant to maintain the transistors biased at near peak $f_t$ current density. Then the desired gain and bandwidth are determined by the resistors in the feedback and load. If the DC current $I_{e1}$ in the TAS changed, the frequency response of the TIS will be changed as well since the bias conditions of transistors in emitter-follower and TIS are changed. Figure 3 shows the transimpedance gain between output voltage and current flowing out of TAS with its 3-dB bandwidth at different bias DC current $I_{e1}$. Decreasing the DC current $I_{e1}$, the bandwidth will decrease while the gain will increase. Such effect is detrimental to the integrity design of the Cherry-Hooper amplifier.

*2.2. Current Gain Cell.* There are two commonly used current gain cells as shown on the right side of Figure 1: current-steering (CS) cell and multiplier (MT) cell. The current-steering cell has better dynamic range performance but its DC output current is not constant. The multiplier cell has constant DC output level due to the cross coupling of the quad

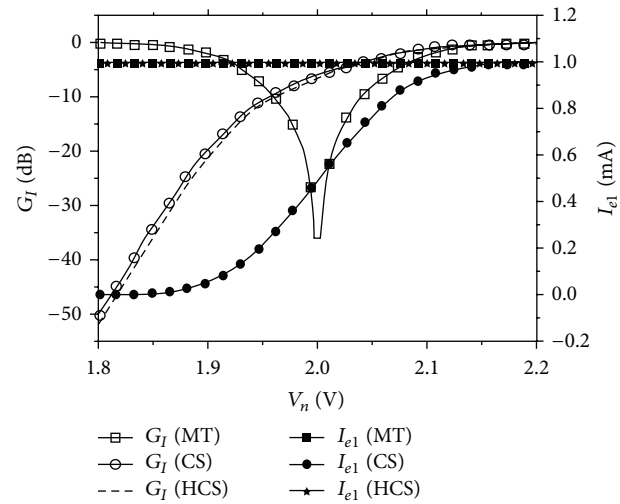


Figure 5: Comparison of current gain and DC current output $I_{e1}$ of MT, CS and HCS cell.

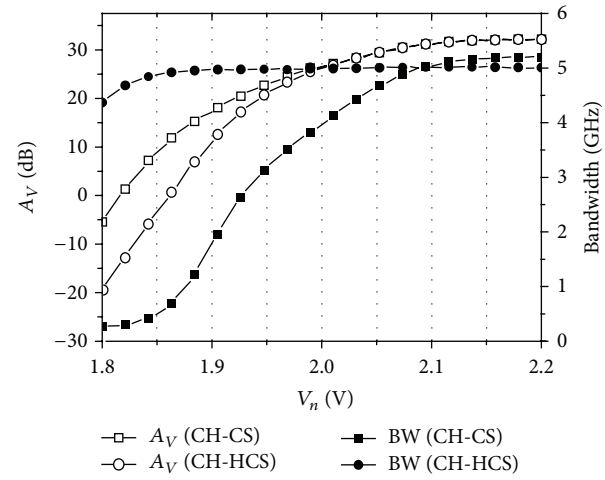


Figure 6: Comparison of voltage gain and its bandwidth of Cherry-Hooper amplifier with CS and HCS cell.

collectors but its gain polarity will change at certain control voltage leading to a limited tuning range.

In order to maintain the broadband characteristics of the Cherry-Hooper amplifier while covering a wide gain range, a hybrid current-steering current gain cell is employed to change gain while having the least influence to the Cherry-Hooper amplifier. A generalized hybrid current-steering cell is shown in Figure 4. The cell is symmetrical about the $y$-axis, thus the DC current output is equal to the DC current input. The output current coming out of the cell is related to the input current as follows:

$$\begin{aligned} I_{\text{out}} &= (\alpha_1 + \alpha_2)(I_{\text{in0}} + i_{\text{in}}) + \alpha_3 (I_{\text{in0}} - i_{\text{in}}) \\ &= I_{\text{in0}} + (\alpha_1 + \alpha_2 - \alpha_3)\, i_{\text{in}} \end{aligned} \tag{8}$$

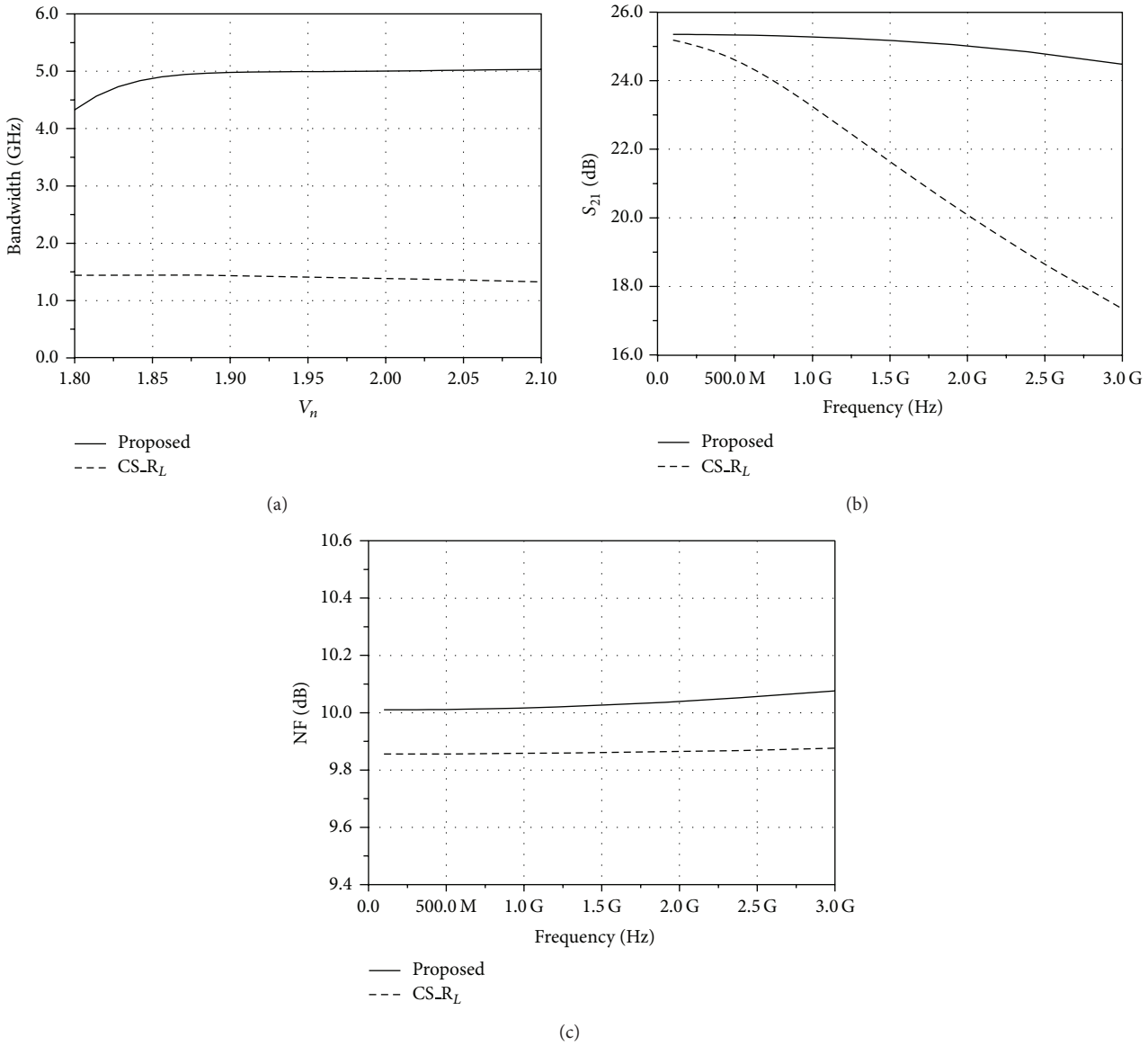


Figure 7: Comparison between proposed CH-HCS cell and CS-R$_L$ cell.

where $\alpha_n$ is the current proportion of the $n$th branch dependent on transistor size and bias voltage as follows:

$$\alpha_n = \frac{1}{\sum_{i=1}^{3} \left(I_{0i}/I_{0n}\right) \exp\left(\left(V_i - V_n\right)/V_T\right)}. \tag{9}$$

Thus the current gain is expressed as

$$G_I = \alpha_1 + \alpha_2 - \alpha_3. \tag{10}$$

In the proposed VGA, a special case with equal $V_2$ and $V_3$ voltage and transistor size arrangement as $Q_1 : Q_2 : Q_3 = 2 : 1 : 1$ [10] is employed with current gain derived from (9) and (10) as follows:

$$G_I = \alpha_1 = \frac{1}{1 + \exp\left(\left(V_2 - V_1\right)/V_T\right)}. \tag{11}$$

The current gain expression of the hybrid current-steering cell is the same as the conventional current-steering cell, which implies that the same linear-dB technology for CS cell can also be used for HCS cell. Figure 5 compares the current gain and DC output current of the three current gain cells: CS, MT, and HCS. The HCS cell has the same wide gain-tuning ability as CS cell while having a constant DC output current as MT cell.

*2.3. Broadband Variable Gain Core.* The strong impedance mismatch between gain stages for broadband technique is maintained with the insertion of hybrid current-steering cell in the middle of the Cherry-Hooper amplifier. The transadmittance stage is composed of the input transconductance amplifier and the hybrid current-steering cell, which has a high input and high output impedance. It is followed by the

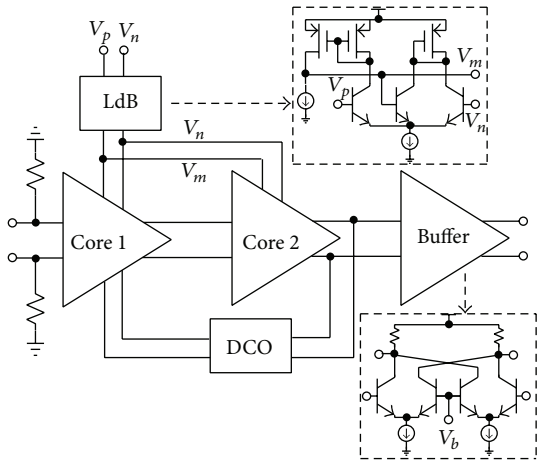


Figure 8: Block diagram of proposed VGA system.

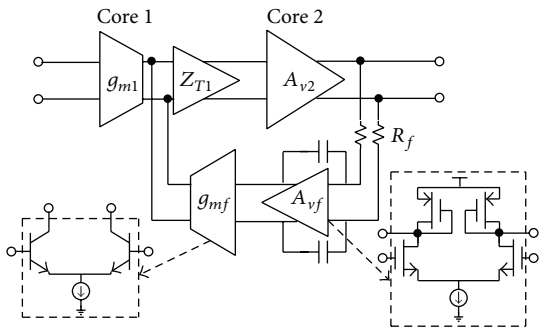


Figure 9: Block diagram of DC offset correction circuit.

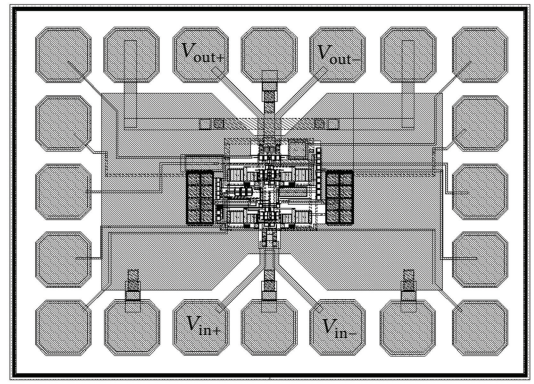


Figure 10: Layout of the VGA.

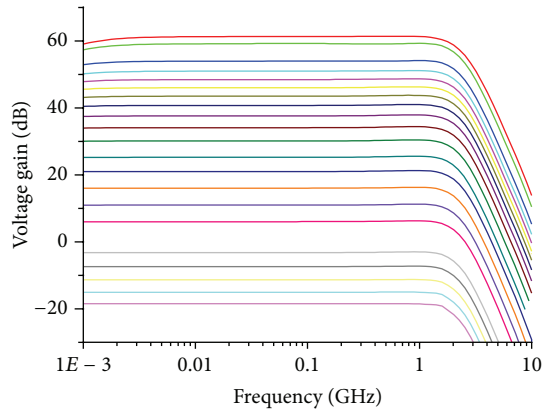


Figure 11: Frequency response versus various control voltage $V_p$.

transimpedance stage which has low input and low output impedance. The bias current of the input transconductance amplifier is reused by the HCS cell and the emitter follower in the feedback path. Since the current gain cell operates as common-base amplifier, the bandwidth of it is much wider than that of the Cherry-Hooper amplifier. Thus the dominant poles of Cherry-Hooper amplifier still dominate the 3-dB bandwidth of the variable gain core and can be optimized to strike a balance between characteristics such as gain, bandwidth, gain flatness, and group delay using guidelines [9].

To show the advantage of the proposed structure, another structure with only difference in that its current gain cell was replaced with a current-steering cell was also designed. Figure 6 shows the comparison of the Cherry-Hooper amplifiers inserted with hybrid current-steering (CH-HCS) cell and with current-steering (CH-CS) cell. The 3-dB bandwidth of the CH-CS cell decreases rapidly with decreasing control voltage, while the bandwidth of CH-HCS cell maintains being flat above 4 GHz in spite of control voltage changing. Moreover, the relationship between gain and control voltage of CH-CS cell is deviated from the CH-HCS cell at low gain range due to the transimpedance gain increases as indicated in Figure 3.

In order to further show the advantage of the proposed CH-HCS cell over traditional current-steering type VGA with load resistor $R_L$ (CS-$R_L$), a CS-$R_L$ cell of the same DC current consumption and peak gain as the CH-HCS cell is designed. The 3-dB bandwidth varying with control voltage is compared in Figure 7(a), which shows that a threefold GBW can be achieved using CH-HCS cell. Figures 7(b) and 7(c) compare the $S_{21}$ and noise figure at the maximum gain, which shows a similar noise performance and wider GBW for the CH-HCS cell over traditional CS-$R_L$ cell.

## 3. VGA Architecture

The proposed VGA architecture is shown in Figure 8. In order to obtain a gain range over 70 dB, two cascaded stages of variable gain core mentioned in Section 2 are employed with each providing about 40-dB gain range. Since the transadmittance and transimpedance stages in one gain core have independent bias currents and allow a dc-coupled output, the first core in cascaded stages behaves as an output buffer to the second core which can eliminate the DC blocking capacitor. For testing purposes, 50 ohm resistors are placed at the differential inputs for input matching and a high-speed $f_t$ doubler output buffer is used at the output.

In order to reduce DC offsets due to component mismatch, a differential feedback loop is designed with its schematic shown in Figure 9. The differential output voltage

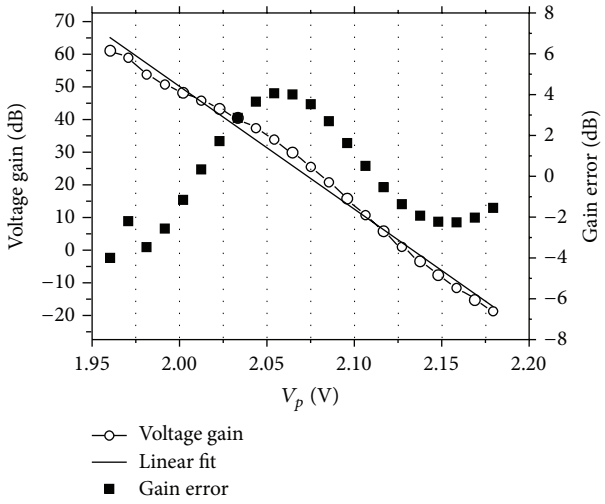


Figure 12: Voltage gain and gain linearity versus control voltage $V_p$.

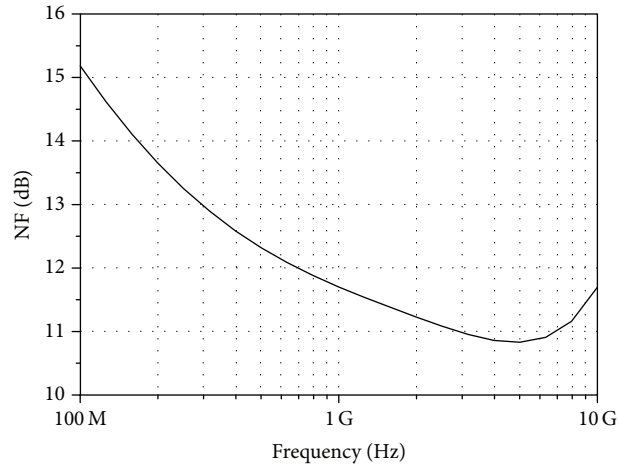


Figure 13: Noise figure at maximum gain.

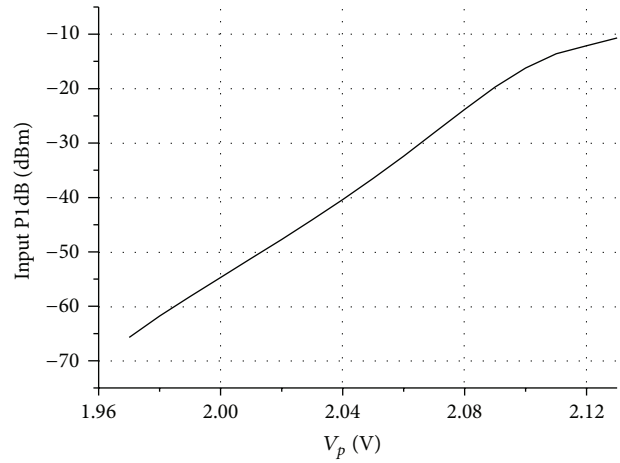


Figure 14: Input P1 dB versus control voltage $V_p$.

of the second variable gain core is sensed by a RC LPF at low frequency and stored in the Miller capacitances. Following a high input impedance voltage amplifier using an NFET differential pair, a transconductance amplifier using an NPN differential pair transforms the input voltage into differential current which is injected back to the output of the transadmittance stage of the first gain core to adjust the output DC offset voltage. This DC offset loop is designed to have a low pass frequency response with a cut-off frequency of 800 kHz.

As mentioned in Section 2, the hybrid current-steering cell has the same relationship between gain and control voltage with the conventional current-steering cell. Thus a curvature linearization circuit [11] designed for current-steering cell is employed to the gain cores in two stages to make the gain control linear-in-dB.

## 4. Postlayout Simulation Results

The proposed architecture is implemented in HHNEC's 0.18 $\mu$m SiGe HBT BiCMOS technology which integrates 0.2 $\mu$m, 1.8 V $BV_{CEO}$, 110 GHz $f_t$ SiGe HBTs, together with 0.18 $\mu$m, 1.8 V Si CMOS devices. The layout of the chip is shown in Figure 10. The VGA occupies 280 $\mu$m by 140 $\mu$m and total chip with testing pads takes an area of 800 $\mu$m by 550 $\mu$m. Under the 3.3 V power supply, the VGA consumes 9.2 mA excluding the output buffer which draws 8 mA.

The frequency response of the proposed VGA is shown in Figure 11 with control voltage $V_p$ ranging from 1.96 V to 2.18 V. At the maximum gain of 61 dB, the simulated 3-dB bandwidth is 2.5 GHz, and at the minimum gain of −19 dB, the bandwidth is 2.0 GHz. Thanks to the broadband character of the Cherry-Hooper amplifier, the gain-bandwidth product at the maximum gain can achieve a quite competitive value of 2805 GHz. Figure 12 shows the voltage gain and linear-in-dB characteristics. The gain error is 4 dB over 80-dB gain range. The noise figure at maximum gain shown in Figure 13 is smaller than 15 dB over the entire band. The simulated input P1 dB is −10 dBm at −19 dB minimum gain and −65 dBm at 61 dB maximum gain as shown in Figure 14.

Table 1 compares the performance of the proposed VGA with other works and shows a competitive gain bandwidth product with the largest gain tuning range among other works.

## 5. Conclusions

The proposed VGA comprises two cascaded variable gain core, in which a hybrid current-steering current gain cell is inserted in the Cherry-Hooper amplifier to maintain a broad bandwidth while covering a wide gain range. The introduced hybrid current-steering cell can provide current transfer function equal to the conventional current-steering cell while maintaining a constant DC output current. Post-layout simulation results confirm that the proposed circuit achieves a 2 GHz 3-dB bandwidth with wide linear-in-dB gain tuning range from −19 dB up to 61 dB. The amplifier offers a competitive gain bandwidth product of 2805 GHz at the maximum gain for a 110-GHz $f_t$ BiCMOS technology.

Table 1: VGA performance comparison.

| | Gain range (dB) | Bandwidth (GHz) | GBP (GHz) | Power (mW) | Technology | Linear-in-dB |
|---|---|---|---|---|---|---|
| Wang et al. 2012 [8] | −10~50 | 2.2 | 700 | 2.5 | CMOS 90 nm | No |
| Kumar et al. 2010 [2] | −10~10 | 4 | 12 | 9 | SiGe 0.18 um | No |
| Manstretta and Dauphinee 2007 [4] | −30~30 | 1 | 32 | 250 | SiGe 0.18 um | No |
| Jianhong et al. 2007 [5] | −17~16 | 0.4~0.8 | 6 | 22 | CMOS 0.18 um | No |
| Chang et al. 2009 [6] | −10~17 | 0.9 | 7 | 40 | SiGe 0.35 um | Yes |
| This work | −19~61 | 2 | 2805 | 31 | SiGe 0.18 um | Yes |

The amplifier core consumes 31 mW from a 3.3 V supply and occupies active area of 280 $\mu$m by 140 $\mu$m.

## Conflict of Interests

The authors declare that they have no conflict of interests regarding the publication of this paper.

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